4GB / 8GB Radiation Tolerant DDR4 Memory

Datasheet DS 60S 219460 (F)

Product Summary

The 4GB / 8GB Radiation Tolerant DDR4 Memory Multi-Chip Package (MCP) is a Ultra High Density Memory Solution, targeting Space Embedded Systems & Applications.
Such MCP products achieve significantly higher memory performance and density per cubic inch than using several discrete memories.

Top level Features

- Density 4GB / 8GB
- Bus width 72 bits (64 bits data + 8 bits ECC)
- Speed Up to 2400 MT/s
- Module size 15 mm x 20 mm x 1.92 mm
- Solder Spheres Count 391
- Pitch 0.8 mm
- Mass 1.2g +/- 0.1g

Space Key Features

- **Space Qualification**:
  - Up to NASA Level 1 (based on NASA EEE-INST-002 - Section M4 – PEMs)
  - Up to ECSS Class 1 (ECSS-Q-ST-60-13C)

- **Radiation Tolerance (for NASA and ECSS Flight Models):**

Revision A (column “Rev” of the Ordering information standing for product revision):

  - SEL LET Threshold > 60.88 MeV.cm²/mg
  - SEU evaluated from LET 2.6 MeV.cm²/mg & Upset cross-section @ 60.88 MeV.cm²/mg = 8.73E-12 cm²/bit
  - SEFI evaluated from LET 2.6 MeV.cm²/mg & SEFI cross-section @ 60.88 MeV.cm²/mg = 4.17E-4 cm²/device
  - TID tolerance: 100 krad(Si)
  - Protons: Data is available up to 190MeV

Revision B (column “Rev” of the Ordering information standing for product revision)

- SEL LET Threshold > 62.5 MeV.cm²/mg
- SEU LET sensitivity Threshold: Under characterization
- Logic error sensitivity Threshold: Under characterization
- TID targeted tolerance: 100 krad(Si)
- Protons: Data will be available up to 190MeV

- **Low outgassing**
  - Compliant with ASTM 595 and ESCC-Q-ST-70-02 for Revision A (“Rev” column in Ordering Information)
  - Under assessment for Revision B (“Rev” column in Ordering Information)

Revision History

Date	Revision	Description
2023	F	Change radiation tolerance sentence Add X1 reference in Ordering information Add note column on table 6 ball description Add 7.5 DDR4 power consumption
2023	E1	“Proprietary and Confidential” removed
2022	E	Update with 8GB information and ordering Information
2021	D	Add Capacitors note Add Outgassing feature Preliminary” removed Add Mass Add Differential Clock Termination scheme Add DDR4P and Grade notes in “Ordering Information” Add new references in “orderable parts” SEU LET sensitivity Theshold changed to 2.6 MeV
2020	C	Temperature compensated refresh only operates on -40 to 105°C temperature range Update of mechanical outline and orderable parts list/table Add termination resistor value Correction of ball size from 0.5 to 0.4 mm
2020	B	Update of « Ordering Information » Add ball’s information; Add orderable parts Change TID target to 100krad Add die configuration and notes Add Mass for RoHS parts Change PadOut picture Add Parity pin
2020	A	Initial Baseline Release

Ordering Information

Product Name	Radiation Performance	DDR Size[2]	Bus width	Temperature Range[2]	Package Type[2]	Speed (MT/s)	Rev	Grade[3]
DDR4[1]	T : Rad Tol	04G : 4 GByte 08G : 8 GByte	72 : 72 bits	M : -55/125C A : -40/105C	ZR : PBGA Stacked Wire Bond (Leaded SnPb) ZS : PBGA Stacked Wire Bond (Lead-free RoHS)	1 : 2133 2 : 2400	A B	EM : Engineering Models EQM : Engineering Qualification Models -N1 : Nasa Level 1 -N2 : Nasa Level 2 -N3 : Nasa Level 3 -E1 : ECSS Class 1 -E2 : ECSS Class 2 -E3 : ECSS Class 3 -X1 : Specific screening flow

Notes:

(1) “DDR4**P**” prototypes are functional devices dedicated to particular uses. Please contact Teledyne e2v sales office to know more about it

(2) For availability of the different versions, contact Teledyne e2v sales office.

(3) To know more about grades please refer to NE60S220869 on our website (ne-60s-220869-b0.pdf (teledyneimaging.com)

Orderable Parts

Available EM:

DDR4T04G72AZR1AEM (4GB - [-40/105°C] - Leaded SnPb - 2133MT/s)
DDR4T04G72AZR2AEM (4GB - [-40/105°C] - Leaded SnPb - 2400MT/s)

Available EQM, FM or X1:

DDR4T04G72AZR1A**XXX*** (4GB - [-40/105°C] - Leaded SnPb-2133MT/s)
DDR4T04G72AZR2A**XXX*** (4GB - [-40/105°C] - Leaded SnPb-2400MT/s)

DDR4T04G72MZR1A**XXX*** (4GB - [-55/125°C] - Leaded SnPb-2133MT/s)
DDR4T04G72MZR2A**XXX*** (4GB - [-55/125°C] - Leaded SnPb-2400MT/s)

*Note: "**XXX**" should be replaced by Grades: EQM, -N1, -N2, -N3, -E3, -X1

Table of Contents

1 Introduction

The 4GB / 8GB Radiation Tolerant DDR4 Memory Multi-Chip Package (MCP) is a Ultra High Density Memory Solution, targeting Space Systems & Applications.
Such MCP products achieve significantly higher memory performance and density per cubic inch than using multiple discrete memories.

1.1 Features

- JEDEC Standard Power Supply
  - VDD = 1.2V ± 5% (VDDQ is not used)
  - External VPP = 2.5 Volt +10%, -5%
- 391 ball MCP
- Die configuration(1):
  - 4GB parts are based on x16 die configuration (2)
  - 8GB parts are based on x8 die configuration
- 1.2V Pseudo-open drain I/O (POD12) DQ lines
- Internally generated VrefDQ
- ECC recovery from command and parity errors
- Programmable CAS Latency: 13,15,16,17,19
- Programmable CAS Write Latency (CWL).
- Programmable Additive Latency (Posted CAS)
- Per DRAM addressability is supported
- Data Bus Inversion support for x8 and x16 devices
- Command/Address (CA) Parity
- On-chip CA Parity detection for the CA bus
- Databus write cyclic redundancy check (CRC)
- Output Driver Calibration
- Reduced interconnect routing
- Reduced trace lengths due to the highly integrated, impedance matched packaging
- Thermally enhanced packaging technology allows silicon integration without performance degradation due to power dissipation (heat)
- Selectable Fixed burst chop of 4 (BC4) and burst length of 8 (BL8) on-the-fly (OTF) via the mode register set (MRS)
- 8n prefetch with 2 bank groups: 8 banks (2 bank groups x 4 banks per bank group)
- Separate activation, read, write, refresh operations for each bank group
- 7 mode registers
- Dynamic On-Die-Termination (ODT) and ODT Park for improved signal integrity.
- Self Refresh, Self Refresh abort and several
  Power Down Modes

- DLL-off mode for power savings
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern
- Asynchronous Reset
- Bidirectional Differentially Buffered Data Strobes
- SnPb and RoHS Compliant package available
- Temperature Compensated Refresh for operating temperature: Extended -40 to 105°C

Notes:

Refer to ‘table 2’ for more details on the differences between 4GB and 8GB devices

ECC uses only the lower byte of the x16 die, the upper byte is not connected

1.2 Benefits

- Very small footprint: saves board space versus implementation with discrete components
- Very high memory capacity per cubic inch
- Very high memory bandwidth per cubic inch
- Rugged: soldered-down PBGA
- Superior signal integrity
- 0.8 mm pitch: leadfree and leaded ball options
- Suitability for use in High-Rel and Space applications requiring Mil-Temp range, small form factor, non-hermetic operation

1.3 Design Considerations

1.3.1 Data Sheet Information

- This product and/or its specifications are subject to change without notice.
- The latest data sheet document should be retrieved from Teledyne e2v, prior to your design consideration.

1.3.2 Design Guide

General design guidelines are provided in the following table. More details can be found in the general user guide of the memory (available on request)

Table 1: DDR4 Design Guide

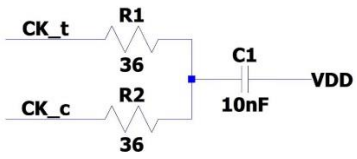
Item	Description	Implementation Suggestion
JEDEC	JEDEC Standards	Follow guidelines per JEDEC Standards and Host Memory Interface requirements
Placement	DDR4 Interface between MCP & Host / Memory Controller	The MCP should be placed as close as possible to the processor/memory controller, with direct / straight interconnect between them.
Rtt Termination	Termination for DDR4 address/command/control signals	Incorporated in MCP - not required externally The nominal value of the termination resistors is 69.8 ohms
Differential Clock Termination	Clock Termination for DDR differential clock input signal	Incorporated in MCP - not required externally 
Decoupling	High Speed Decoupling	The MCP incorporates some decoupling capacitors. For recommended external decoupling scheme please refer to the general user guide.
Bulk Decoupling	Low speed / low frequency	Refer to general user guide
Plane	Power	Must incorporate Power Plane for good and effective power distribution
Plane	Ground	Must incorporate Ground Plane for good return path
Thermal	Need to have extremely efficient heat dissipation paths	Incorporate as many thermal relief vias as possible such as via in pad in Ground plane with copper fill or highly thermally conductive material fill
Trace impedance	Impedance	Follow DDR4 impedance guidelines per signal group.
Trace Spacing	Crosstalk	Traces shall be spaced such that crosstalk in minimized
Trace Lengths	Data Byte Lanes	Trace lengths for each Byte Lane shall be tuned to be within 1%
Trace Lengths	Address & Command	Trace lengths for all Address and Control signals shall be tuned to be within 5%
Calibration	Zq resistor for drive strength calibration	Teledyne e2v recommends adding an external ZQ resistor population option to the motherboard layout (Zq=240 ohm +/- 1%).
BG1 - 8GB capacity support	Future migration to support 8GB capacity	BG1 should be routed to Host/Memory Controller for future migration to support 8GB capacity
Signal Integrity Simulation	End to End Simulation of all I/O signals	It is critical that simulation be done end to end from Host / Memory Controller to MCP package. Simulation should be done for each signal group i.e. Data, Address/Command, Control, Clock
Simulation Model	MCP Package, Die Models	Spice model of the MCP package and IBIS model for the die as well as EBD model are available from Teledyne e2v
Signal Integrity Simulation Model	Host / Memory Controller	Customer to use appropriate model for the Host / Memory Controller supplied by the respective manufacturer
Power consumption estimation	Power calculation spreadsheet	This can be supplied by Teledyne e2V
Thermal Simulation Model	MCP thermal model	This can be supplied by Teledyne e2v in Icepack or ECXML format

Table 2: Future Migration from 4GB to 8GB

Signal	Implementation
BG1	To support future migration to 8GB part, this signal should be connected to the Host / Memory Controller. All other signals are applicable for both capacities. BG1 signal is not used in 4GB parts.
ZQ0 thru ZQ8	Calibration Reference - To support future migration to 8GB part, connect all 9 ZQx signals to GND via 240Ω 1% Resistor and install them. ZQ1, ZQ3, ZQ5, ZQ7 signals are not used in 4GB parts.

1.4 Mapping of MCP signals to JEDEC DDR4 288pin UDIMM & DDR4 260 pin SO-DIMM signals.

For mapping of MCP signals to JEDEC DDR4 288pin UDIMM & DDR4 260 pin SO-DIMM signals, see Appendix A & B.

1.5 DDR4 SPEED BINs and Timing Summary

Table 3: DDR4 SPEED BIN Nomenclature

Speed	Clock
DDR4-1866	933 MHz
DDR4-2133	1066 MHz
DDR4-2400	1200 MHz

Table 4: DDR4 Timing Summary

MT/s	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR4-1866	1.071	13	13.92	13.92	34	47.92	13-13-13
DDR4-2133	0.93	15	14.06	14.06	33	47.05	15-15-15
DDR4-2400	0.83	17	14.16	14.16	32	46.16	17-17-17

Notes:
CL = CAS Latency, tRCD = Activate –to-Command Time, tRP = Precharge Time. Refer to Speed Bin tables for details.

1.6 Addressing

Table 5: Addressing

		4GB : 512Mx72	8GB : 1024Mx72
Bank Address	# of Bank Groups	2	4
	BG Address	BG0	BG0,BG1
	Bank Address in a BG	BA0 to BA1	BA0 to BA1
Bank Count per Group		4	4
Row Address		64K(A0 to A15)	64K(A0 to A15)
Column Address		1K(A0 to A9)	1K(A0 to A9)
Die Organization		8Gb (512M x 16), 8 Banks	8Gb (1024M x 8), 16 Banks
MCP Rank Address		CS0_n	CS0_n

2 DDR4 MCP Ball Assignments

2.1 MCP Data Byte Ball Assignments (4GB/8GB)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VPP	GND	VDD	GND	VDD	GND	DQ30	GND	VDD	GND	DQ25	GND	DQ22	GND	DQ19	DQ17	GND
B	GND	NC	GND	NC	VDD	NC	DQ28	GND	DQ29	GND	DQ27	VDD	DQ20	GND	DQ16	VDD	DQS2_c
C	NC	NC	NC	NC	GND	NC	NC	GND	DQ31	ZQ2	DQ26	DQS3_t	DQ23	DQ21	DQ18	GND	DQS2_t
D	NC	NC	NC	NC	NC	GND	NC	VDD	DQ24	ZQ3	DM3_n /DBI3_	DQS3_c	NC	GND	VDD	DM2_n /DBI2_	GND
E	NC	NC	GND	NC	NC	NC	GND	GND	VDD	GND	VDD	GND	DQ15	VDD	GND	DQ9	VPP
F	NC	NC	NC	NC	GND	NC	NC	VDD	DQ3	ZQ1	GND	DQS0_c	DQ12	GND	DQ10	GND	DQS1_t
G	NC	NC	NC	NC	GND	NC	DQ7	VDD	DQ2	ZQ0	DM0_n /DBI0_	DQS0_t	DQ13	VDD	DQ8	VDD	DQS1_c
H	GND	VDD	GND	VDD	VDD	GND	DQ4	GND	DQ5	ZQ8	DQ1	VDD	DQ14	GND	DQ11	DM1_n /DBI1_	GND
J	VTT	GND	VDD	GND	VDD	VDD	DQ6	NC	GND	NC	DQ0	GND	CB7	CB5	DM8_n /DBI8_	CB1	DQS8_t
K	VDD	GND	GND	VDD	GND	VDD	GND	NC	CB6	NC	CB3	GND	CB4	CB2	GND	CB0	DQS8_c
L	A13	A9	ALERT_ n	A6	TEN	BA1	BG0	NC	A12/BC _n	NC	ACT_n	A14/W E_n	CS0_n	VDD	GND	VDD	VTT
M	A11	GND	A7	A1	RESET_ n	A4	GND	NC	VREFCA	NC	GND	A16/RA S_n	ODT0	CK_c	CK_t	GND	VTT
N	PARITY	A2	A8	A0	A5	A3	BA0	NC	A10/AP	NC	BG1	A15/CA S_n	CKE0	VDD	GND	VDD	VTT
P	VDD	GND	GND	VDD	GND	VDD	GND	NC	NC	NC	NC	GND	NC	NC	GND	NC	NC
R	VTT	GND	VDD	GND	VDD	VDD	DQ62	NC	GND	NC	DQ59	GND	NC	NC	NC	NC	NC
T	GND	VDD	GND	VDD	VDD	GND	DQ60	GND	DQ61	NC	DQ57	VDD	DQ54	GND	DQ51	DM6_n /DBI6_	GND
U	NC	NC	NC	NC	GND	NC	DQ63	VDD	DQ58	ZQ6	DQ52	DQ53	DQ55	VDD	DQ48	VDD	DQS6_c
V	NC	NC	NC	NC	GND	NC	NC	VDD	DQ56	ZQ7	GND	DM7_n /DBI7_	DQS7_t	GND	DQ50	GND	DQS6_t
W	NC	NC	GND	NC	NC	NC	GND	GND	VDD	GND	VDD	GND	DQS7_c	VDD	GND	DQ49	VPP
Y	NC	NC	NC	NC	NC	GND	NC	VDD	DQ39	ZQ5	DQ34	DQS4_c	NC	GND	VDD	DM5_n /DBI5_	GND
AA	NC	NC	NC	NC	GND	NC	NC	GND	DQ32	ZQ4	DM4_n /DBI4_	DQS4_t	DQ47	DQ45	DQ42	GND	DQS5_t
AB	GND	NC	GND	NC	VDD	NC	DQ38	GND	DQ37	GND	DQ33	VDD	DQ46	GND	DQ40	VDD	DQS5_c
AC	VPP	GND	VDD	GND	VDD	GND	DQ36	GND	VDD	GND	DQ35	GND	DQ44	GND	DQ43	DQ41	GND
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

- DataByte 0
- DataByte 0
- DataByte 1
- DataByte 2
- DataByte 3
- DataByte 4
- DataByte 5
- DataByte 6
- DataByte 7
- ECC Byte
- Clock
- Address
- Bank Group
- Miscellaneous
- Ground / VSS
- VREFCA
- VDD
- VPP
- VTT
- ZQ
- TEN
- No Connect

Top view, A1 top left corner

3 Ball Description

- Number of solder balls: 391
- Ball diameter: 0.4 mm
- Pitch: 0.80 mm
- Solder balls for leaded option: 63%Sn, 37%Pb
- Solder balls for Lead-free RoHS option: 96.5%Sn, 3%Ag, 0.5%Cu

Table 6: Ball Description

Symbol	Type	Function	Note
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.	
CKE0	Input	Clock Enable: CKE0 HIGH activates, and CKE0 Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE0 Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE0 is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE0, are disabled during power-down. Input buffers, excluding CKE0, are disabled during Self-Refresh.	1
CS0_n	Input	Chip Select: All commands are masked when CS0_n is registered HIGH. CS0_n provides for external Rank selection on systems with multiple Ranks. CS0_n is considered part of the command code.	1
ODT0	Input	On Die Termination: ODT0 (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT0 is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t,NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT0 is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT0 ball will be ignored if MR1 is programmed to disable RTT_NOM.	1
PARITY	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17;0], A10/AP, A12/BC_n, BA[1;0] and BG[1;0] with C0, C1 and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density and configuration specific should be treated internally as 0s by the DRAM pariy logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.	1
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS0_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.	1
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS0_n) define the command being entered. Those balls have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command balls for Read, Write and other command defined in command truth table.	1
DM_n/DBI_n/ TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.	
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.	1
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.	1

Symbol	Type	Function	Note
A0-A13, A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.	1
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.	
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.	
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.	
DQ<63:00>	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0toDQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.	
CB<7:0>	Input / Output	Check Bit Input/ Output: Bi-directional ECC portion of data bus for x72 configurations	
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.	
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. This signal is internally pulled-up to VDD with a 51Ω resistor. No external resistor is required.	
TEN	Input	Boundary Scan Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this ball will enable boundary scan operation along with other balls. It is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.	
NC		No Connect: No internal electrical connection is present.	
V_{DD}	Supply	Power Supply: 1.2 V +/- 0.06 V	
GND	Supply	Ground	
V_{TT}	Supply	Power Supply: 0.6 V +/- 3%	
Vpp	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)	
VREFCA	Supply	Reference voltage for CA	
ZQ	Supply	Reference Ball for ZQ calibration	

Note:

1) No external termination required on input only balls

4 MECHANICAL OUTLINE - PACKAGE DETAILS

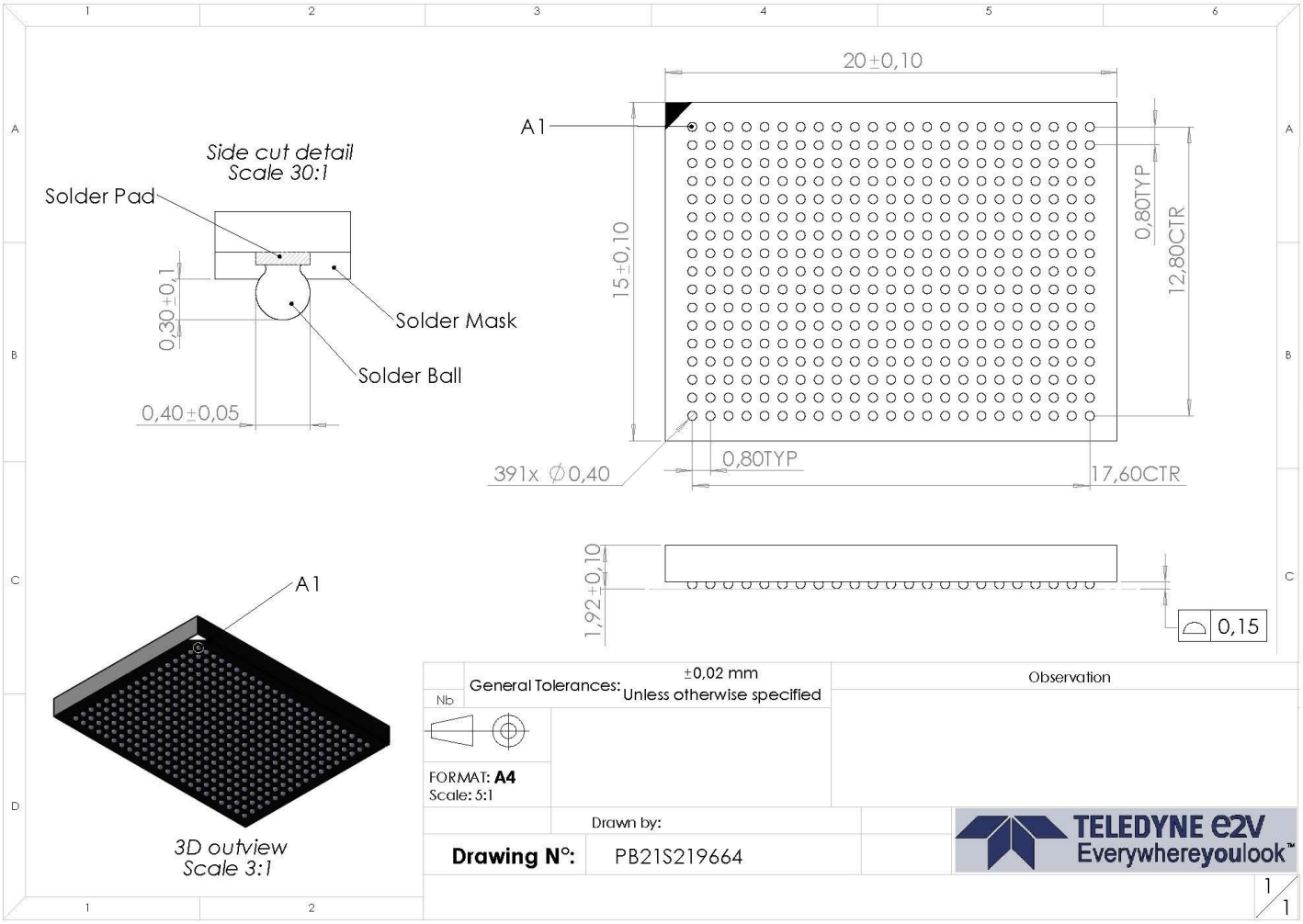


Figure 1. MECHANICAL OUTLINE - PACKAGE DETAILS

5 DDR4 MODE REGISTERS

5.1 Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MR*n*) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. The MRS command cycle time, tMRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the tMRD Timing figure. Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply tMRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode
- Per-DRAM addressability
- Maximum power saving mode
- CS to command/address latency
- CA parity latency mode
- VREFDQ training value
- VREFDQ training mode
- VREFDQ training range

Some mode register settings may not be supported because they are not required by certain speed bins.

5.1.1 tMRD Timing Diagram

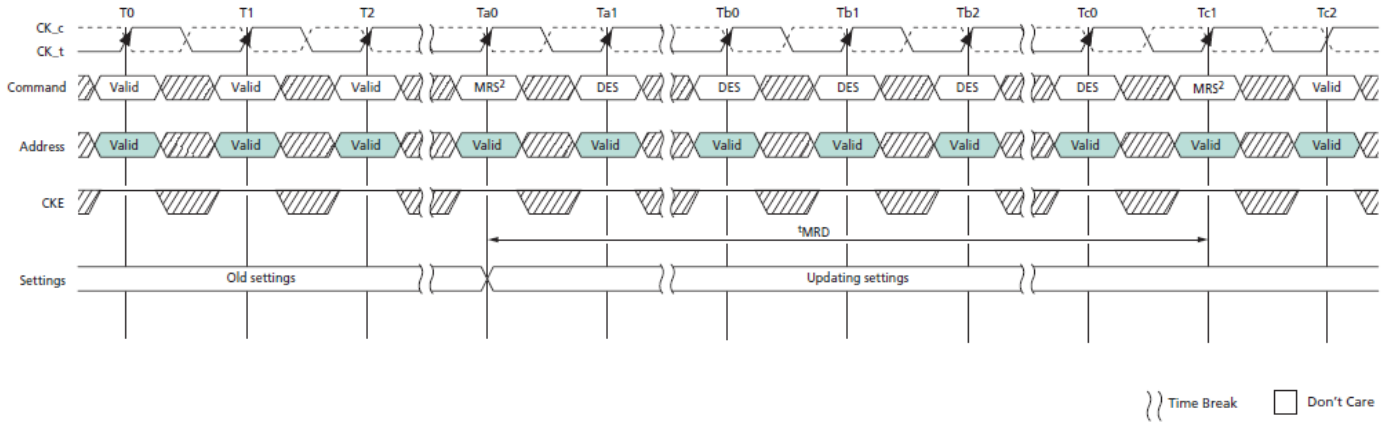


Figure 2. tMRD Timing

Notes:

This timing diagram depicts CA parity mode "disabled" case.
tMRD applies to all MRS commands with the following exceptions:
Gear-down mode
CA parity mode
CAL mode
Per-DRAM addressability mode
VREFDQ training value, VREFDQ training mode, and VREFDQ training range

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET. tMOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the tMOD Timing figure.

5.1.2 tMOD Timing Diagram

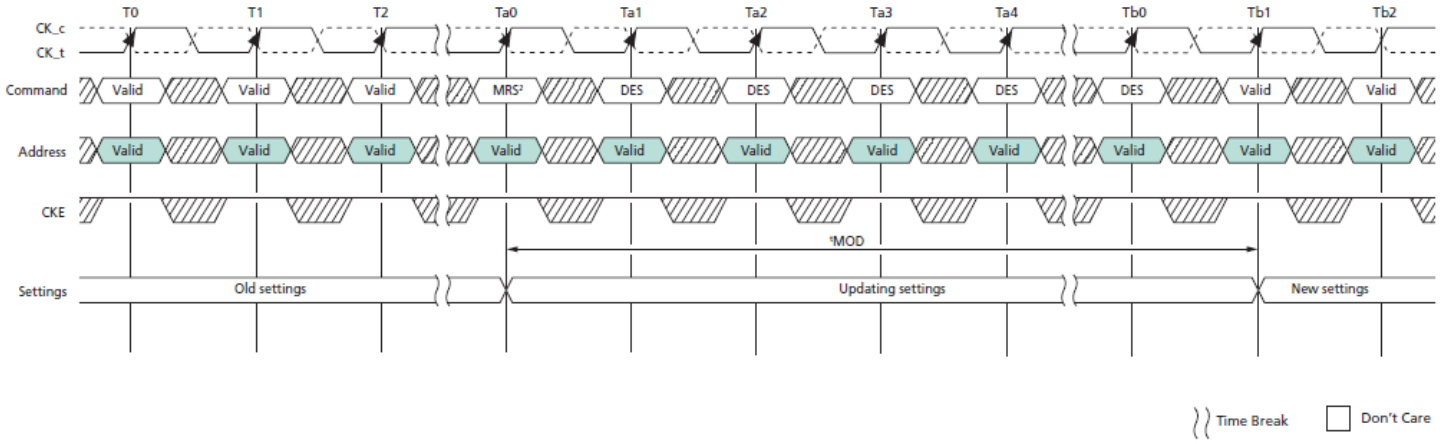


Figure 3. tMOD Timing

Notes

This timing diagram depicts CA parity mode “disabled” case.

tMOD applies to all MRS commands with the following exceptions:
DLL enable, Gear-down mode
VREFDQ training value, internal VREF training monitor, VREFDQ training mode, and VREFDQ training range
Maximum power savings mode , Per-DRAM addressability mode, and CA parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with tRP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the RTT(NOM) feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring RTT is in an off state prior to the MRS command. The ODT signal may be registered HIGH after tMOD has expired. If the RTT(NOM) feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes. In some mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

5.2 MODE REGISTER 0

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Table 7: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS _n	CAS _n	WE _n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 8: MR0 Register Definition

Mode Register 0	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** **000 = MR0** 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13,11:9	**WR (WRITE recovery)/RTP (READ-to-PRECHARGE)** 0000 = 10 / 5 clocks1 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks1 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks1 0101 = 20 /10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks1 1000 = 26 / 13 clocks1 1001 through 1111 = Reserved
8	**DLL reset** 0 = No 1 = Yes
7	**Test mode (TM) – Manufacturer use only** 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	**CAS latency (CL) – Delay in clock cycles from the internal READ command to first data-out** 00000 = 9 clocks1 00001 = 10 clocks 00010 = 11 clocks1 00011 = 12 clocks 00100 = 13 clocks1 00101 = 14 clocks 00110 = 15 clocks1 00111 = 16 clocks 01000 = 18 clocks 01001 = 20 clocks 01010 = 22 clocks 01011 = 24 clocks 01100 = 23 clocks1 01101 = 17 clocks1 01110 = 19 clocks1 01111 = 21 clocks 1 10000 = 25 clocks (3DS use only) 10001 = 26 clocks 10010 = 27 clocks (3DS use only) 10011 = 28 clocks 10100 = 29 clocks1

Mode Register 0	Description
	10101 = 30 clocks 10110 = 31 clocks1 10111 = 32 clocks
3	Burst type (BT) – Data burst ordering within a READ or WRITE burst access 0 = Nibble sequential 1 = Interleave
1:0	**Burst length (BL) – Data burst size associated with each read or write access** 00 = BL8 (fixed) 01 = BC4 or BL8 (on-the-fly) 10 = BC4 (fixed) 11 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

5.2.1 Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 9: Burst Type and Burst Order

Note 1 applies to the entire table

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	3

Notes:

0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.

When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks as described in the BC4 (fixed) case.

T = Output driver for data and strobes are in High-Z.
V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
X = “Don’t Care.”

5.2.2 CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

5.2.3 Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No perations or functionality is specified if MR0[7] = 1.

5.2.4 Write Recovery(WR)/READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine tDAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing t_{WR} (in ns) by tCK (in ns) and rounding up to the next integer: WR (MIN) cycles = roundup (t_{WR} [ns]/tCK[ns]). The WR value must be programmed to be equal to or larger than t_{WR} (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; t_{WR} values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data. Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer: RTP (MIN) cycles = roundup (tRTP[ns]/tCK[ns]). The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with tRP to determine the ACT timing to the same bank.

5.2.5 DLL RESET

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, tDLLK must be met before functions requiring the DLL can be used, such as READ commands or synchronous ODT operations, for example,).

5.3 MODE REGISTER 1

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Table 10: Address Pin Mapping

Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 11: MR1 Register Definition

Mode Register 1	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 **001 = MR1** 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	RFU 0 = Must be programmed to 0 1 = Reserved
12	Data output disable (Qoff) – Output buffer disable 0 = Enabled (normal operation) 1 = Disabled (both ODI and RTT)
11	Termination data strobe (TDQS) – Additional termination pins (x8 configuration only) 0 = TDQS disabled 1 = TDQS enabled
10, 9, 8	Nominal ODT (RTT(NOM) – Data bus termination setting (Zq=240 ohm) 000 = RTT(NOM) disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
7	Write leveling (WL) – Write leveling mode 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)
6, 5	RFU 0 = Must be programmed to 0 1 = Reserved
4, 3	Additive latency (AL) – Command additive latency setting 00 = 0 (AL disabled) 01 = CL - 11 10 = CL - 2 11 = Reserved

Mode Register 1	Description
2, 1	Output driver impedance (ODI) – Output driver impedance setting (Zq=240 ohm) 00 = RZQ/7 (34 ohm) 01 = RZQ/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm) 11 = Reserved
0	DLL enable – DLL enable feature 0 = DLL disabled 1 = DLL enabled (normal operation)

5.3.1 DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when RTT(WR) is enabled and the DLL is required for proper ODT operation.
The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT(NOM) bits MR1[9,6,2] = 000 via an MRS command during DLL off mode. The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set RTT(WR), MR2[10:9] = 00.

5.3.2 Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

5.3.3 ODT RTT(NOM) Values

The device is capable of providing three different termination values: RTT(Static), RTT(NOM), and RTT(WR). The nominal termination value, RTT(NOM), is programmed in MR1. A separate value, RTT(WR), may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITE operations. The RTT(WR) value can be applied during WRITE commands even when RTT(NOM) is disabled. A third RTT value, RTT(Static), is programmed in MR5. RTT(Static) provides a termination value when the ODT signal is LOW.

5.3.4 Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 12: Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note: 1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

5.3.5 Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

5.3.6 Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring MCP power. For normal operation, set MR1[12] to 0.

5.3.7 Termination Data Strobe

Termination data strobe (TDQS) is a feature of the x8 device and provides additional termination resistance outputs that may be useful in some system configurations. Because this function is available only in a x8 configuration, it must be disabled for x4 and x16 configurations. While TDQS is not supported in x4 or x16 configurations, the same termination resistance function that is applied to the TDQS pins is applied to the DQS pins when enabled via the mode register. The TDQS, DBI, and DATA MASK (DM) functions share the same pin. When the TDQS function is enabled via the mode register, the DM and DBI functions are not supported. When the TDQS function is disabled, the DM and DBI functions can be enabled separately.

Table 13: TDQS Function Matrix

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	**Enabled** or disabled
Disabled	Enabled	**Enabled** or disabled	
Disabled	Disabled	**Enabled** or disabled	
Enabled	Disabled	Disabled	Disabled

5.4 MODE REGISTER 2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Table 14: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 15: MR2 Register Definition

Mode Register 2	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	TRR mode 0 = Disabled 1 = Enabled
12	WRITE data bus CRC 0 = Disabled 1 = Enabled
11:9	Dynamic ODT (RTT(WR)) – Data bus termination setting during WRITEs (Zq=240 ohm) 000 = RTT(WR) disabled (WRITE does not affect RTT value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm) 101 = Reserved 110 = Reserved 111 = Reserved
7:6	Low-power auto self refresh (LPASR) – Mode summary 00 = Manual mode - Normal operating temperature range (TC: 0°C–85°C) 01 = Manual mode - Reduced operating temperature range (TC: 0°C–45°C) 10 = Manual mode - Extended operating temperature range (TC: 0°C–95°C) 11 = ASR mode - Automatically switching among all modes
5:3	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1tCK WRITE preamble 000 = 9 (DDR4-1600)1 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600)1 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2tCK WRITE preamble

Mode Register 2	Description
	000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	TRR mode - BGn control 00 = BG0 01 = BG1 10 = BG2 11 = BG3
1:0	TRR mode - BAn control 00 = BA0 01 = BA1 10 = BA2 11 = BA3

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

5.4.1 CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

5.4.2 Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

5.4.3 Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT (RTT(WR)) settings in MR2[11:9]. In write leveling mode, only RTT(NOM) is available.

5.4.4 Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

5.4.5 Target Row Refresh Mode

For the device, rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (tMAW) before the adjacent rows need to be refreshed regardless of how the activates are distributed over tMAW. The row receiving the excessive activates is the target row (TR*n*); the two adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TR*n*, either the device must receive (roundup of tMAW / tREFI) REFRESH commands (REF) before another row activate is issued, or it needs to be placed into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TR*n* that encountered the MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the activates from two target rows on a victim row should not exceed the MAC value as well. When the temperature controlled refresh (TCR) mode is enabled, tMAW should be adjusted depending on the TCR range as shown in the following table. Using TRR mode is not required, and in some cases has been rendered inoperable, as the device automatically performs TRR Mode in the background.

5.5 MODE REGISTER 3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 16: Address Pin Mapping

Address Pin Mapping																					
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 17: MR3 Register Definition

Mode Register 3	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	RFU 0 = Must be programmed to 0 1 = Reserved
12:11	Multipurpose register (MPR) – Read format 00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
10:9	WRITE CMD latency when CRC/DM enabled 0 = 4CK (DDR4-1600) 01 = 5CK (DDR4-1866/2133/2400) 10 = 6CK (DDR4-2666/2933/3200) 11 = Reserved
8:6	Fine granularity refresh mode 000 = Normal mode (fixed 1x) 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 110 = On-the-fly 1x/4x 111 = Reserved
5	Temperature sensor statu 0 = Disabled 1 = Enabled
4	Per-DRAM addressability 0 = Normal operation (disabled) 1 = Enable

Mode Register 3	Description
3	Gear-down mode – Ratio of internal clock to external data rate 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	Multipurpose register (MPR) access 0 = Normal operation 1 = Data flow from MPR
1:0	MPR page select 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

5.5.1 Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MR*n* registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

5.5.2 WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled.

5.5.3 Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

5.5.4 Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

5.5.5 Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

5.5.6 Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode,
no MRS command or sync pulse is required.

5.6 MODE REGISTER 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Table 18: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 19: MR4 Register Definition

Mode Register 4	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	Post Package Repair (PPR mode) 0 = Disabled 1 = Enabled
12	WRITE preamble setting 0 = 1tCK toggle1 1 = 2tCK toggle
11	READ preamble setting 0 = 1tCK toggle1 1 = 2tCK toggle (When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.)
10	READ preamble training 0 = Disabled

Mode Register 4	Description
	1 = Enabled
9	Self refresh abort mode 0 = Disabled 1 = Enabled
8:6	CMD (CAL) address latency 000 = 0 clocks (disabled) 001 =3 clocks1 010 = 4 clocks 011 = 5 clocks1 100 = 6 clocks 101 = 8 clocks 110 = Reserved 111 = Reserved
5	soft Post Package Repair (sPPR mode) 0 = Disabled 1 = Enabled
4	Internal VREF monitor 0 = Disabled 1 = Enabled
3	Temperature controlled refresh mode 0 = Disabled 1 = Enabled
2	Temperature controlled refresh range 0 = Normal temperature mode 1 = Extended temperature mode
1	Maximum power savings mode 0 = Normal operation 1 = Enabled
0	RFU 0 = Must be programmed to 0 1 = Reserved

Note:

Not allowed when 1/4 rate gear-down mode is enabled.

5.6.1 Post Package Repair Mode

The post package repair (PPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether PPR mode is available (A7 = 1) or not available (A7 = 0). PPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank group can be repaired. The repair process is irrevocable so great care should be exercised when using.

5.6.2 Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank group can be repaired. The repair process is revocable by either doing a reset or power-down.

5.6.3 WRITE Preamble

Programmable WRITE preamble, t_{WPRE}, can be set to 1tCK or 2tCK via the MR4 register. The 1tCK setting is similar to DDR3. However, when operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

5.6.4 READ Preamble

Programmable READ preamble tRPRE can be set to 1tCK or 2tCK via the MR4 register. Both the 1tCK and 2tCK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training. When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

5.6.5 READ Preamble Training

Programmable READ preamble training can be set to 1tCK or 2tCK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

5.6.6 Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C, while the extended temperature range covers 0°C to 95°C.

5.6.7 Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [tCK(ns)/tCAL(ns)].

5.6.8 Internal VREF Monitor

The device generates its own internal VREFDQ. This mode may be enabled during VREFDQ training, and when enabled, VREF,time-short and VREF,time-long need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

5.6.9 Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

5.7 MODE REGISTER 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Table 20: Address Pin Mapping

Address Pin Mapping																					
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 21: MR5 Register Definition

Mode Register 5	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	N/A on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	RFU 0 = Must be programmed to 0 1 = Reserved
12	Data bus inversion (DBI) – READ DBI enable 0 = Disabled 1 = Enabled
11	Data bus inversion (DBI) – WRITE DBI enable 0 = Disabled 1 = Enabled
10	Data mask (DM) 0 = Disabled 1 = Enabled
9	CA parity persistent error mode 0 = Disabled 1 = Enabled
8:6	Parked ODT value (RTT(Park)) (Zq=240 ohm) 000 = RTT(Park) disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
5	ODT input buffer for power-down 0 = Buffer enabled 1 = Buffer disabled

Mode Register 5	Description
4	CA parity error status 0 = Clear 1 = Error
3	CRC error status 0 = Clear 1 = Error
2:0	CA parity latency mode 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400)1 011 = 6 clocks (DDR4-2666) 100 = 8 clocks (DDR4-2933/3200) 101 = Reserved 110 = Reserved 111 = Reserved

Note:

Not allowed when 1/4 rate gear-down mode is enabled.

5.7.1 Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12. DBI is not allowed during MPR READ operations.

5.7.2 Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

5.7.3 CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

5.7.4 ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide RTT(NOM) termination. However, the device may provide RTT(Park) termination depending on the MR settings. This is primarily for additional power savings.

5.7.5 CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

5.7.6 CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

5.7.7 CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16 , CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

5.8 MODE REGISTER 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Table 22: Address Pin Mapping

Address Pin Mapping																						
Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note:

RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 23: MR6 Register Definition

Mode Register 6	Description
21	RFU 0 = Must be programmed to 0 1 = Reserved
20:18	MR select 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	NA on 4Gb and 8Gb, RFU 0 = Must be programmed to 0 1 = Reserved
13	RFU 0 = Must be programmed to 0 1 = Reserved

Mode Register 6	Description
12:10	tCCD_L 000 = 4 clocks (≤1333 Mb/s) 001 = 5 clocks (>1333 Mb/s and ≤1866 Mb/s) 010 = 6 clocks (>1866 Mb/s and ≤2400 Mb/s) 011 = 7 clocks (>2400 Mb/s and ≤2666 Mb/s) 100 = 8 clocks (>2666 Mb/s and ≤3200 Mb/s) 101 = Reserved 110 = Reserved 111 = Reserved
9, 8	**RFU** 0 = Must be programmed to 0 1 = Reserved
7	**VREF Calibration Enable** 0 = Disable 1 = Enable
6	**VREF Calibration Range** 0 = Range 1 1 = Range 2
5:0	VREF Calibration Value See the VREFDQ Range and Levels table in the VREFDQ Calibration section

5.8.1 t_{CCD_L} Programming

The device controller must program the correct t_{CCD_L} value. t_{CCD_L} will be programmed according to the value defined per operating frequency in the AC parameter table. Although JEDEC specifies the larger of 5nCK or Xns, Micron's DRAM supports the larger of 4nCK or Xns.

5.8.2 VREFDQ Calibration Enable

VREFDQ calibration is where the device internally generates its own VREFDQ to be used by the DQ input receivers. The VREFDQ value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal VREFDQ level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ calibration must be used whenever values are being written to the MR6[6:0] register.

5.8.3 VREFDQ Calibration Range

The device defines two VREFDQ calibration ranges: Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDD while Range 2 supports VREFDQ between 45% and 77% of VDD, as seen in VREFDQ Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

5.8.4 VREFDQ Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ, as seen in VREFDQ Range and Levels table in the VREFDQ Calibration section.

6 DQ Internal Vref Specifications

6.1 VREFDQ Calibration and Training

The VREFDQ level, which is used by the DRAM DQ input receivers, is internally generated. The DRAM VREFDQ does not have a default value upon power-up and must be set to the desired value, usually via VREFDQ calibration mode. If PDA or PPR modes are used prior to VREFDQ calibration, VREFDQ should initially be set at the midpoint between the VDD,max, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for VREFDQ calibration to determine the best internal VREFDQ level. The VREFDQ calibration is enabled/disabled via MR6[7], MR6[6] selects Range 1 (60% to 92.5% of VDD) or Range 2 (45% to 77.5% of VDD), and an MRS protocol using MR6[5:0] to adjust the VREFDQ level up and down. MR6[6:0] bits can be altered using the MRS command if MR6[7] is disabled. The DRAM controller will likely use a series of writes and reads in conjunction with VREFDQ adjustments to obtain the best VREFDQ, which in turn optimizes the data eye. The internal VREFDQ specification parameters are voltage range, step size, VREF step time, VREF full step time, and VREF valid level. The voltage operating range specifies the minimum required VREF setting range for DDR4 SDRAM devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust VREFDQ and optimize the timing and voltage margin of the DRAM data input receivers. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

6.1.1 VREFDQ Voltage Range

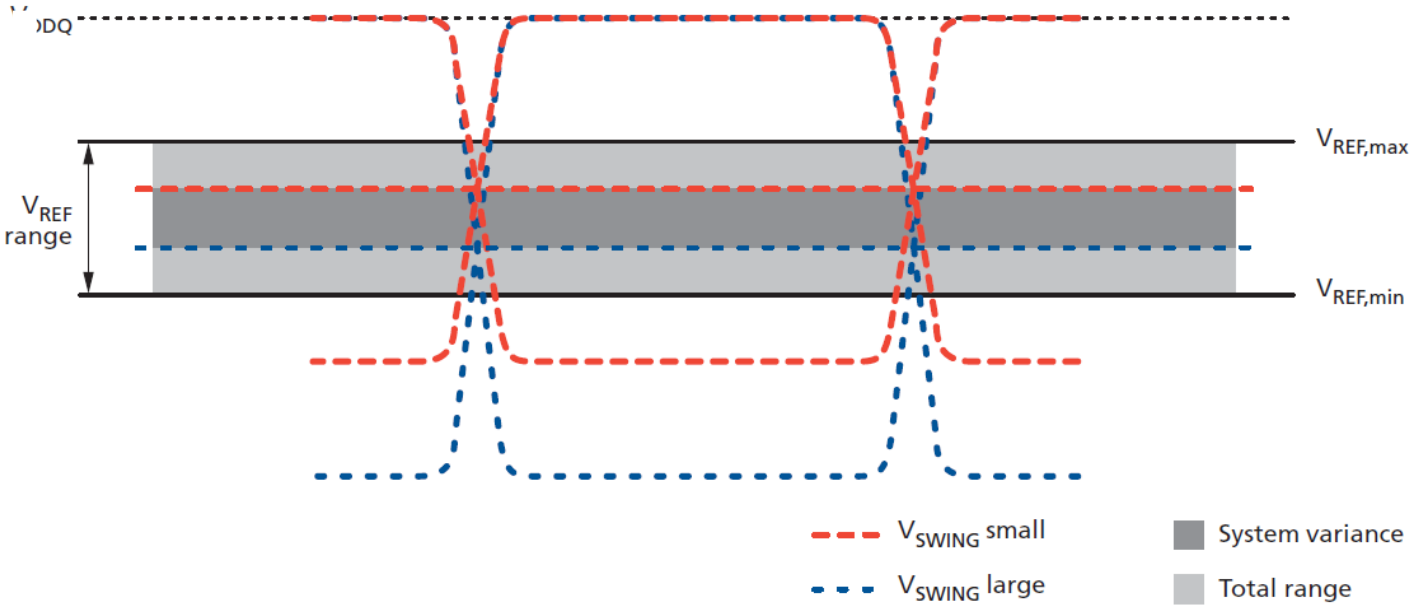


Figure 4. VREFDQ Voltage Range

6.1.2 VREFDQ Range and Levels

Table 24: VREFDQ Range and Levels

MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1	MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 = Reserved		

6.1.3 VREFDQ Step Size

The VREF step size is defined as the step size between adjacent steps. VREF step size ranges from 0.5% VDD to 0.8% VDD. However, for a given design, the device has one value for VREF step size that falls within the range. The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps n. The VREF set tolerance is measured with respect to the ideal line, which is based on the MIN and MAX VREF value endpoints for a specified range. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

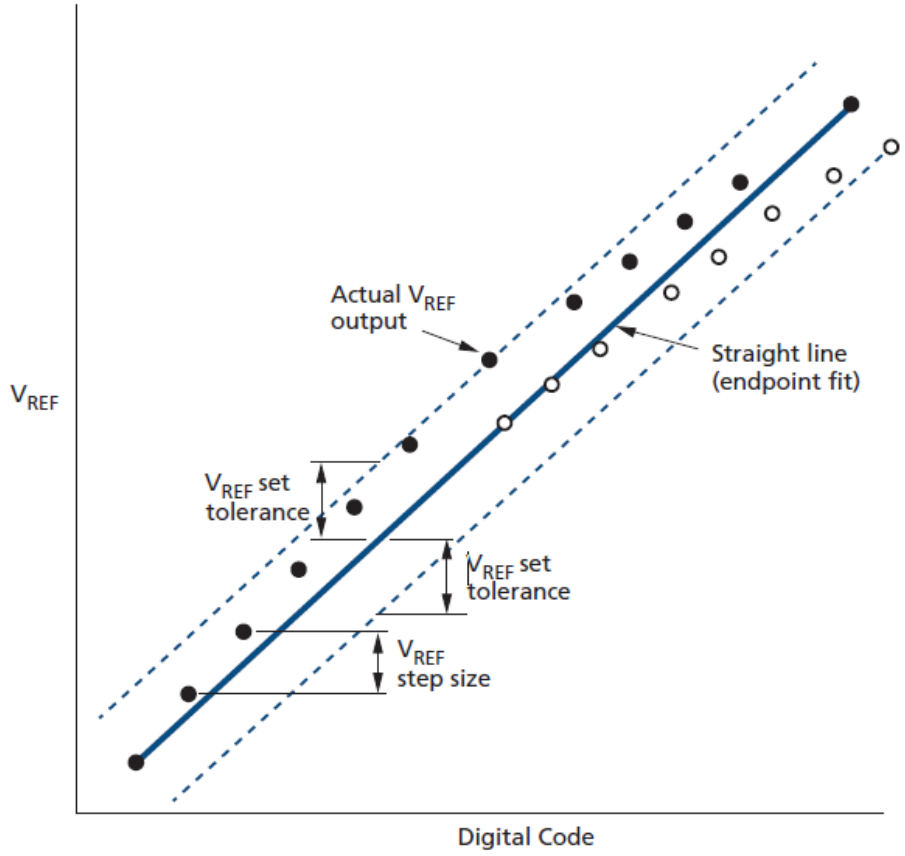


Figure 5. Example of VREF Set Tolerance and Step Size

Note: 1. Maximum case shown.

6.1.4 VREFDQ Increment and Decrement Timing

The VREF increment/decrement step times are defined by VREF,time. VREF,time is defined from t0 to t1, where t1 is referenced to the VREF voltage at the final DC level within the VREF valid tolerance (VREF,val_tol). The VREF valid level is defined by VREF,val tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment.

Note:
t0 is referenced to the MRS command clock
t1 is referenced to VREF,tol

6.1.4.1 VREFDQ Timing Diagram for VREF,time Parameter

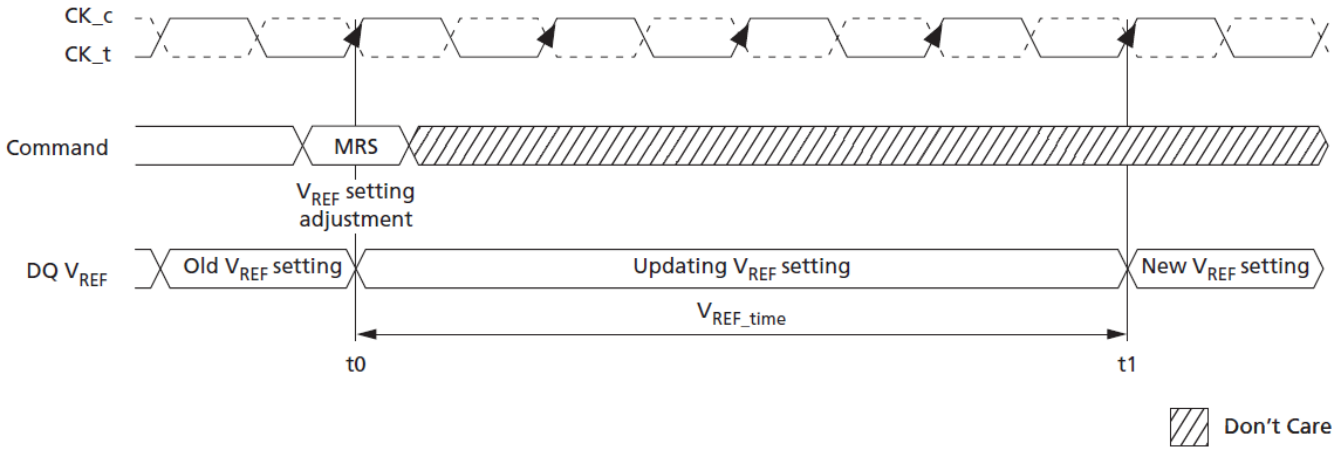


Figure 6. VREFDQ Timing Diagram for VREF,time Parameter

VREFDQ calibration mode is entered via an MRS command, setting MR6[7] to 1 (0 disables VREFDQ calibration mode) and setting MR6[6] to either 0 or 1 to select the desired range (MR6[5:0] are "Don't Care"). After VREFDQ calibration mode has been entered, VREFDQ calibration mode legal commands may be issued once tVREFDQE has been satisfied. Legal commands for VREFDQ calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set VREFDQ values, and MRS to exit VREFDQ calibration mode. Also, after VREFDQ calibration mode has been entered, “dummy” WRITE commands are allowed prior to adjusting the VREFDQ value the first time VREFDQ calibration is performed after initialization. Setting VREFDQ values requires MR6[7] be set to 1 and MR6[6] be unchanged from the initial range selection; MR6[5:0] may be set to the desired VREFDQ values. If MR6[7] is set to 0, MR6[6:0] are not written. VREF,time-short or VREF,time-long must be satisfied after each MR6 command to set VREFDQ value before the internal VREFDQ value is valid. If PDA mode is used in conjunction with VREFDQ calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only VREFDQ calibration mode legal commands noted above that may be used are the MRS commands: MRS to set VREFDQ values and MRS to exit VREFDQ calibration mode.
The last MR6[6:0] setting written to MR6 prior to exiting VREFDQ calibration mode is the range and value used for the internal VREFDQ setting. REFDQ calibration mode may be exited when the DRAM is in idle state. After the MRS command to exit VREFDQ calibration mode has been issued, DES must be issued until tVREFDQX has been satisfied where any legal command may then be issued. VREFDQ setting should be updated if the die temperature changes too much from the calibration temperature. The following are typical script when applying the above rules for VREFDQ calibration routine when performing VREFDQ calibration in Range 1:

- MR6[7:6]10 [5:0]XXXXXXX.
  - Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set VREFDQ values and exit VREFDQ calibration mode).
- All subsequent VREFDQ calibration MR setting commands are MR6[7:6]10 [5:0]VVVVVV.
  - "VVVVVV" are desired settings for VREFDQ.

- Issue ACT/WR/RD looking for pass/fail to determine VCENT (midpoint) as needed.
- To exit VREFDQ calibration, the last two VREFDQ calibration MR commands are:
  - MR6[7:6]10 [5:0]VVVVVV* where VVVVVV* = desired value for VREFDQ.
  - MR6[7]0 [6:0]XXXXXXX to exit VREFDQ calibration mode.
- The following are typical script when applying the above rules for VREFDQ calibration routine when performing VREFDQ calibration in Range 2:
  - MR6[7:6]11 [5:0]XXXXXXX.
  - Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set VREFDQ values and exit VREFDQ calibration mode).
- All subsequent VREFDQ calibration MR setting commands are MR6[7:6]11[5:0]VVVVVV.
- "VVVVVV" are desired settings for VREFDQ.
- Issue ACT/WR/RD looking for pass/fail to determine VCENT (midpoint) as needed.
- To exit VREFDQ calibration, the last two VREFDQ calibration MR commands are:
  - MR6[7:6]11 [5:0]VVVVVV* where VVVVVV* = desired value for VREFDQ.
  - MR6[7]0 [6:0]XXXXXXX to exit VREFDQ calibration mode.

Note:
Range may only be set or changed when entering VREFDQ calibration mode; changing range while in or exiting VREFDQ calibration mode is illegal.

6.1.4.2 VREFDQ Training Mode Entry and Exit Timing Diagram

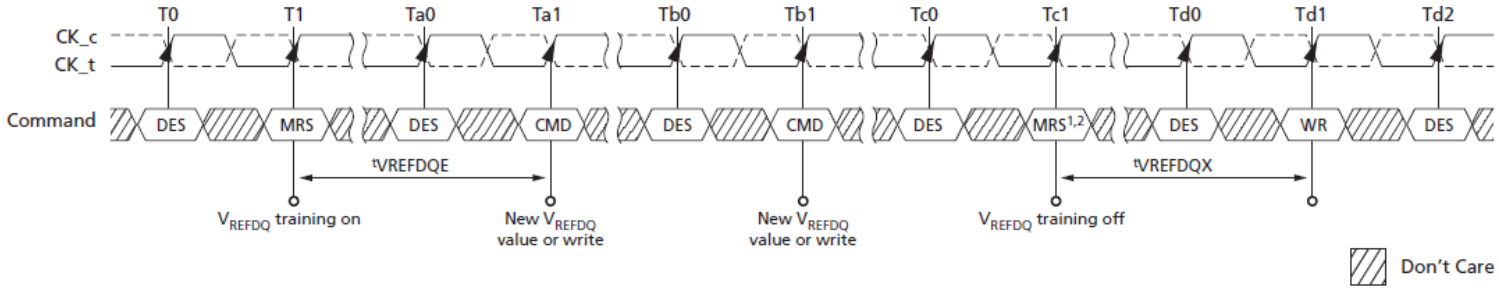


Figure 7. VREFDQ Training Mode Entry and Exit Timing Diagram

Notes:

New VREFDQ values are not allowed with an MRS command during calibration mode entry.

Depending on the step size of the latest programmed VREF value, VREF must be satisfied before disabling VREFDQ training mode.

6.1.4.3 VREF Step: Single Step Size Increment Case

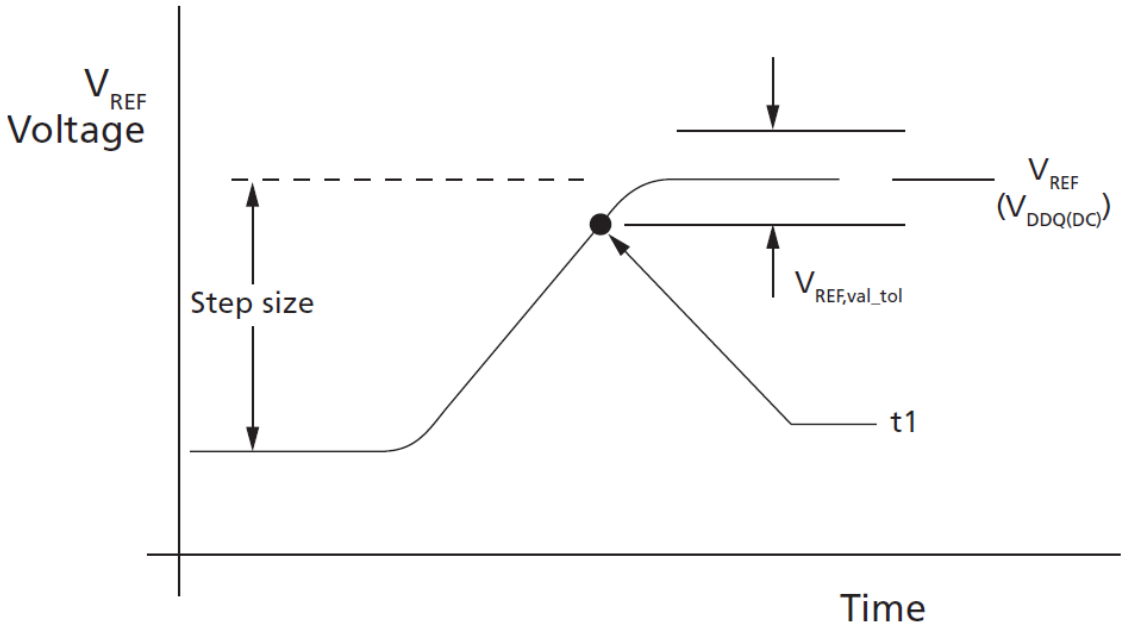


Figure 8. VREF Step: Single Step Size Increment Case

6.1.4.4 VREF Step: Single Step Size Decrement Case

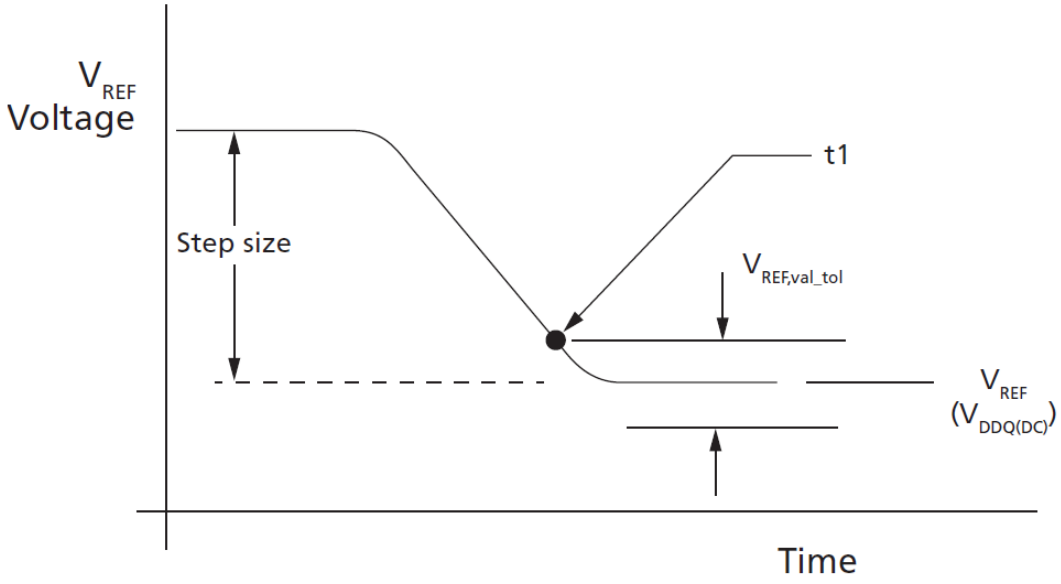


Figure 9. VREF Step: Single Step Size Decrement Case

6.1.4.5 VREF Full Step: From VREF,min to VREF,maxCase

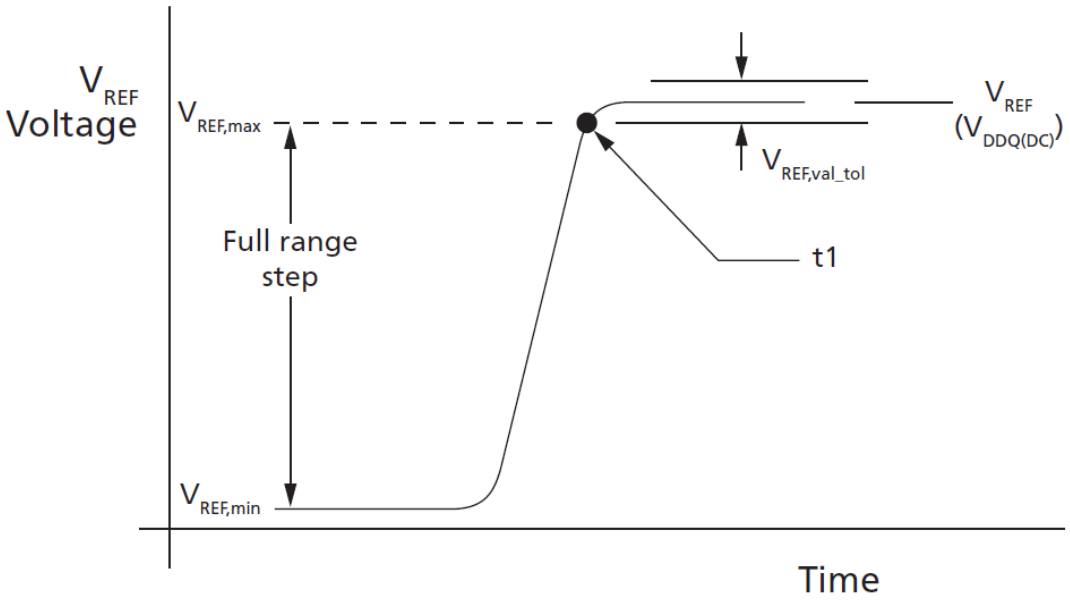


Figure 10. VREF Full Step: From VREF,min to VREF,maxCase

6.1.4.6 VREF Full Step: From VREF,max to VREF,minCase

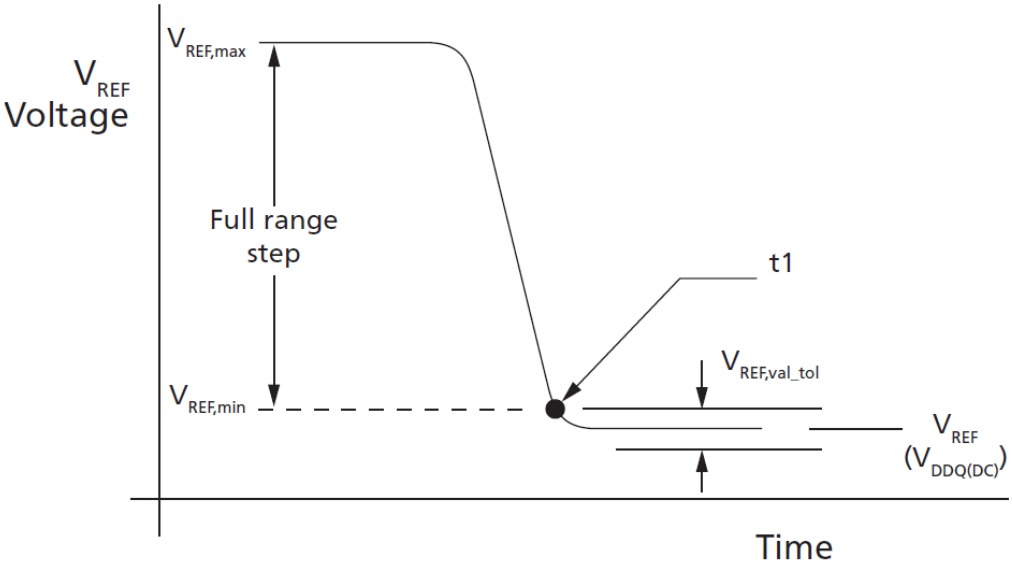


Figure 11. VREF Full Step: From VREF,max to VREF,minCase

6.1.5 VREFDQ Target Settings

The VREFDQ initial settings are largely dependant on the ODT termination settings. The table below shows all of the possible initial settings available for VREFDQ training; it is unlikely the lower ODT settings would be used in most cases.

Table 25: VREFDQ Settings (VDD = 1.2V)

RON	ODT	Vx – VIN LOW (mV)	VREFDQ (mv)	VREFDQ (%VDD)
34 ohm	34 ohm	600	900	75%
	40 ohm	550	875	73%
	48 ohm	500	850	71%
	60 ohm	435	815	68%
	80 ohm	360	780	65%
	120 ohm	265	732	61%
	240 ohm	150	675	56%
48 ohm	34 ohm	700	950	79%
	40 ohm	655	925	77%
	48 ohm	600	900	75%
	60 ohm	535	865	72%
	80 ohm	450	825	69%
	120 ohm	345	770	64%
	240 ohm	200	700	58%

6.1.5.1 VREFDQ Equivalent Circuit

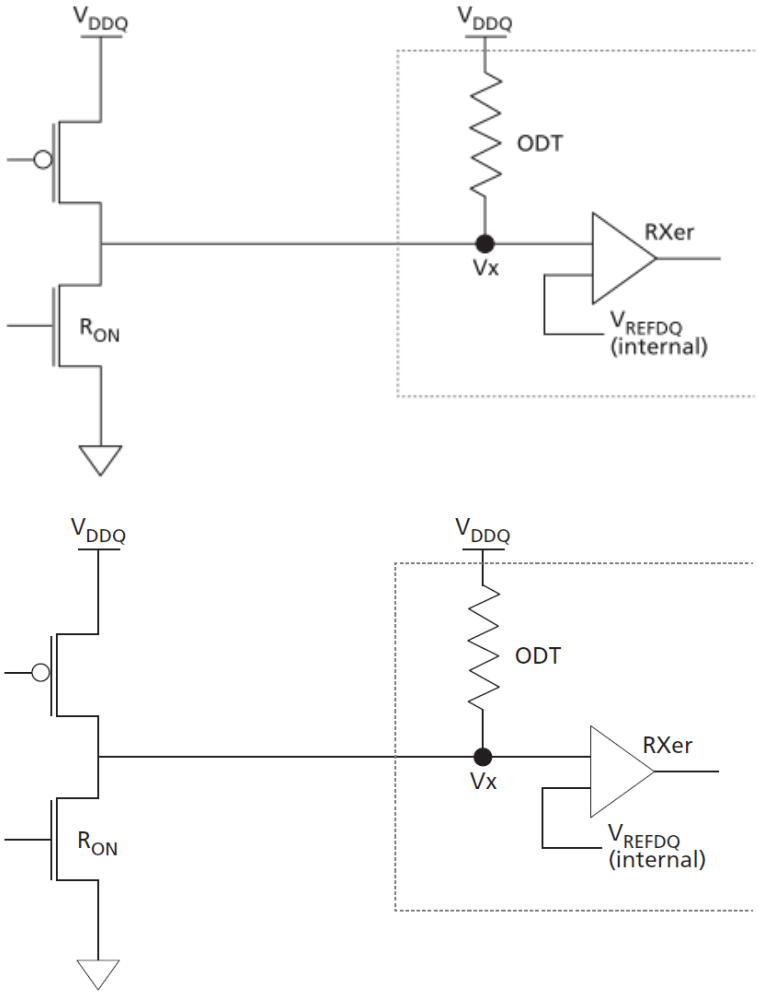


Figure 12. VREFDQ Equivalent Circuit

Notes:

JESD8-24 specifies Vref to be 70% of VDD (VDD=1.2V)

Vref stepsize increment/decrement range. Vref at DC level.

Vref_new = Vref_old+n*Vref_step; n=number of step; if increment use “+”; If decrement use “-”

The minimum value of Vref setting tolerance=Vref_new-1.625%*VDD. The maximum value of Vref setting tolerance=Vref_new+1.625%*VDD. For n>4

The maximum value of Vref setting tolerance=Vref_new-0.15%*VDD. The maximum value of Vref setting tolerance=Vref_new+0.15%*VDD. For n&4 tbd

Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line

Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line

Time from MRS command to increment of decrement one step size for Vref

Time from MRS command to increment of decrement more than one step size up to full range of Vref

Only applicable for MCP component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.

MCP range1 or 2 set by MRS bit MR6,A6.

7 DC OPERATING CONDITIONS AND CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Table 26: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Notes
Voltage on any ball relative to GND	Vin, Vout	-0.3 to 1.5	V	1,
Voltage on VDD supply relative to GND	VDD	-0.3 to 1.5	V	1,3
Voltage on VPP supply relative to GND	VPP	-0.3 to 3.0	V	4
Storage temperature	Tstg	-55 to +150	°C	1,2

Notes:

Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, refer to JESD51- 2 standard.

VDD must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDD, When VDD are less than 500 mV; VREF may be equal to or less than 300 mV

VPP must be equal or greater than VDD at all times

Refer to JEDEC JC451 specification

7.2 MCP Component Operating Temperature Range

Table 27: DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Note
Toper	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3
MCP operating temperature (ambient)	Commercial	0 to 70	°C	
MCP operating temperature (ambient)	Industrial	-40 to 85	°C	
MCP operating temperature (ambient)	Extended	-40 to 105	°C	
MCP operating temperature (ambient)	Military	-55 to 125	°C	

Notes:

Operating Temperature TOPER is the case surface temperature on the center / top side of the MCP. For measurement conditions, refer to the JEDEC document JESD51-2.

The Normal Temperature Range specifies the temperatures where all MCP specifications will be supported.
During operation, the MCP case temperature must be maintained under all operating conditions.

Some applications require operation of the MCP in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range.

7.3 tREFI by Temperature

Table 28: tREFI by Temperature

Parameter	Symbol		8Gb	Units
Average periodic refresh interval	tREFI	0°C ≤ Tcase ≤ 85°C (self/auto refresh)	7.8	µs
		85°C ≤ Tcase ≤ 95°C (see note 1)	3.9	µs
		95°C ≤ Tcase ≤ 105°C (manual refresh)	1.95	µs
		105°C ≤ Tcase ≤ 125°C (manual refresh)	0.4876	µs

Notes

If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range.

8192 cycle refresh is
64ms between 0 to 85°C
32ms between 85 to 95°C
16ms between 95 to 105°C
4ms between 105 to 125°C

7.4 DC OPERATING VOLTAGE

Table 29: DC OPERATING VOLTAGE (POD12)

Symbol	Parameter	Rating			Units	Notes
		Min	Typ	Max		
VDD	Supply Voltage VDD: PC4:1.2V±5%,	1.14	1.2	1.26	v	1,2,3
VPP	2.5V +10%, -5%	2.375	2.5	2.75	v	3

Notes:

JESD8-24 specifies Vref to be 70% of VDD.

DC bandwidth is limited to 20MHz.,

PODI2 1.2V Pseudo Open Drain Interface has a VDD value of 1.2V but the reference voltage allows PODI2 to be used with other VDD values. POD12 signals have pull-up-only parallel input termination and have an asymmetric output drive impedance. For example, if the output drivers were using a 60 ohm pull-up drive impedance then the pull-down drivers would be expected to produce a 40 ohm pull-down drive impedance. PODI2 does not explicitly call for series termination resistors, so it is suitable for point-to-point as well as multi-drop stub environments which may require some additional termination.

7.5 DDR4 power consumption

The DDR4 power consumption during normal operation strongly depends on the usage profile (transfer speed, write and read duty cycles, …). For this reason, it is not possible to provide power key figures fitting all applications. Teledyne e2v provides a power consumption estimation spreadsheet that should be used to estimate the power drawn by the DDR4 on D1_VDD and D1_VPP supplies. This power calculation tool is available upon request.

The maximum D1_VDD current consumed by the DDR4 memory during the initialization is provided in the following table:

Symbol	DDR4-2100	Unit
Iddinit: DDR4 initialization current on D1_VDD (1)	1600	mA
Ippinit: DDR4 initialization current on D1_Vpp (2)	N/S (2)	mA

(1) : Current during initialization of the DDR4 done by the LS1046A DDR4 controller during the boot of Qormino (ex: initialization under U-Boot). Maximum duration: 1s
(2) : The initialization current on D1_VPP is not specified. It is lower or equal than the current drawn in normal operation, which can be estimated with the power consumption estimation spreadsheet.

D1_VTT corresponds to the termination voltage for the Address/Control/Command signals of the DDR4 (to which the integrated termination resistors are connected). The current on this supply can be either positive or negative, meaning that the voltage regulation must have sink and source capability. The maximum current on D1_VTT is reached when all Address/Control/Command signals are in the same state, and it is given in the next table.

VREFCA is not a supply, and it is used as a voltage reference. Its maximum leakage current is also provided in the table.

Supply	Maximum	Unit
D1_VTT	±223	mA
VREFCA 4GB Rev A (Z01A)	±10	µA
VREFCA 4GB / 8GB Rev B (Z11B)	±18	µA

Power supply sizing depends on the memory DDR4 controller. Teledyne e2v can't specify a value and users need to pay attention to this. Some typical power sizing examples are provided in the following table:

Table 30 Typical operating current on VDD depending on memory and DDR4 controller

Memory controller	DDR4	Power supply sizing
LS1046	4GB (Rev A)	1.2 A
	4/8GB (Rev B)	1.6 A
T1040	4GB (Rev A)	1.7 A
	4/8GB (Rev B)	1.9 A

8 AC OPERATING CONDITIONS AND CHARACTERISTICS

8.1 Speed Bins by Speed Grade

Table 31: DDR4-1866 Speed Bins and Operating Conditions

Speed Bin				**DDR4-1866**		**Unit**	**NOTE**
CL-nRCD-nRP				**13-13-13**			
Parameter			**Symbol**	**Min**	**Max**		
Internal read command to first data			tAA	13.92[14] (13.50)[5,12]	18	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	
ACT to internal read or write delay time			tRCD	13.92 (13.50)[5,12]	-	ns	
PRE command period			tRP	13.92 (13.50)[5,12]	-	ns	
ACT to PRE command period			tRAS	34	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,12]	-	ns	
	Normal	Read DBI					
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11 ,14
	CL=10	CL=12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL=9,11	CL=10	CL=12	tCK(AVG)				4
	CL=11	CL=13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional)[5,12]			
	CL=12	CL=14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL=10,12	CL=12	CL=14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL=13	CL=15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL=14	CL=16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				9,11,12,13,14		nCK	13,14
Supported CL Settings with read DBI				11,13,14 ,15,16		nCK	13
Supported CWL Settings				9,10,11,12		nCK	

Table 32: DDR4-2133 Speed Bins and Operating Conditions

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.06[14] (13.75)[5,12]	18	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	
ACT to internal read or write delay time			tRCD	14.06 (13.75)[5,12]	-	ns	
PRE command period			tRP	14.06 (13.75)[5,12]	-	ns	
ACT to PRE command period			tRAS	33	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	47.06 (46.75)[5,12]	-	ns	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11, 14
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)			ns	1,2,3,4,7
			tCK(AVG)	(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
			tCK(AVG)	(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = TBD	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = TBD	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = TBD	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				(9),(11),12,(13),14,15,16		nCK	13,14
Supported CL Settings with read DBI				(11),(13),14,(15),16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

Table 33: DDR4-2400 Speed Bins and Operating Conditions

Speed Bin			DDR4-2400		Unit	NOTE
CL-nRCD-nRP			17-17-17			
Parameter		Symbol	Min	Max		
Internal read command to first data		tAA	14.16[14] (13.75)[5,12]	18	ns	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	
ACT to internal read or write delay time		tRCD	14.16 (13.75)[5,12]	-	ns	
PRE command period		tRP	14.16 (13.75)[5,12]	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	46.16 (45.75)[5,12]	-	ns	
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved	ns	1,2,3,4,11, 14
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)			ns	1,2,3,4,7
			tCK(AVG)	(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
			tCK(AVG)	(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.938	ns	1,2,3
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	ns	1,2,3,4
Supported CL Settings			(10),(11),12,(13),14,15,16,17,18		nCK	13,14
Supported CL Settings with read DBI			(12),(13),14,(15),16,18,19,20,21		nCK	
Supported CWL Settings			9,10,11,12,14,16		nCK	

Table 34: Timing Parameters for Speed Grades 1866 to 2133

Speed		DDR4-1866		DDR4-2133		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	ns	23
Average Clock Period	tCK(avg)	See Speed Bins Table				ps	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	tCK(avg)	24
Absolute clock Low pulse width	tCL(abs)	0.45	-	0.45	-	tCK(avg)	25
Clock Period Jitter-total	JIT(per)_tot	-0.1	0.1	-0.1	0.1	UI	26
Clock Period Jitter-deterministic	JIT(per)_dj					UI	27
Clock Period Jitter during DLL locking period	tJIT(per, lck)					UI	
Cycle to Cycle Period Jitter	tJIT(cc)_tot					UI	26
Cycle to Cycle Period Jitter- deterministic	tJIT(cc)_dj	0.2		0.2		UI	27
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)					UI	
Duty cycle Jitter	tJIT(duty)					UI	
Cumulative error across 2 cycles	tERR(2per)					UI	
Cumulative error across 3 cycles	tERR(3per)					UI	
Cumulative error across 4 cycles	tERR(4per)					UI	
Cumulative error across 5 cycles	tERR(5per)					UI	
Cumulative error across 6 cycles	tERR(6per)					UI	
Cumulative error across 7 cycles	tERR(7per)					UI	
Cumulative error across 8 cycles	tERR(8per)					UI	
Cumulative error across 9 cycles	tERR(9per)					UI	
Cumulative error across 10 cycles	tERR(10per)					UI	
Cumulative error across 11 cycles	tERR(11per)					UI	
Cumulative error across 12 cycles	tERR(12per)					UI	

Speed		DDR4-1866		DDR4-2133		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)					UI	
Command and Address Timing							
CAS_n to CAS_n command delay for same bank group	t_{CCD_L}	5	-	6	-	nCK	
CAS_n to CAS_n command delay for different bank group	t_{CCD_S}	4	-	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/KB page size	tRRD_L(1/2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
Four activate window for 2KB page size	tFAW_2K	30		30		ns	
Four activate window for 1KB page size	tFAW _1K	23		21		ns	
Four activate window for 1KB page size	tFAW _1/2K	17		15		ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	ns	1

Speed		DDR4-1866		DDR4-2133		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
WRITE recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	ns	1,29
Delay from start of internal write transaction to internal read command for different bank groups with both CRC and OM enabled	tWTR_S_ CRC_DM	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	ns	2,30
Delay from start of internal write transaction to internal read command for same bank group with both CRC and OM enabled	tWTR_L_ CRC_DM	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	ns	3,31
DLL locking time	tDLLK					nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	
Multi-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min)	-	tMOD (min)	-		
CS_n to Command Address Latency							
CS_n to Command Address Latency	tCAL	4	-	4	-	nCK	
DRAM Data Timing							
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	tbd	-	tbd	tCK(avg)/2	14,1,9
DQS_t,DQS_c to DQ skew deterministic, per group, per access	tDQSQ	-	tbd	-	tbd	tCK(avg)/2	15,1,7,19
DQ output hold time from DQS_t,DQS_c	tQH		-		-	tCK(avg)/2	14,1,8,19
DQ output hold time deterministic from DQS_t, DQS_c	tQH		-		-	UI	15,1,7,19
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	tbd	-	tbd	UI	14,20
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	UI	14,20
DQ to DQ offset , per group, per access refer-enced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	UI	16, 17
Data Strobe Timing							
DQS_t,DQS_c differential output high time	tQSH	TBD	TBD	TBD	TBD	tCK(avg)/2	22

Speed		DDR4-1866		DDR4-2133		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
DQS_t,DQS_c differential output low time	tQSL	TBD	TBD	TBD	TBD	tCK(avg)/2	21
MPSM Timing							
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-		
Calibration Timing							
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min) + 10ns)	-	max (5nCK,tRFC(min) + 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-		

Speed		DDR4-1866		DDR4-2133		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Power-Down when CA Parity is enabled							
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen t commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		3
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		32,33
Command pass disable delay	tCPDED	4	-	4	-		
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	2	-		7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	2	-		7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Downentry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	2	-	nCK	7,8
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-		
PDA Timing							
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-		

Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD			
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing							
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	13
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	13
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE					ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	Max(2nCK,3ns)	-	Max(2nCK,3ns)		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	56	112	64	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	50	-	57	nCK	
Parity Latency [1715.64, JC42.3C]	PL	4	4	nCK			
CRC Error Reporting							
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	nCK	
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	10
delay from start of internal write transaction to internal	tWTR_S_CRC_DM	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	11

delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled							
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	12
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR					
CKE HIGH Assert Geardown Enable time(T2/CKE)	tXS_GEAR	tXS					
MRS command to Sync pulse time(T3)	tSYNC_GEAR	tMOD(min)+4nCK					28
Sync pulse to First valid command(T4)	tCMD_GEAR						28
Geardown setup time	tGEAR_setup					nCK	
Geardown hold time	tGEAR_hold					nCK	
tREFI							
tRFC1 (min)	2Gb	160	-	160	-	ns	
	4Gb	260	-	260	-	ns	
	8Gb	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	ns	
tRFC2 (min)	2Gb	110	-	110	-	ns	
	4Gb	160	-	160	-	ns	
	8Gb	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	ns	
tRFC4 (min	2Gb	90	-	90	-	ns	
	4Gb	110	-	110	-	ns	
	8Gb	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Table 35: Timing Parameters for Speed Grades 2400

Speed		**DDR4-2400**		**Units**	**Note**
Parameter	**Symbol**	**MIN**	**MAX**		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns	23
Average Clock Period	tCK(avg)	See Speed Bins Table		ps	
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)	

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)	24
Absolute clock Low pulse width	tCL(abs)	0.45	-	tCK(avg)	25
Clock Period Jitter- total	JIT(per)_tot	-42	42	UI	26
Clock Period Jitter- deterministic	JIT(per)_dj	tbd		UI	27
Clock Period Jitter during DLL locking period	tJIT(per, lck)	tbd		UI	
Cycle to Cycle Period Jitter	tJIT(cc)_tot	83		UI	26
Cycle to Cycle Period Jitter- deterministic	tJIT(cc)_dj	tbd		UI	27
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	tbd		UI	
Duty cycle Jitter	tJIT(duty)	tbd		UI	
Cumulative error across 2 cycles	tERR(2per)	tbd		UI	
Cumulative error across 3 cycles	tERR(3per)	tbd		UI	
Cumulative error across 4 cycles	tERR(4per)	tbd		UI	
Cumulative error across 5 cycles	tERR(5per)	tbd		UI	
Cumulative error across 6 cycles	tERR(6per)	tbd		UI	
Cumulative error across 7 cycles	tERR(7per)	tbd		UI	
Cumulative error across 8 cycles	tERR(8per)	tbd		UI	
Cumulative error across 9 cycles	tERR(9per)	tbd		UI	
Cumulative error across 10 cycles	tERR(10per)	tbd		UI	
Cumulative error across 11 cycles	tERR(11per)	tbd		UI	
Cumulative error across 12 cycles	tERR(12per)	tbd		UI	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tbd		UI	
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	6	-	nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK,3.3ns)	-	nCK	

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/KB page size	tRRD_L(1/2K)	Max(4nCK,4.9ns)	-	nCK	
Four activate window for 2KB page size	tFAW_2K	30		ns	
Four activate window for 1KB page size	tFAW _1K	21		ns	
Four activate window for 1KB page size	tFAW _1/2K	13		ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	ns	1
WRITE recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(5nCK,3.75ns)	-	ns	1,29
Delay from start of internal write transaction to internal read command for different bank groups with both CRC and OM enabled	tWTR_S_ CRC_DM	tWTR_S+max(5nCK,3.75ns)	-	ns	2,30
Delay from start of internal write transaction to internal read command for same bank group with both CRC and OM enabled	tWTR_L_ CRC_DM	tWTR_L+max(5nCK,3.75ns)	-	ns	3,31
DLL locking time	tDLLK	TBD		nCK	
Mode Register Set command cycle time	tMRD	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	
Multi-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-		

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
CS_n to Command Address Latency					
CS_n to Command Address Latency	tCAL	5	-	nCK	
DRAM Data Timing					
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	tbd	tCK(avg)/2	14,1,9
DQS_t,DQS_c to DQ skew deterministic, per group, per access	tDQSQ	-	tbd	tCK(avg)/2	15,1,7,19
DQ output hold time from DQS_t,DQS_c	tQH	tbd	-	tCK(avg)/2	14,1,8,19
DQ output hold time deterministic from DQS_t, DQS_c	tQH	tbd	-	UI	15,1,7,19
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	tbd	UI	14,20
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	UI	14,20
DQ to DQ offset , per group, per access refer-enced to DQS_t, DQS_c	tDQSQ	TBD	TBD	UI	16, 17
Data Strobe Timing					
DQS_t,DQS_c differential output high time	tQSH	TBD	TBD	tCK(avg)/2	22
DQS_t,DQS_c differential output low time	tQSL	TBD	TBD	tCK(avg)/2	21
MPSM Timing					
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-		
Calibration Timing					
Power-up and RESET calibration time	tZQinit	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	nCK	

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min) + 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-		
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen t commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-		3
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-		32,33
Command pass disable delay	tCPDED	4	-		
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	2	-		7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-		7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK	5

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
Timing of WR command to Power Downentry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK	7,8
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-		
PDA Timing					
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD			
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	ns	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timing					
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	13
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	13
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	ns	
Write leveling output error	tWLOE			ns	
CA Parity Timing					
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	Max(2nCK,3ns)		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	$t_{PAR\_ALERT\_PW}$	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	64	nCK	

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
Parity Latency [1715.64, JC42.3C]	PL	5		nCK	
CRC Error Reporting					
CRC error to ALERT_n latency	t_{CRC_ALERT}	-	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	nCK	
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR+max} (5nCK,3.75ns)	-	ns	10
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_C\ RC\_DM}$	t_{WTR_S+max} (5nCK,3.75ns)	-	ns	11
delay from start of internal write transaction to internal delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_C\ RC\_DM}$	t_{WTR_L+max} (5nCK,3.75ns)	-	ns	12
Geardown timing					
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	tXPR			
CKE HIGH Assert Geardown Enable time(T2/CKE)	t_{XS_GEAR}	tXS			
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	tMOD(min)+4nCK			28
Sync pulse to First valid command(T4)	t_{CMD_GEAR}				28
Geardown setup time	t_{GEAR_setup}			nCK	
Geardown hold time	t_{GEAR_hold}			nCK	
tREFI					
tRFC1 (min)	2Gb	160	-	ns	
	4Gb	260	-	ns	
	8Gb	350	-	ns	
	16Gb	TBD by JEDEC board spec)	-	ns	
tRFC2 (min)	2Gb	110	-	ns	
	4Gb	160	-	ns	
	8Gb	260	-	ns	
	16Gb	TBD by JEDEC board spec)	-	ns	
tRFC4 (min	2Gb	90	-	ns	
	4Gb	110	-	ns	
	8Gb	160	-	ns	

Speed		DDR4-2400		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**		
	16Gb	TBD by JEDEC board spec)	-	ns	

Notes:

Start of internal write transaction is defined as follows:
For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled

Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} to the next integer.

WR in clock cycles as programmed in MR0.

tREFI depends on TOPER.

CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See 0.1.3 “Power- Down clarifications - Case 2” in RB11112 . — DQ Receiver(Rx) compliance mask

For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.

When CRC and DM are both enabled $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.

When CRC and DM are both enabled $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.

The max values are system dependent.

DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.

The deterministic component of the total timing. Measurement method tbd.

DQ to DQ static offset relative to strobe per group. Measurement method tbd.

This parameter will be characterized and guaranteed by design.

When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output) Deratings are relative to the SDRAM input clock). Example tbd.

DRAM DBI mode is off.

DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge

Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.

The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.

This parameter has to be even number of clocks

When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.

When CRC and DM are both enabled $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.

When CRC and DM are both enabled $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.

After CKE is registered LOW, CKE signal level shall be maintained below VILDC for t_{CKE} specification (Low pulse width).

After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for t_{CKE} specification (HIGH pulse width).
UI=tCK(avg).min/2

Appendix A

The table below maps MCP signals to JEDEC DDR4 288 Pin UDIMM & 260 Pin SO-DIMM. The Table provides a cross reference between standard JEDEC signals and or Embedded Processor / Memory Controller and MCP sorted by functional groups. 4GB part is configured for x16 & 8GB part is configured for x8

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
J11	DQ0	DataByte 0	5	DQ0	8	DQ0
H11	DQ1		150	DQ1	7	DQ1
G9	DQ2		12	DQ2	20	DQ2
F9	DQ3		157	DQ3	21	DQ3
H7	DQ4		3	DQ4	4	DQ4
H9	DQ5		148	DQ5	3	DQ5
J7	DQ6		10	DQ6	16	DQ6
G7	DQ7		155	DQ7	17	DQ7
G12	DQS0_t		153	DQS0_t	13	DQS0_t
F12	DQS0_c		152	DQS0_c	11	DQS0_c
G11	DM0_n		7	DM0_n, DBI0_n, NC	12	DM0_n, DBI0_n, NC
G15	DQ8	DataByte 1	16	DQ8	28	DQ8
E16	DQ9		161	DQ9	29	DQ9
F15	DQ10		23	DQ10	41	DQ10
H15	DQ11		168	DQ11	42	DQ11
F13	DQ12		14	DQ12	24	DQ12
G13	DQ13		159	DQ13	25	DQ13
H13	DQ14		21	DQ14	38	DQ14
E13	DQ15		166	DQ15	37	DQ15
F17	DQS1_t		164	DQS1_t	34	DQS1_t
G17	DQS1_c		163	DQS1_c	32	DQS1_c
H16	DM1_n		18	DM1_n, DBI1_n, NC	33	DM1_n, DBI1_n, NC
B15	DQ16	DataByte 2	27	DQ16	50	DQ16

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
A16	DQ17		172	DQ17	49	DQ17
C15	DQ18		34	DQ18	62	DQ18
A15	DQ19		179	DQ19	63	DQ19
B13	DQ20		25	DQ20	46	DQ20
C14	DQ21		170	DQ21	45	DQ21
A13	DQ22		32	DQ22	58	DQ22
C13	DQ23		177	DQ23	59	DQ23
C17	DQS2_t		175	DQS2_t	55	DQS2_t
B17	DQS2_c		174	DQS2_c	53	DQS2_c
D16	DM2_n		29	DM2_n, DBI2_n, NC	54	DM2_n, DBI2_n, NC
D9	DQ24	DataByte 3	38	DQ24	70	DQ24
A11	DQ25		183	DQ25	71	DQ25
C11	DQ26		45	DQ26	83	DQ26
B11	DQ27		190	DQ27	84	DQ27
B7	DQ28		36	DQ28	66	DQ28
B9	DQ29		181	DQ29	67	DQ29
A7	DQ30		43	DQ30	79	DQ30
C9	DQ31		188	DQ31	80	DQ31
C12	DQS3_t		186	DQS3_t	76	DQS3_t
D12	DQS3_c		185	DQS3_c	74	DQS3_c
D11	DM3_n		40	DM3_n, DBI3_n, NC	75	DM3_n, DBI3_n, NC
AA9	DQ32	DataByte 4	97	DQ32	174	DQ32
AB11	DQ33		242	DQ33	173	DQ33
Y11	DQ34		104	DQ34	187	DQ34
AC11	DQ35		249	DQ35	186	DQ35
AC7	DQ36		95	DQ36	170	DQ36
AB9	DQ37		240	DQ37	169	DQ37

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
AB7	DQ38		102	DQ38	183	DQ38
Y9	DQ39		247	DQ39	182	DQ39
AA12	DQS4_t		245	DQS4_t	179	DQS4_t
Y12	DQS4_c		244	DQS4_c	177	DQS4_c
AA11	DM4_n		99	DM4_n, DB14_N, NC	178	DM4_n, DB14_N, NC
AB15	DQ40	DataByte 5	108	DQ40	195	DQ40
AC16	DQ41		253	DQ41	194	DQ41
AA15	DQ42		115	DQ42	207	DQ42
AC15	DQ43		260	DQ43	208	DQ43
AC13	DQ44		106	DQ44	191	DQ44
AA14	DQ45		251	DQ45	190	DQ45
AB13	DQ46		113	DQ46	203	DQ46
AA13	DQ47		258	DQ47	204	DQ47
AA17	DQS5_t		256	DQS5_t	200	DQS5_t
AB17	DQS5_c		255	DQS5_c	198	DQS5_c
Y16	DM5_n		110	DM5_n, DB15_n, NC	199	DM5_n, DB15_n, NC
U15	DQ48	DataByte 6	119	DQ48	216	DQ48
W16	DQ49		264	DQ49	215	DQ49
V15	DQ50		126	DQ50	228	DQ50
T15	DQ51		271	DQ51	229	DQ51
U11	DQ52		117	DQ52	211	DQ52
U12	DQ53		262	DQ53	212	DQ53
T13	DQ54		124	DQ54	224	DQ54
U13	DQ55		269	DQ55	225	DQ55
V17	DQS6_t		267	DQS6_t	221	DQS6_t
U17	DQS6_c		266	DQS6_c	219	DQS6_c
T16	DM6_n		121	DM6_n, DB16_n, NC	220	DM6_n, DB16_n, NC

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
V9	DQ56	DataByte 7	130	DQ56	237	DQ56
T11	DQ57		275	DQ57	236	DQ57
U9	DQ58		137	DQ58	249	DQ58
R11	DQ59		282	DQ59	250	DQ59
T7	DQ60		128	DQ60	232	DQ60
T9	DQ61		273	DQ61	233	DQ61
R7	DQ62		135	DQ62	245	DQ62
U7	DQ63		280	DQ63	246	DQ63
V13	DQS7_t		278	DQS7_t	242	DQS7_t
W13	DQS7_c		277	DQS7_c	240	DQS7_c
V12	DM7_n		132	DM7_n, DB17_n, NC	241	DM7_n, DB17_n, NC
K16	CB0	ECC Byte	49	CB0, NC	92	CB0, NC
J16	CB1		194	CB1, NC	91	CB1, NC
K14	CB2		56	CB2, NC	101	CB2, NC
K11	CB3		201	CB3, NC	105	CB3, NC
K13	CB4		47	CB4, NC	88	CB4, NC
J14	CB5		192	CB5, NC	87	CB5, NC
K9	CB6		54	CB6, NC	100	CB6, NC
J13	CB7		199	CB7, NC	104	CB7, NC
J17	DQS8_t		197	DQS8_t	97	DQS8_t
K17	DQS8_c		196	DQS8_c	95	DQS8_c
J15	DM8_n		51	DM8_n, DBI8_n, NC	96	DM8_n, DBI8_n, NC
M15	CK0_t	Clock	74	CK0_t	137	CK0_t
M14	CK0_c		75	CK0_c	139	CK0_c
N13	CKE0		60	CKE0	109	CKE0
N4	A0	Address	79	A0	144	A0
M4	A1		72	A1	133	A1

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
N2	A2		216	A2	132	A2
N6	A3		71	A3	131	A3
M6	A4		214	A4	128	A4
N5	A5		213	A5	126	A5
L4	A6		69	A6	127	A6
M3	A7		211	A7	122	A7
N3	A8		68	A8	125	A8
L2	A9		66	A9	121	A9
N9	A10/AP		225	A10/AP	146	A10/AP
M1	A11		210	A11	120	A11
L9	A12		65	A12/BC_n	119	A12
L1	A13		232	A13	158	A13
L12	A14/WE_n		228	WE_n/A14	151	A14/WE_n
N12	A15/CAS_n		86	CAS_n/A15	156	A15/CAS_n
M12	A16/RAS_n		82	RAS_n/A16	152	A16/RAS_n
N7	BA0	Bank Group	81	BA0	150	BA0
L6	BA1		224	BA1	145	BA1
L7	BG0		63	BG0	115	BG0
N11	BG1	Connect to Processor / Memory Controller for future migration from 4GB to 8GB MCP	207	BG1	113	BG1
L13	CS0_n		84	CS0_n	149	CS0_n
L11	ACT_n	Miscellaneous	62	ACT_n	114	ACT_n
L3	ALERT_n		208	ALERT_n	116	ALERT_n
M13	ODT0		87	ODT0	155	ODT0
N1	PARITY		222	PARITY	143	PARITY
M5	RESET_n		58	RESET_n	108	RESET_n
A2	GND	Ground / VSS	2	VSS	1	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
A4	GND		4	VSS	2	VSS
A6	GND		6	VSS	5	VSS
A8	GND		9	VSS	6	VSS
A10	GND		11	VSS	9	VSS
A12	GND		13	VSS	10	VSS
A14	GND		15	VSS	14	VSS
A17	GND		17	VSS	15	VSS
AA5	GND		259	VSS	230	VSS
AA8	GND		261	VSS	231	VSS
AA16	GND		263	VSS	234	VSS
AB1	GND		265	VSS	235	VSS
AB3	GND		268	VSS	238	VSS
AB8	GND		270	VSS	239	VSS
AB10	GND		272	VSS	243	VSS
AB14	GND		274	VSS	244	VSS
AC2	GND		276	VSS	247	VSS
AC4	GND		279	VSS	248	VSS
AC6	GND		281	VSS	251	VSS
AC8	GND		283	VSS	252	VSS
AC10	GND		20	VSS	18	VSS
AC12	GND		22	VSS	19	VSS
AC14	GND		24	VSS	22	VSS
AC17	GND		26	VSS	23	VSS
B1	GND		28	VSS	26	VSS
B3	GND		31	VSS	27	VSS
B8	GND		33	VSS	30	VSS
B10	GND		35	VSS	31	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
B14	GND		37	VSS	35	VSS
C5	GND		39	VSS	36	VSS
C8	GND		42	VSS	39	VSS
C16	GND		44	VSS	40	VSS
D6	GND		46	VSS	43	VSS
D14	GND		48	VSS	44	VSS
D17	GND		50	VSS	47	VSS
E3	GND		53	VSS	48	VSS
E7	GND		55	VSS	51	VSS
E8	GND		57	VSS	52	VSS
E10	GND		94	VSS	56	VSS
E12	GND		96	VSS	57	VSS
E15	GND		98	VSS	60	VSS
F5	GND		101	VSS	61	VSS
F11	GND		103	VSS	64	VSS
F14	GND		105	VSS	65	VSS
F16	GND		107	VSS	68	VSS
G5	GND		109	VSS	69	VSS
H1	GND		112	VSS	72	VSS
H3	GND		114	VSS	73	VSS
H6	GND		116	VSS	77	VSS
H8	GND		118	VSS	78	VSS
H14	GND		120	VSS	81	VSS
H17	GND		123	VSS	82	VSS
J2	GND		125	VSS	85	VSS
J4	GND		127	VSS	86	VSS
J9	GND		129	VSS	89	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
J12	GND		131	VSS	90	VSS
K2	GND		134	VSS	93	VSS
K3	GND		136	VSS	94	VSS
K5	GND		138	VSS	98	VSS
K7	GND		147	VSS	99	VSS
K12	GND		149	VSS	102	VSS
K15	GND		151	VSS	103	VSS
L15	GND		154	VSS	106	VSS
M2	GND		156	VSS	107	VSS
M7	GND		158	VSS	167	VSS
M11	GND		160	VSS	168	VSS
M16	GND		162	VSS	171	VSS
N15	GND		165	VSS	172	VSS
P2	GND		167	VSS	175	VSS
P3	GND		169	VSS	176	VSS
P5	GND		171	VSS	180	VSS
P7	GND		173	VSS	181	VSS
P12	GND		176	VSS	184	VSS
P15	GND		178	VSS	185	VSS
R2	GND		180	VSS	188	VSS
R4	GND		182	VSS	189	VSS
R9	GND		184	VSS	192	VSS
R12	GND		187	VSS	193	VSS
T1	GND		189	VSS	196	VSS
T3	GND		191	VSS	197	VSS
T6	GND		193	VSS	201	VSS
T8	GND		195	VSS	202	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Function						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
T14	GND		198	VSS	205	VSS
T17	GND		200	VSS	206	VSS
U5	GND		202	VSS	209	VSS
V5	GND		239	VSS	210	VSS
V11	GND		241	VSS	213	VSS
V14	GND		243	VSS	214	VSS
V16	GND		246	VSS	217	VSS
W3	GND		248	VSS	218	VSS
W7	GND		250	VSS	222	VSS
W8	GND		252	VSS	223	VSS
W10	GND		254	VSS	226	VSS
W12	GND		257	VSS	227	VSS
W15	GND					
Y6	GND					
Y14	GND					
Y17	GND					
M9	VREFCA		146	VREFCA	164	VREFCA
A3	VDD		59	VDD	135	VDD
A5	VDD		61	VDD	136	VDD
A9	VDD		64	VDD	130	VDD
AB5	VDD		67	VDD	154	VDD
AB12	VDD		70	VDD	141	VDD
AB16	VDD		73	VDD	142	VDD
AC3	VDD		76	VDD	147	VDD
AC5	VDD		80	VDD	159	VDD
AC9	VDD		83	VDD	148	VDD
B5	VDD		85	VDD	153	VDD

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
B12	VDD		88	VDD	160	VDD
B16	VDD		90	VDD	163	VDD
D8	VDD		92	VDD	111	VDD
D15	VDD		204	VDD	112	VDD
E9	VDD		206	VDD	117	VDD
E11	VDD		209	VDD	123	VDD
E14	VDD		212	VDD	124	VDD
F8	VDD		215	VDD	118	VDD
G8	VDD		217	VDD	129	VDD
G14	VDD		220	VDD		
G16	VDD		223	VDD		
H2	VDD		226	VDD		
H4	VDD		229	VDD		
H5	VDD		231	VDD		
H12	VDD		233	VDD		
J3	VDD		236	VDD		
J5	VDD					
J6	VDD					
K1	VDD					
K4	VDD					
K6	VDD					
L14	VDD					
L16	VDD					
N14	VDD					
N16	VDD					
P1	VDD					
P4	VDD					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
P6	VDD					
R3	VDD					
R5	VDD					
R6	VDD					
T2	VDD					
T4	VDD					
T5	VDD					
T12	VDD					
U8	VDD					
U14	VDD					
U16	VDD					
V8	VDD					
W9	VDD					
W11	VDD					
W14	VDD					
Y8	VDD					
Y15	VDD					
A1	VPP		143	VPP	257	VPP
E17	VPP		286	VPP	259	VPP
AC1	VPP		287	VPP		
W17	VPP		288	VPP		
			142	VPP		
L17	VTT		221	VTT	258	VTT
J1	VTT		77	VTT		
M17	VTT					
N17	VTT					
R1	VTT					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
G10	ZQ0	Calibration Reference - Connect to GND via 240Ω 1% Resistor				
F10	ZQ1					
C10	ZQ2					
D10	ZQ3					
AA10	ZQ4					
Y10	ZQ5					
U10	ZQ6					
V10	ZQ7					
H10	ZQ8					
L5	TEN	Active High signal. Must be Low during normal operation				
AA1	NC	No Connect				
AA2	NC					
AA3	NC					
AA4	NC					
AA6	NC					
AA7	NC					
AB2	NC					
AB4	NC					
AB6	NC					
B2	NC					
B4	NC					
B6	NC					
C1	NC					
C2	NC					
C3	NC					
C4	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
C6	NC					
C7	NC					
D1	NC					
D2	NC					
D3	NC					
D4	NC					
D5	NC					
D7	NC					
D13	NC					
E1	NC					
E2	NC					
E4	NC					
E5	NC					
E6	NC					
F1	NC					
F2	NC					
F3	NC					
F4	NC					
F6	NC					
F7	NC					
G1	NC					
G2	NC					
G3	NC					
G4	NC					
G6	NC					
J8	NC					
J10	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
K8	NC					
K10	NC					
L8	NC					
L10	NC					
M8	NC					
M10	NC					
N8	NC					
N10	NC					
P8	NC					
P9	NC					
P10	NC					
P11	NC					
P13	NC					
P14	NC					
P16	NC					
P17	NC					
R8	NC					
R10	NC					
R13	NC					
R14	NC					
R15	NC					
R16	NC					
R17	NC					
T10	NC					
U1	NC					
U2	NC					
U3	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
U4	NC					
U6	NC					
V1	NC					
V2	NC					
V3	NC					
V4	NC					
V6	NC					
V7	NC					
W1	NC					
W2	NC					
W4	NC					
W5	NC					
W6	NC					
Y1	NC					
Y2	NC					
Y3	NC					
Y4	NC					
Y5	NC					
Y7	NC					
Y13	NC					
		Signals for External	139	SA0	256	SA0
		SPD EEPROM to interface	140	SA1	260	SA1
		to Host Processor /	238	SA2	166	SA2
		Memory Controller	141	SCL	253	SCL
		if used or NC	285	SDA	254	SDA
			284	VDDSPD	255	VDDSPD
		Not Required - NC	219	CK1_c	140	CK1_c

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Function

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
			218	CK1_t	138	CK1_t
			203	CKE1	110	CKE1
			78	EVENT_n	134	EVENT_n
			91	ODT1	161	ODT1
			89	CS1_n	157	CS1_n
			93	CS2_n C[0]	162	C0, CS2_n, NC
			237	CS3_n C[1]	165	C1, CS3_N, NC
			234	A17 NC		
			235	C[2] NC		
			1	12V NC		
			145	12V NC		
		Reserved - NC	144	RFU		
			205	RFU		
			227	RFU		
		No Connect	19	NC		
			30	NC		
			41	NC		
			100	NC		
			111	NC		
			122	NC		
			133	NC		
			52	NC		
			8	NC		
			230	NC		

Appendix B

The table below maps MCP signals to JEDEC DDR4 288 Pin UDIMM & 260 Pin SO-DIMM 4GB (x16) Single Channel x 72. The Table provides a cross reference between standard JEDEC signals and or Embedded Processor / Memory Controller and MCP sorted by MCP Ballout designation. 4GB part is configured for x16 & 8GB part is configured for x8

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
A1	VPP		143	VPP	257	VPP
A2	GND		2	VSS	1	VSS
A3	VDD		59	VDD	135	VDD
A4	GND		4	VSS	2	VSS
A5	VDD		61	VDD	136	VDD
A6	GND		6	VSS	5	VSS
A7	DQ30		43	DQ30	79	DQ30
A8	GND		9	VSS	6	VSS
A9	VDD		64	VDD	130	VDD
A10	GND		11	VSS	9	VSS
A11	DQ25		183	DQ25	71	DQ25
A12	GND	Ground / VSS	13	VSS	10	VSS
A13	DQ22		32	DQ22	58	DQ22
A14	GND		15	VSS	14	VSS
A15	DQ19		179	DQ19	63	DQ19
A16	DQ17		172	DQ17	49	DQ17
A17	GND		17	VSS	15	VSS
B1	GND		20	VSS	18	VSS
B2	NC					
B3	GND		22	VSS	19	VSS
B4	NC					
B5	VDD		67	VDD	154	VDD
B6	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
B7	DQ28		36	DQ28	66	DQ28
B8	GND		24	VSS	22	VSS
B9	DQ29		181	DQ29	67	DQ29
B10	GND		26	VSS	23	VSS
B11	DQ27		190	DQ27	84	DQ27
B12	VDD		70	VDD	141	VDD
B13	DQ20		25	DQ20	46	DQ20
B14	GND		28	VSS	26	VSS
B15	DQ16	DataByte 2	27	DQ16	50	DQ16
B16	VDD		73	VDD	142	VDD
B17	DQS2_c		174	DQS2_c	53	DQS2_c
C1	NC					
C2	NC					
C3	NC					
C4	NC					
C5	GND		31	VSS	27	VSS
C6	NC					
C7	NC					
C8	GND		33	VSS	30	VSS
C9	DQ31		188	DQ31	80	DQ31
C10	ZQ2	Calibration Reference				
C11	DQ26		45	DQ26	83	DQ26
C12	DQS3_t		186	DQS3_t	76	DQS3_t
C13	DQ23		177	DQ23	59	DQ23
C14	DQ21		170	DQ21	45	DQ21
C15	DQ18		34	DQ18	62	DQ18
C16	GND		35	VSS	31	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Ballout

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
C17	DQS2_t		175	DQS2_t	55	DQS2_t
D1	NC					
D2	NC					
D3	NC					
D4	NC					
D5	NC					
D6	GND		37	VSS	35	VSS
D7	NC					
D8	VDD		76	VDD	147	VDD
D9	DQ24	DataByte 3	38	DQ24	70	DQ24
D10	ZQ3	Calibration Reference				
D11	DM3_n		40	DM3_n, DBI3_n, NC	75	DM3_n, DBI3_n, NC
D12	DQS3_c		185	DQS3_c	74	DQS3_c
D13	NC					
D14	GND		39	VSS	36	VSS
D15	VDD		80	VDD	159	VDD
D16	DM2_n		29	DM2_n, DBI2_n, NC	54	DM2_n, DBI2_n, NC
D17	GND		42	VSS	39	VSS
E1	NC					
E2	NC					
E3	GND		44	VSS	40	VSS
E4	NC					
E5	NC					
E6	NC					
E7	GND		46	VSS	43	VSS
E8	GND		48	VSS	44	VSS
E9	VDD		83	VDD	148	VDD

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
E10	GND		50	VSS	47	VSS
E11	VDD		85	VDD	153	VDD
E12	GND		53	VSS	48	VSS
E13	DQ15		166	DQ15	37	DQ15
E14	VDD		88	VDD	160	VDD
E15	GND		55	VSS	51	VSS
E16	DQ9		161	DQ9	29	DQ9
E17	VPP		286	VPP	259	VPP
F1	NC					
F2	NC					
F3	NC					
F4	NC					
F5	GND		57	VSS	52	VSS
F6	NC					
F7	NC					
F8	VDD		90	VDD	163	VDD
F9	DQ3		157	DQ3	21	DQ3
F10	ZQ1	Calibration Reference				
F11	GND		94	VSS	56	VSS
F12	DQS0_c		152	DQS0_c	11	DQS0_c
F13	DQ12		14	DQ12	24	DQ12
F14	GND		96	VSS	57	VSS
F15	DQ10		23	DQ10	41	DQ10
F16	GND		98	VSS	60	VSS
F17	DQS1_t		164	DQS1_t	34	DQS1_t
G1	NC					
G2	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
G3	NC					
G4	NC					
G5	GND		101	VSS	61	VSS
G6	NC					
G7	DQ7		155	DQ7	17	DQ7
G8	VDD		92	VDD		
G9	DQ2		12	DQ2	20	DQ2
G10	ZQ0	Calibration Reference				
G11	DM0_n		7	DM0_n, DBI0_n, NC	12	DM0_n, DBI0_n, NC
G12	DQS0_t		153	DQS0_t	13	DQS0_t
G13	DQ13		159	DQ13	25	DQ13
G14	VDD		204	VDD		
G15	DQ8	DataByte 1	16	DQ8	28	DQ8
G16	VDD		206	VDD		
G17	DQS1_c		163	DQS1_c	32	DQS1_c
H1	GND		103	VSS	64	VSS
H2	VDD		209	VDD		
H3	GND		105	VSS	65	VSS
H4	VDD		212	VDD		
H5	VDD		215	VDD		
H6	GND		107	VSS	68	VSS
H7	DQ4		3	DQ4	4	DQ4
H8	GND		109	VSS	69	VSS
H9	DQ5		148	DQ5	3	DQ5
H10	ZQ8	Calibration Reference				
H11	DQ1		150	DQ1	7	DQ1
H12	VDD		217	VDD		

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
H13	DQ14		21	DQ14	38	DQ14
H14	GND		112	VSS	72	VSS
H15	DQ11		168	DQ11	42	DQ11
H16	DM1_n		18	DM1_n, DBI1_n, NC	33	DM1_n, DBI1_n, NC
H17	GND		114	VSS	73	VSS
J1	VTT		77	VTT		
J2	GND		116	VSS	77	VSS
J3	VDD		220	VDD	111	VDD
J4	GND		118	VSS	78	VSS
J5	VDD		223	VDD	112	VDD
J6	VDD		226	VDD	117	VDD
J7	DQ6		10	DQ6	16	DQ6
J8	NC					
J9	GND		120	VSS	81	VSS
J10	NC					
J11	DQ0	DataByte 0	5	DQ0	8	DQ0
J12	GND		123	VSS	82	VSS
J13	CB7		199	CB7, NC	104	CB7, NC
J14	CB5		192	CB5, NC	87	CB5, NC
J15	DM8_n		51	DM8_n, DBI8_n, NC	96	DM8_n, DBI8_n, NC
J16	CB1		194	CB1, NC	91	CB1, NC
J17	DQS8_t		197	DQS8_t	97	DQS8_t
K1	VDD		229	VDD	123	VDD
K2	GND		125	VSS	85	VSS
K3	GND		127	VSS	86	VSS
K4	VDD					
K5	GND		129	VSS	89	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
K6	VDD					
K7	GND		131	VSS	90	VSS
K8	NC					
K9	CB6		54	CB6, NC	100	CB6, NC
K10	NC					
K11	CB3		201	CB3, NC	105	CB3, NC
K12	GND		134	VSS	93	VSS
K13	CB4		47	CB4, NC	88	CB4, NC
K14	CB2		56	CB2, NC	101	CB2, NC
K15	GND		136	VSS	94	VSS
K16	CB0	ECC Byte	49	CB0, NC	92	CB0, NC
K17	DQS8_c		196	DQS8_c	95	DQS8_c
L1	A13		232	A13	158	A13
L2	A9		66	A9	121	A9
L3	ALERT_n		208	ALERT_n	116	ALERT_n
L4	A6		69	A6	127	A6
L5	TEN	Active High signal. Must be Low during normal operation				
L6	BA1		224	BA1	145	BA1
L7	BG0		63	BG0	115	BG0
L8	NC					
L9	A12		65	A12/BC_n	119	A12
L10	NC					
L11	ACT_n	Miscellaneous	62	ACT_n	114	ACT_n
L12	A14/WE_n		228	WE_n/A14	151	A14/WE_n
L13	CS0_n		84	CS0_n	149	CS0_n
L14	VDD					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
L15	GND		138	VSS	98	VSS
L16	VDD					
L17	VTT		221	VTT	258	VTT
M1	A11		210	A11	120	A11
M2	GND		147	VSS	99	VSS
M3	A7		211	A7	122	A7
M4	A1		72	A1	133	A1
M5	RESET_n		58	RESET_n	108	RESET_n
M6	A4		214	A4	128	A4
M7	GND		149	VSS	102	VSS
M8	NC					
M9	VREFCA		146	VREFCA	164	VREFCA
M10	NC					
M11	GND		151	VSS	103	VSS
M12	A16/RAS_n		82	RAS_n/A16	152	A16/RAS_n
M13	ODT0		87	ODT0	155	ODT0
M14	CK0_c		75	CK0_c	139	CK0_c
M15	CK0_t	Clock	74	CK0_t	137	CK0_t
M16	GND		154	VSS	106	VSS
M17	VTT					
N1	PARITY		222	PARITY	143	PARITY
N2	A2		216	A2	132	A2
N3	A8		68	A8	125	A8
N4	A0	Address	79	A0	144	A0
N5	A5		213	A5	126	A5
N6	A3		71	A3	131	A3
N7	BA0	Bank Group	81	BA0	150	BA0

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
N8	NC					
N9	A10/AP		225	A10/AP	146	A10/AP
N10	NC					
N11	BG1	Connect to Processor / Memory Controller for future migration from 4GB to 8GB MCP	207	BG1	113	BG1
N12	A15/CAS_n		86	CAS_n/A15	156	A15/CAS_n
N13	CKE0		60	CKE0	109	CKE0
N14	VDD					
N15	GND		156	VSS	107	VSS
N16	VDD					
N17	VTT					
P1	VDD					
P2	GND		158	VSS	167	VSS
P3	GND		160	VSS	168	VSS
P4	VDD					
P5	GND		162	VSS	171	VSS
P6	VDD					
P7	GND		165	VSS	172	VSS
P8	NC					
P9	NC					
P10	NC					
P11	NC					
P12	GND		167	VSS	175	VSS
P13	NC					
P14	NC					
P15	GND		169	VSS	176	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
P16	NC					
P17	NC					
R1	VTT					
R2	GND		171	VSS	180	VSS
R3	VDD					
R4	GND		173	VSS	181	VSS
R5	VDD					
R6	VDD					
R7	DQ62		135	DQ62	245	DQ62
R8	NC					
R9	GND		176	VSS	184	VSS
R10	NC					
R11	DQ59		282	DQ59	250	DQ59
R12	GND		178	VSS	185	VSS
R13	NC					
R14	NC					
R15	NC					
R16	NC					
R17	NC					
T1	GND		180	VSS	188	VSS
T2	VDD					
T3	GND		182	VSS	189	VSS
T4	VDD					
T5	VDD					
T6	GND		184	VSS	192	VSS
T7	DQ60		128	DQ60	232	DQ60
T8	GND		187	VSS	193	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible
4GB (x16) or 8GB (x8) Single Channel x 72

Sort by Ballout

Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
T9	DQ61		273	DQ61	233	DQ61
T10	NC					
T11	DQ57		275	DQ57	236	DQ57
T12	VDD					
T13	DQ54		124	DQ54	224	DQ54
T14	GND		189	VSS	196	VSS
T15	DQ51		271	DQ51	229	DQ51
T16	DM6_n		121	DM6_n, DB16_n, NC	220	DM6_n, DB16_n, NC
T17	GND		191	VSS	197	VSS
U1	NC					
U2	NC					
U3	NC					
U4	NC					
U5	GND		193	VSS	201	VSS
U6	NC					
U7	DQ63		280	DQ63	246	DQ63
U8	VDD		231	VDD	124	VDD
U9	DQ58		137	DQ58	249	DQ58
U10	ZQ6	Calibration Reference				
U11	DQ52		117	DQ52	211	DQ52
U12	DQ53		262	DQ53	212	DQ53
U13	DQ55		269	DQ55	225	DQ55
U14	VDD					
U15	DQ48	DataByte 6	119	DQ48	216	DQ48
U16	VDD					
U17	DQS6_c		266	DQS6_c	219	DQS6_c
V1	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
V2	NC					
V3	NC					
V4	NC					
V5	GND		195	VSS	202	VSS
V6	NC					
V7	NC					
V8	VDD		233	VDD	118	VDD
V9	DQ56	DataByte 7	130	DQ56	237	DQ56
V10	ZQ7	Calibration Reference				
V11	GND		198	VSS	205	VSS
V12	DM7_n		132	DM7_n, DB17_n, NC	241	DM7_n, DB17_n, NC
V13	DQS7_t		278	DQS7_t	242	DQS7_t
V14	GND		200	VSS	206	VSS
V15	DQ50		126	DQ50	228	DQ50
V16	GND		202	VSS	209	VSS
V17	DQS6_t		267	DQS6_t	221	DQS6_t
W1	NC					
W2	NC					
W3	GND		239	VSS	210	VSS
W4	NC					
W5	NC					
W6	NC					
W7	GND		241	VSS	213	VSS
W8	GND		243	VSS	214	VSS
W9	VDD					
W10	GND		246	VSS	217	VSS
W11	VDD					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
W12	GND		248	VSS	218	VSS
W13	DQS7_c		277	DQS7_c	240	DQS7_c
W14	VDD					
W15	GND		250	VSS	222	VSS
W16	DQ49		264	DQ49	215	DQ49
W17	VPP		288	VPP		
Y1	NC					
Y2	NC					
Y3	NC					
Y4	NC					
Y5	NC					
Y6	GND		252	VSS	223	VSS
Y7	NC					
Y8	VDD		236	VDD	129	VDD
Y9	DQ39		247	DQ39	182	DQ39
Y10	ZQ5	Calibration Reference				
Y11	DQ34		104	DQ34	187	DQ34
Y12	DQS4_c		244	DQS4_c	177	DQS4_c
Y13	NC					
Y14	GND		254	VSS	226	VSS
Y15	VDD					
Y16	DM5_n		110	DM5_n, DB15_n, NC	199	DM5_n, DB15_n, NC
Y17	GND		257	VSS	227	VSS
AA1	NC	No Connect				
AA2	NC					
AA3	NC					
AA4	NC					

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
AA5	GND		259	VSS	230	VSS
AA6	NC					
AA7	NC					
AA8	GND		261	VSS	231	VSS
AA9	DQ32	DataByte 4	97	DQ32	174	DQ32
AA10	ZQ4	Calibration Reference				
AA11	DM4_n		99	DM4_n, DB14_N, NC	178	DM4_n, DB14_N, NC
AA12	DQS4_t		245	DQS4_t	179	DQS4_t
AA13	DQ47		258	DQ47	204	DQ47
AA14	DQ45		251	DQ45	190	DQ45
AA15	DQ42		115	DQ42	207	DQ42
AA16	GND		263	VSS	234	VSS
AA17	DQS5_t		256	DQS5_t	200	DQS5_t
AB1	GND		265	VSS	235	VSS
AB2	NC					
AB3	GND		268	VSS	238	VSS
AB4	NC					
AB5	VDD					
AB6	NC					
AB7	DQ38		102	DQ38	183	DQ38
AB8	GND		270	VSS	239	VSS
AB9	DQ37		240	DQ37	169	DQ37
AB10	GND		272	VSS	243	VSS
AB11	DQ33		242	DQ33	173	DQ33
AB12	VDD					
AB13	DQ46		113	DQ46	203	DQ46
AB14	GND		274	VSS	244	VSS

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72						
Sort by Ballout						
Byte	0	1	2	3		
Byte	4	5	6	7	ECC	
Control	Clock	Addr	Bank Grp	Miscel		
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8	
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8	
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V	
9/18/2018	Rev C3					
MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
AB15	DQ40	DataByte 5	108	DQ40	195	DQ40
AB16	VDD					
AB17	DQS5_c		255	DQS5_c	198	DQS5_c
AC1	VPP		287	VPP		
AC2	GND		276	VSS	247	VSS
AC3	VDD					
AC4	GND		279	VSS	248	VSS
AC5	VDD					
AC6	GND		281	VSS	251	VSS
AC7	DQ36		95	DQ36	170	DQ36
AC8	GND		283	VSS	252	VSS
AC9	VDD					
AC10	GND					
AC11	DQ35		249	DQ35	186	DQ35
AC12	GND					
AC13	DQ44		106	DQ44	191	DQ44
AC14	GND					
AC15	DQ43		260	DQ43	208	DQ43
AC16	DQ41		253	DQ41	194	DQ41
AC17	GND					
			142	VPP		
		Signals for External	139	SA0	256	SA0
		SPD EEPROM to interface	140	SA1	260	SA1
		to Host Processor /	238	SA2	166	SA2
		Memory Controller	141	SCL	253	SCL
		if used	285	SDA	254	SDA
			284	VDDSPD	255	VDDSPD

4GB x16 & 8GB x8 Ballout - Mapped to JEDEC DDR4 : 288 Pin UDIMM & 260 Pin SO-DIMM Compatible 4GB (x16) or 8GB (x8) Single Channel x 72					
Sort by Ballout					
Byte	0	1	2	3	
Byte	4	5	6	7	ECC
Control	Clock	Addr	Bank Grp	Miscel	
ZQ x16	ZQ0	ZQ2	ZQ4	ZQ6	ZQ8
ZQ x8	ZQ0, ZQ1	ZQ2, ZQ3	ZQ4, ZQ5	ZQ6, ZQ7	ZQ8
Power	GND / VSS	VREFCA = VDD/2 = 0.6V	VDD = 1.2V	VPP = 2.5V	VTT = VDD/2 = 0.6V
9/18/2018	Rev C3				

MCP - 391 Balls		Notes	JEDEC UDIMM - 288 pin		JEDEC SO-DIMM - 260 pin	
Ball	Signal MCP		Pin UDM	Signal UDM	Pin SODM	Signal SODM
		Not Required - NC	219	CK1_c	140	CK1_c
			218	CK1_t	138	CK1_t
			203	CKE1	110	CKE1
			78	EVENT_n	134	EVENT_n
			91	ODT1	161	ODT1
			89	CS1_n	157	CS1_n
			93	CS2_n C[0]	162	C0, CS2_n, NC
			237	CS3_n C[1]	165	C1, CS3_N, NC
			234	A17 NC		
			235	C[2] NC		
			1	12V NC		
			145	12V NC		
		Reserved - NC	144	RFU		
			205	RFU		
			227	RFU		
		No Connect	19	NC		
			30	NC		
			41	NC		
			100	NC		
			111	NC		
			122	NC		
			133	NC		
			52	NC		
			8	NC		
			230	NC		

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