How to improve EV12AQ600 ADC SNR performance using Simultaneous Sampling and Averaging

October 2019

Introduction

This document aims at describing the potential gain in Signal to Noise Ratio (SNR) achievable through simultaneous sampling and averaging of the 4 cores of the Teledyne e2v's EV12AQ600, a 12-bit quad 1.6/3.2/6.4 GSps ADC. The method is compared to the averaging of multiple acquisitions.
Documents such as the datasheet of the EV12AQ600 ADC have to be read prior to this application note.

Note: it is recommended to refer to the product datasheet to get more details on EV12AQ600 configuration registers.

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1. Definition of Terms

ADC: Analog to Digital Converter

CPS: Cross-Point Switch

ENOB: Effective Number Of Bits

SNR: Signal to Noise Ratio

THD: Total Harmonic Distortion

2. Theory

Given a signal:

$f_i(t) = s_i(t) + z_i(t)$, where $s_i(t)$ is a sine wave and $z_i(t)$ some added noise.

If we assume for simplicity that $z_i(t)$ is random (uncorrelated) and $s_i(t)$ is not correlated to $z_i(t)$ then summing multiple signals leads to:

$$\sum_i f_i(t) = \sum_i s_i(t) + \sqrt{\sum_i z_i^2(t)} = N * S(t) + \sqrt{N} * \sigma_z(t)$$

, where $\sigma_z(t)$ is the noise rms value.

The sine wave signals add constructively while noise adds in quadrature (for more detailed calculations, the user can refer to Lemons (2002)[1].

When expressed in terms of SNR, summing and averaging N signals shows that:

$$\sum_i SNR_i = \sum_i \frac{s_i(t)}{z_i(t)} = \frac{N * S(t)}{\sqrt{N} * \sigma_z(t)} = \sqrt{N} * SNR$$

Key information
Averaging N signals will improve SNR by a factor of $\sqrt{N}$

The theoretical gain in SNR (expressed in dB) obtained when averaging multiple signals is therefore:

Number of signals	Increase in SNR (dB)
2	3
4	6
16	12
64	18

[1] D.S. Lemons, An Introduction to Stochastic Processes in Physics, The Johns Hopkins University Press, p. 34, 2002

In conclusion, summing and averaging 4 ADCs signals (and any subsequent power of 4) ideally leads to a 6 dB increase in SNR (under the assumption that noise is totally random and uncorrelated), hence an increase of 1-bit of ENOB (provided that distortion is negligible).

3. ADC configuration

Thanks to its built-in Cross-Point Switch (CPS) and clock control, the EV12AQ600 ADC allows simultaneous sampling of its 4 internal ADCs.

The CPS distributes the analog input signal to the 4 independent ADCs as depicted in Figure 1. The CPS configuration is controlled by SPI through the CPS_CTRL register (@0x000B, value 000). In addition, the clock sampling mode can be configured so that each independent ADC samples the signal simultaneously at the exact same time. This is controlled by SPI through the CLK_MODE_SEL register (@0x000A, value 11).

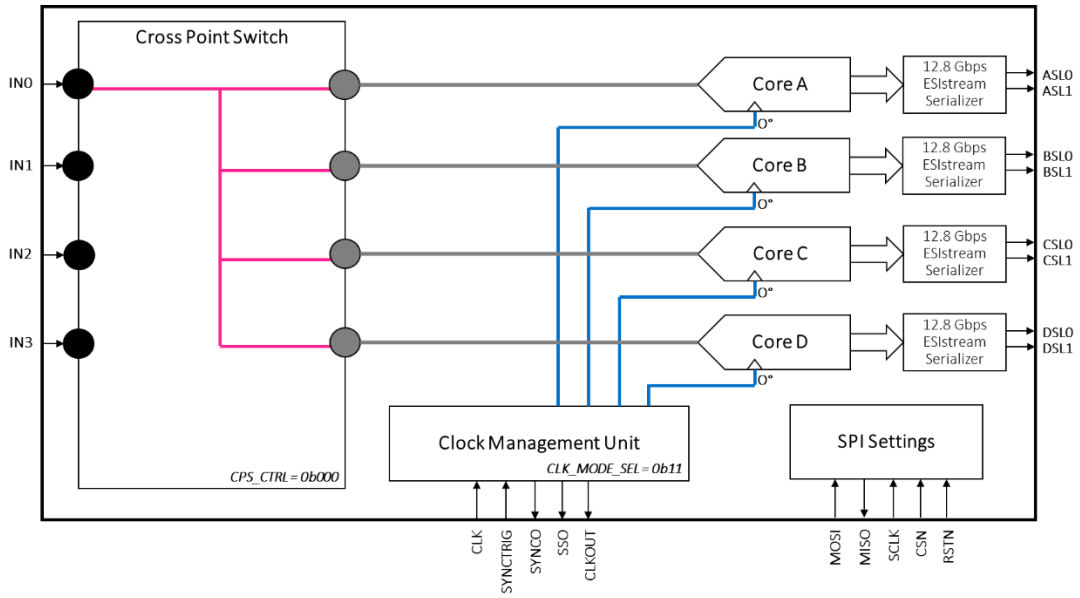

Figure 1 – CPS and clock mode configurations

CPS_CTRL register configuration:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value														0	0	0

CLK_MODE_SEL register configuration:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															1	1

4. Measurement results and Analysis

Impact on Signal to Noise Ratio

SNR measurement results are plot on Figure 2.

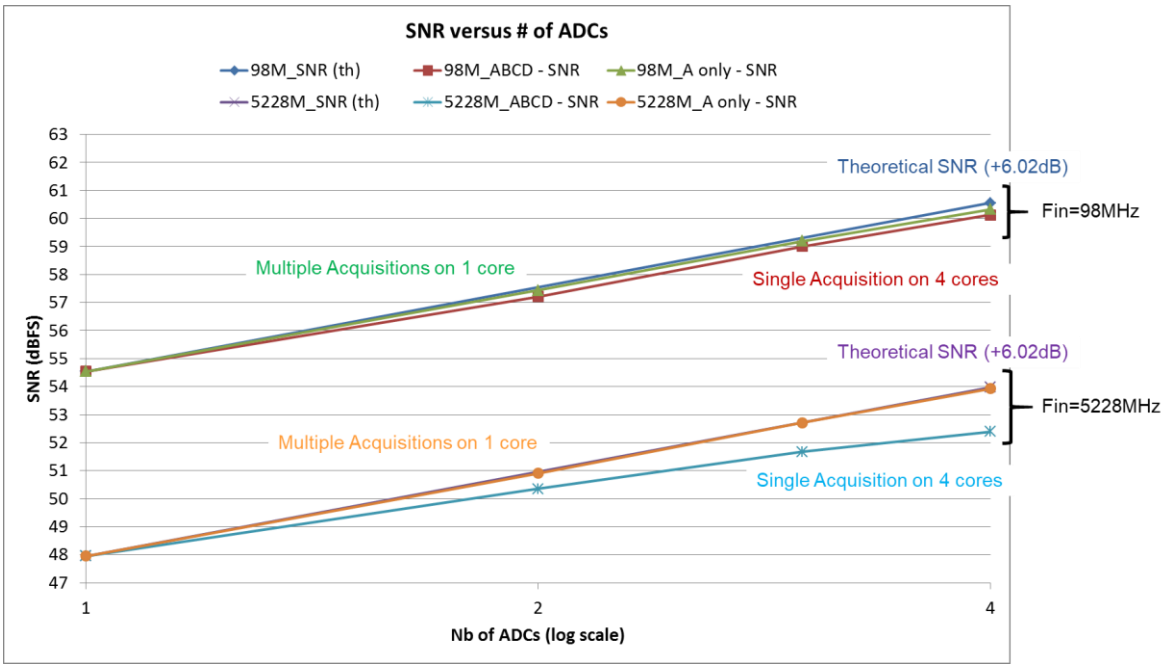

Figure 2 – SNR results

At low frequencies (100MHz), averaging 4 ADCs (or 4 acquisitions of the same ADC) allows for a gain in SNR of almost 6 dB (near theoretical value).

- At low frequencies, the SNR is dominated by thermal noise, while jitter induced and quantization noise are an order of magnitude lower.
- Thermal noise being perfectly white and uncorrelated, averaging reduces its impact strongly. The slight deviation is due to residual correlated noise in Jitter induced noise (see below)

At higher frequencies (>5GHz), we can see that while averaging 4 acquisitions of the same ADC leads to a 6 dB gain in SNR. Doing so with 4 different ADCs leads to a much lower increase (4.5 dB).

- At higher frequencies, the SNR is mainly dominated by clock jitter (one order of magnitude higher than thermal noise and 2 orders higher than quantization noise).
- Due to the intrinsic nature of clock distribution in EV12AQ600, the clock jitter propagates equally and coherently to each ADC core so that averaging does not reduce this portion of noise.
- When averaging 4 different acquisitions of the same core, the clock jitter is redistributed randomly at each acquisition so that averaging reduces its impact.

When averaging a higher number of ADCs, this effect levels out as all uncorrelated components of jitter induced noise are wiped out and only remains the correlated part.

Results summary:

	Increase in SNR (dB)				
		Fin = 98 MHz		Fin = 5228 MHz	
Nb of ADCs or acquisitions	Theoretical	Multiple acq.	Multiple ADCs	Multiple acq.	Multiple ADCs
2	3.01	2.89	2.68	2.95	2.39
4	**6.02**	**5.79**	**5.60**	**5.98**	**4.44**

Impact on Total Harmonic Distortion

In order to illustrate the fact that the linearity is not impacted by the simultaneous and averaging computation, the THD is plotted on Figure 3.

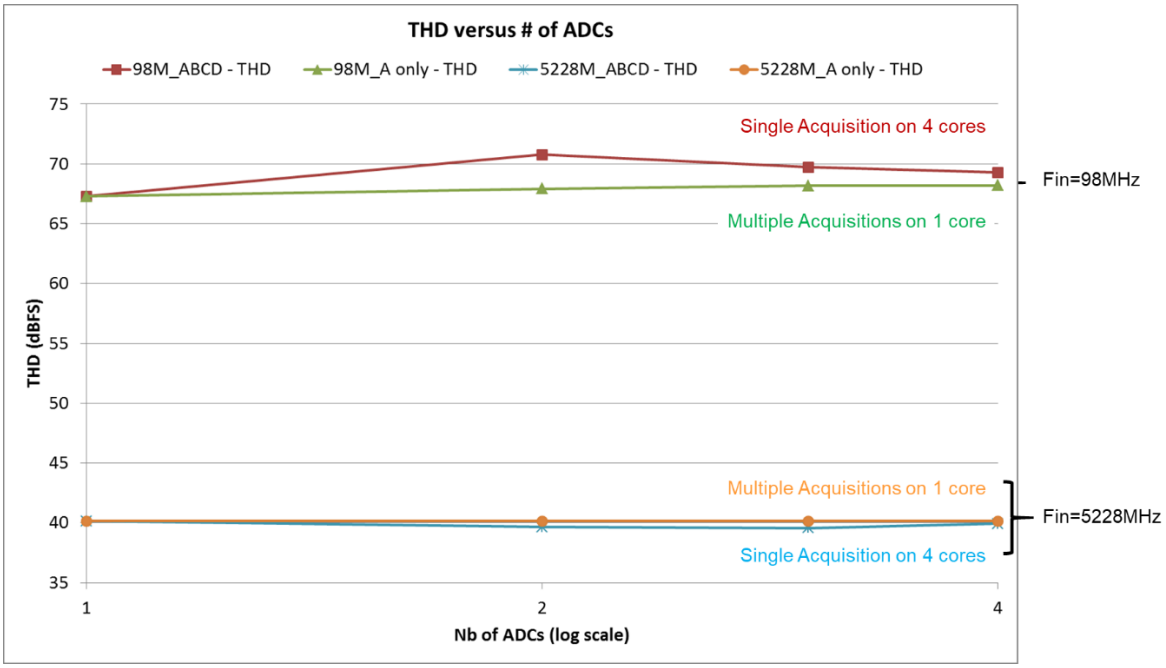

Figure 3 – THD results

Impact on ENOB

ENOB measurement results are plotted on Figure 4.

As can be observed, averaging does only enhance ENOB for low frequencies.

ENOB is defined as: $ENOB = \frac{(SINAD - 1.76)}{6.02}$, where SINAD is SNR + distorsion and can be expressed has: $SINAD = -10 * \log\left(10^{-SNR/10} + 10^{-THD/10}\right)$

At low frequencies, SINAD is dominated by SNR ($SINAD \sim -10 \times \log\left(10^{-SNR/10}\right)$)

The increase in SNR due to averaging thus directly impacts SINAD, hence ENOB.

When going to higher frequencies, the THD tends to dominate SINAD ($SINAD \sim -10 \times \log\left(10^{-THD/10}\right)$).

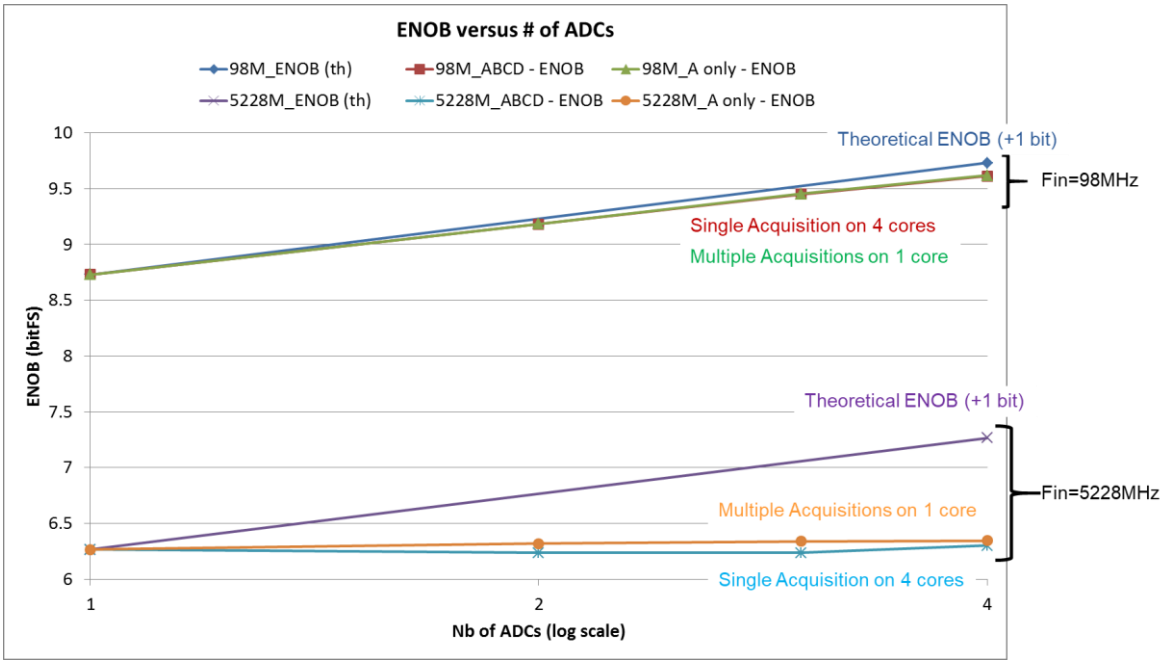

Figure 4 – ENOB results

Impact on spectrum plot

Spectrum plots are shown on Figure 5.

Spectrum representation clearly shows the gain in SNR (lower noise floor) when averaging is applied.

Averaging multiple ADCs slightly impacts the level of higher order harmonic spurs (>H5).

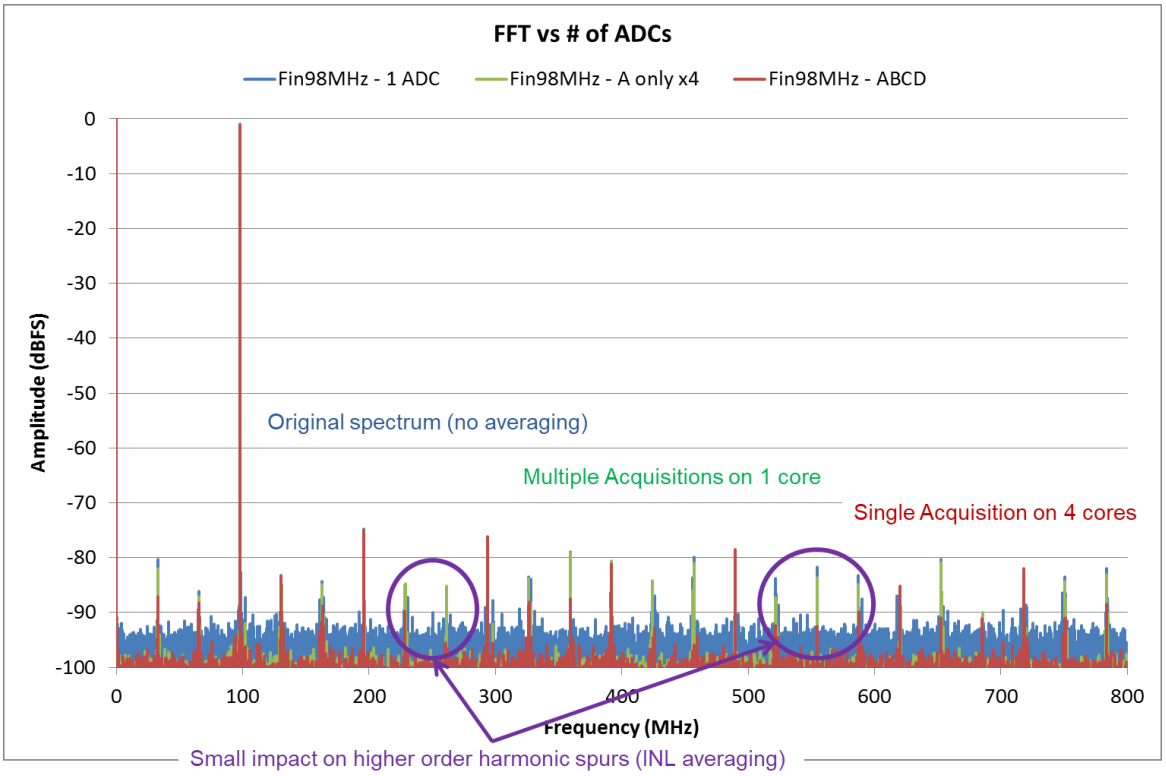

Figure 5 – Spectrum plots

For more information, please contact: GRE-HOTLINE-BDC@Teledyne.com

Related documentation

EV12AQ600 Datasheet available on the Product Webpage:
https://www.teledyne-e2v.com/products/semiconductors/adc/ev12aq600/

Newsletter about synchronization chaining scheme used by EV12AQ600:
https://www.teledyne-e2v.com/products/semiconductors/teledyne-e2v-semiconductors-newsletters/adcsynchronization/

Revision history

Table 1 – Document revision history

Date	Revision	Changes
October 2019	A.1	Initial release

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