EV12DS130B – Multi Component Synchronization

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Scope :	**BUSINESS UNIT BMS CLIENTS - CUSTOMERS**

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Approbation

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1. DOCUMENT AMENDMENT RECORD

Author	Issue	Date	Reason for change
BARNEOUD Heline	A	24/02/2023	Creation

Approbation

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The EV12DS130B, is Teledyne e2v solution to allow easy interface with standard LVDS FPGAs while benefiting from the 3GSps performance. It is a single channel 12-bit DAC.

If you require any support, please contact your local FAE or send an email at GRE-HOTLINE-BDC@Teledyne.com.

Summary

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2. INTRODUCTION:

To ensure synchronous behavior between several DACs it is mandatory that the sampling clocks are aligned at the clock input of both of the components.
EV12DS130B has a SYNC input, that is used as a synchronization input: both DACs SYNC input must be time aligned at the input of each component.

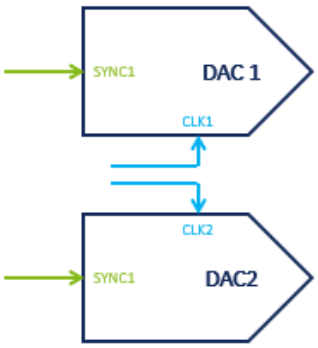

Figure 1: EV12DS130B SYNC input in multi component configuration

The uncertainty due to the state of the latches around clock edges leads to metastability. To ensure deterministic conversion, the SYNC signal edges must be positioned in regards to the clock edges. Thus, it will ensure, for each DAC to have a deterministic start.

Figure 2: EV12DS130 illustration of deterministic start area

DAC analog output and DSP_CLK output will stop deterministically if SYNC rising edge falls out of metastable zone defined by T1 and T2 timings.

DAC analog output and DSP_CLK output will restart deterministically if SYNC falling edge falls out of metastable zone defined by T1 and T2 timings.

Only position of SYNC falling edge compared to T1 and T2 timings impacts deterministic restart of DSP_CLK.
So, SYNC pulse must be synchronous with DAC input clock.

To ensure a deterministic synchronization over multiple DACs, we suggest the 3 following methods. Next chapter is dedicated to description of each solution, and T1 T2 timings measurements can be found in annex.

3. SYNC GENERATION METHODS

3.1 Generating the SYNC with an FPGA

This solution is based on a SYNC pulse is sent by the FPGA directly to the DAC time aligned at the DAC input.

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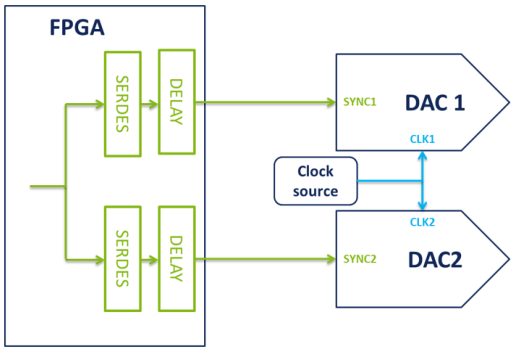

Figure 3: SYNC generation with an FPGA

The SERDES lines allows to improve the speed and edges of the SYNC signal, the clock is used to generate the SYNC
With this configuration, the delay bloc can be used to tune the SYNC timings versus the DAC clock and help to avoid meta-stability. It is also a good way to cope with temperature impact on the timing.
This solution eases the timing management and reduces the constraints on the SYNC signal layout if the delay has a small enough granularity.
It is important no metastability occurs at the SYNC input of the DACs for this solution to work.

3.2 Compensating the delay between DACs in the FPGA

The following implementation is using an FPGA and a delay detection stage. It is only compensating delays, not solving metastabilities.
After power-up, the delay between DACs is identified through the detection stage after the DAC output.
The delay information is then corrected either prior to the DAC or in the reception stage through a buffer adding the correct number of clock cycle.

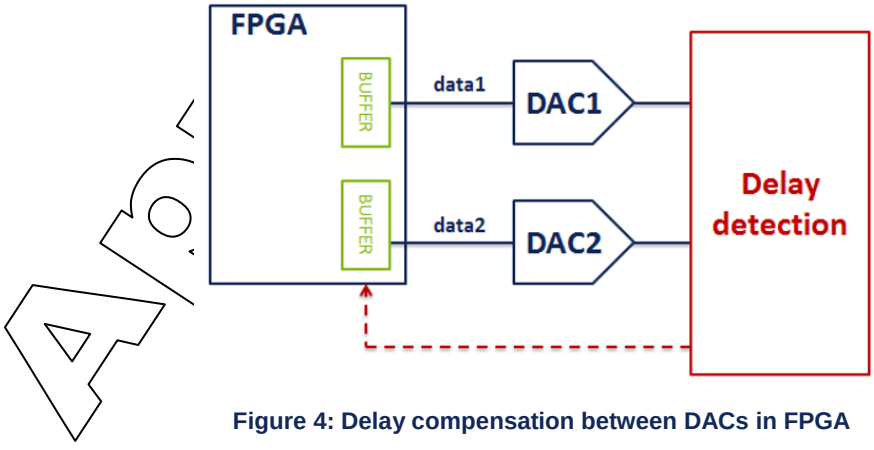

Figure 4: Delay compensation between DACs in FPGA

- This solution requires only some digital processing but imply that a detection method is possible.
- The correction to add is only a multiple of clock cycle onto one or the other path.

However it needs to be done at every start-up of the system as the timing in the DAC starts randomly if no SYNC is done.
Detection method are generally built into systems like MIMO or phased array receptors.
Other detection system could involve a feedback loop from the DAC output back to the FPGA through an ADC.

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To facilitate the detection, test mode can be implemented in the FPGA and output of the DAC and the SYNC is unused in this case.

3.3 Using external flip-flop :

This architecture uses external fast flip flop.
The SYNC pulse is sent by the FPGA to the fast flip-flop, the fast flip-flop output is then propagated to the DACs. They are using the same or inverted clock in regard to the DAC.

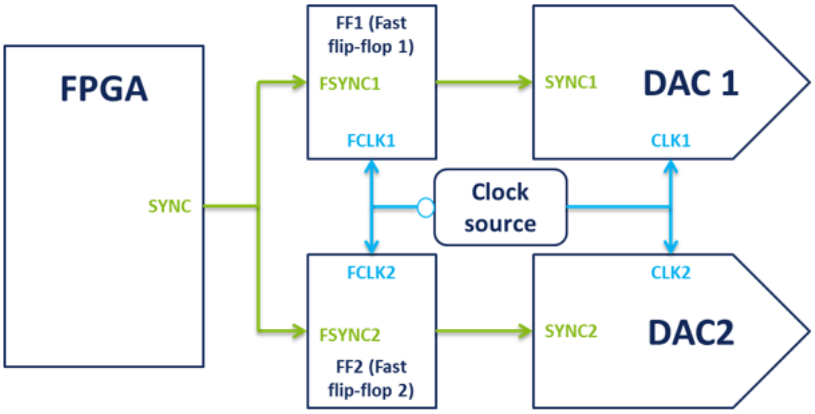

Figure 5: SYNC signal propagated by Fast Flip-Flop from FPGA to DACs

- This solution facilitates the timing management and reduces the constraints on the SYNC signal layout.
- The propagation time of the SYNC path needs to be considered carefully so that SYNC1 and SYNC2 arrives within the same clock cycle.
- The clock used for the flip-flop can be divided by 2 or 4 compared to the DAC to ease the timing at the flip-flop input.

A single flip flop can be used for multiple DACs. In that case, the metastability at the flip flop input is not an issue but the SYNC trace length matching may be harder to achieve
It is important no metastability occurs at the flip flop input and the SYNC input of the DACs for this solution to work.

Applicable

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ANNEX : MEASURE OF TIME T1 AND T2 ON THE EV12DS130B

Why perform this measure ?

This T1 T2 timing measure has been performed due to the rising need of using several DACs or several synched DACs channels. The target is to provide to the customer a solution to implement correct synchronization procedure when multiple DAC are required.
If multiple DACs need to be synchronized, then a deterministic SYNC must be sent out of the metastable zone of each DAC.
To perform this, two methods can be implemented:

- T1 T2 timing must be respected for the SYNC position in regards to the clock.
- Creation of a DSP_CLK Phase detector characterize the metastable zone in “real time” using Idelay and Odelay features of the FPGA (in our example Xilinx Ultrascale) and then send the SYNC out of the metastable zone selecting the right Odelay value.
  This solution needs an external reference clk (DIV_CLK) synchronous to DAC_CLK and connected to the FPGA to sample DSP_CLK.

In this application note, we will focus only on the first method where T1 and T2 must be respected. Below are presented the measures of T1 values for 2 EV12DS130B different sample at several clock rate and using a wide temperature range. This, to see impact of clock frequency and of temperature over the T1 value.

Setup equipment:

To perform this test of characterization of T1 timing the following equipment was used:

- Teledyne LeCroy Waverunner 640Zi scope with two differential probes
- Rohde&Schwartz signal generator SMA100A (x2)
- Agilent 81134A Pulse generator

The synoptic of the set-up is presented below:

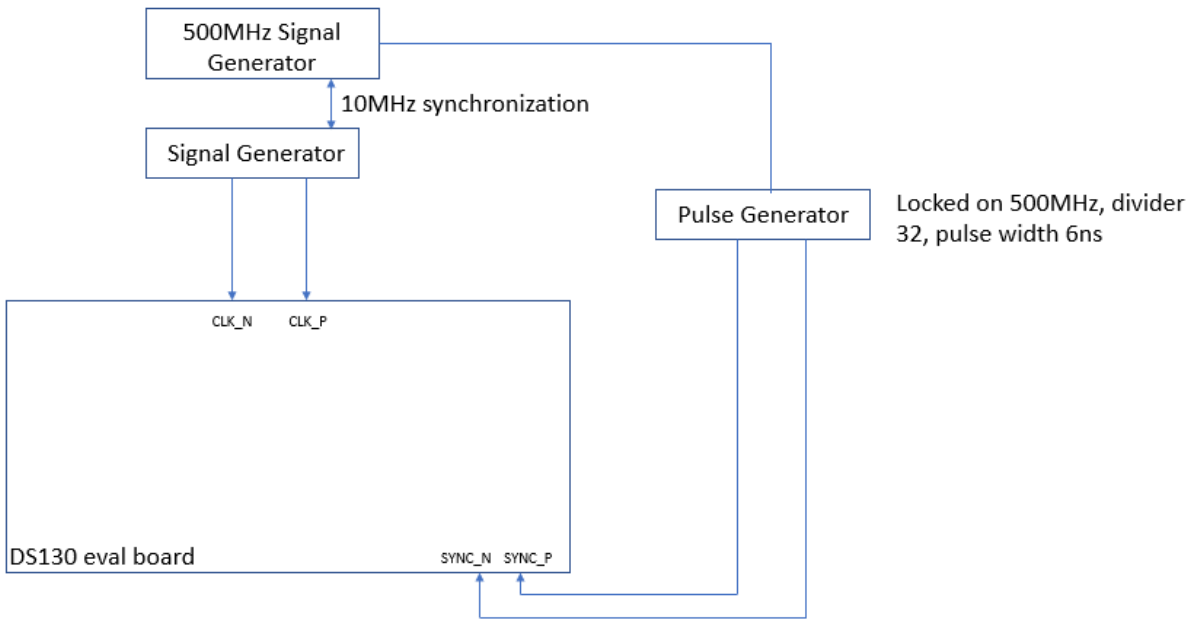

Figure 6: Synoptic of the measurement setup

The picture taken of the cable configuration is presented below:

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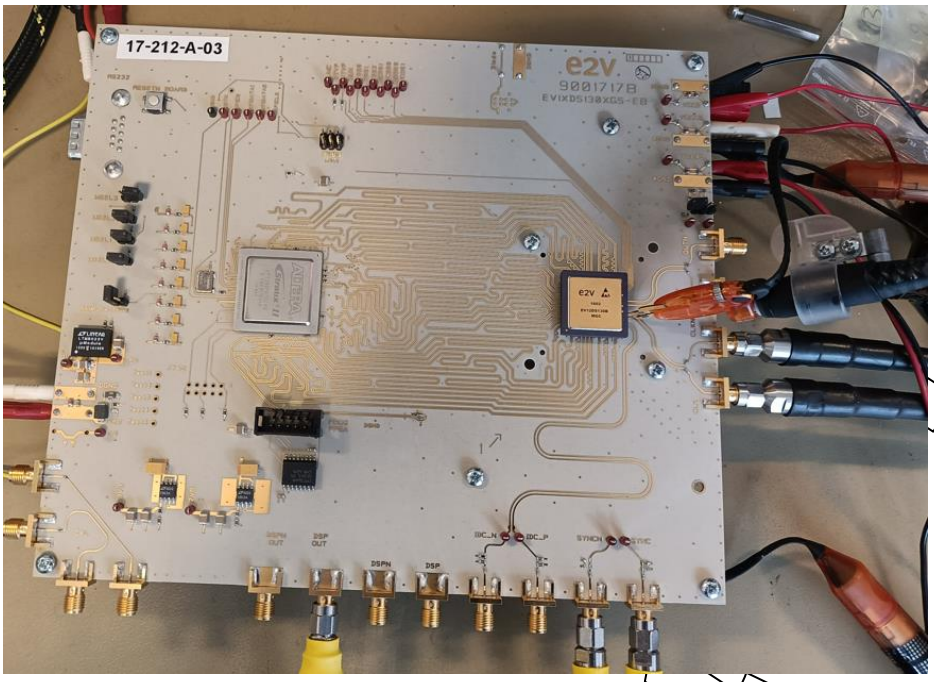

« + » of CLK logic probe is on CLK_N line
-> use of invert function on the Scope

500MHz clock generator (for pulse) and CLK clock generator are synchronized (same 10MHz reference)

SYNC signal logic probe is soldered on the bottom as close as possible to the component (no deskew needed)

DSP signal is visualized on scope in single mode on 50Ohm and used to find metastable zone

Figure 7: Picture of the measure setup

Illustration of the metastable zone

Measures are performed with persistence mode ON: SYNC signal is sent periodically. Multiple occurrences of SYNC are displayed. On the scope capture the DSP signal overlaps itself over the multiple trigs on SYNC rising edge.
The SYNC signal is taken into account on one deterministic clock signal edge. Thus, we ensure if several DACs are provided this same CLK signal and SYNC signal their DSP will start at the same clock edge instant.

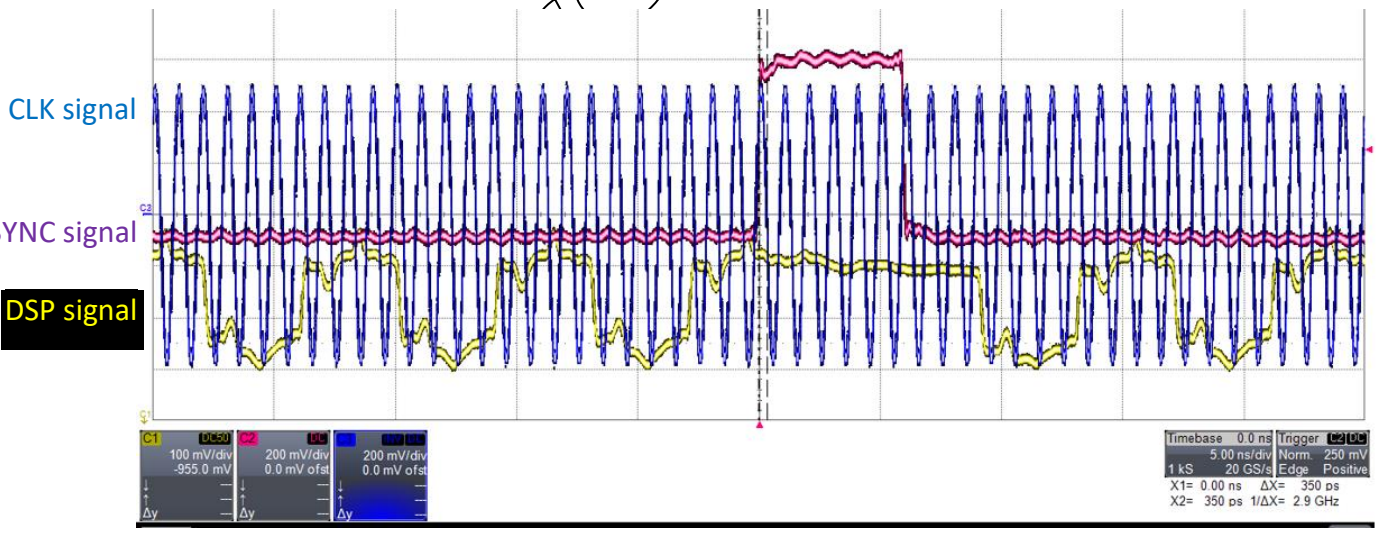

Figure 8: Scope capture SYNC out of metastable zone

Measures are performed with persistence mode ON: SYNC signal is sent periodically. Multiple occurrences of SYNC are displayed. On the scope capture the DSP signal overlaps itself over the multiple trigs on SYNC rising edge.

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The SYNC signal is taken into account on one deterministic clock signal edge. Thus, we ensure if several DACs are provided this same CLK signal and SYNC signal their DSP will start at the same clock edge instant.

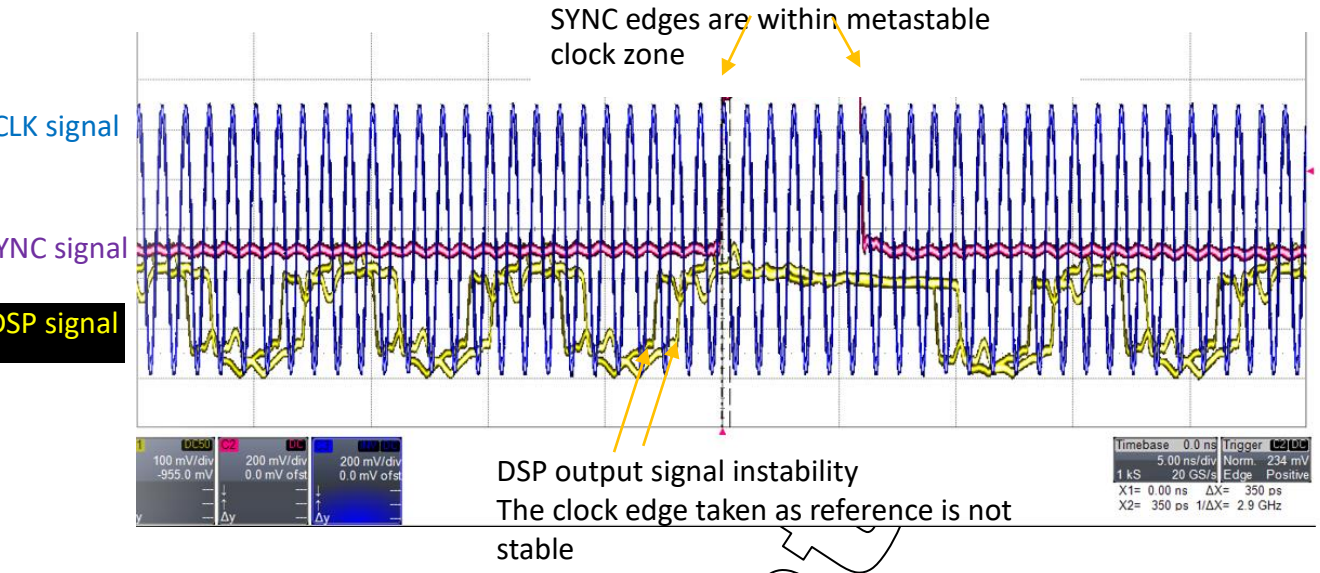

Figure 9: Scope capture SYNC inside clock metastable zone

Metastable zone can be described by the schematic below :

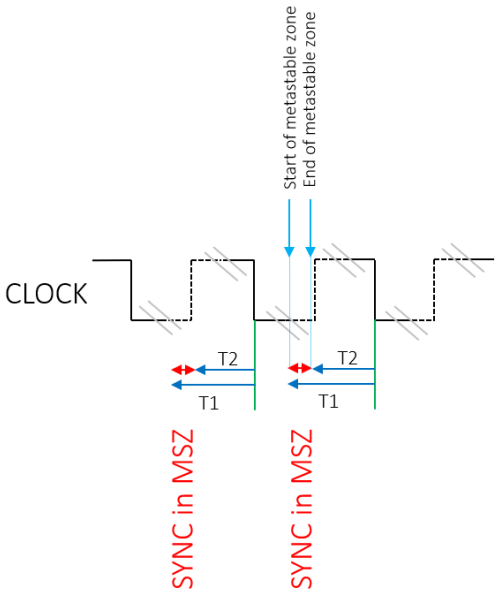

Figure 10: schematical representation of the metastable zone (MSZ)

Note : metastable zone width has been measured and is 20ps wide.

Measure of the delay T1

The measures of T1 delay that are shown below are performed for a clock frequency of 1GHz. Measures are performed at ambient temperature on two different samples. At ambient temperature, values read are the same, approximation error.
The SYNC signal is positioned just before the metastable zone. SYNC pulse width is a multiple of clock period, in this example pulse width is 6 clock period long.

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The aim of this measure is to determine for two metastable positions if the SYNC rising edge time to clock falling edge is the same as SYNC falling edge time to clock falling edge.

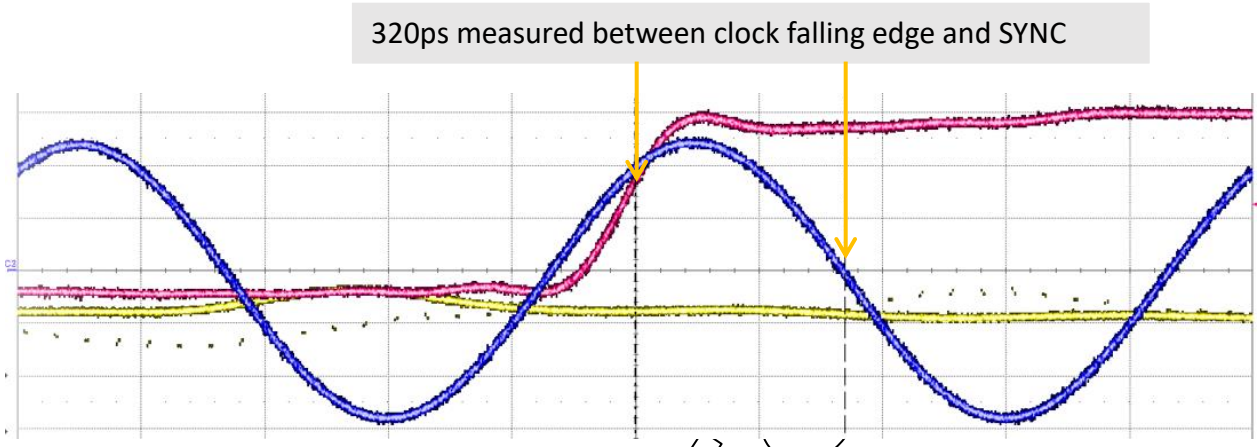

Figure 11: Measure of T1 - clock falling edge reference to SYNC rising edge

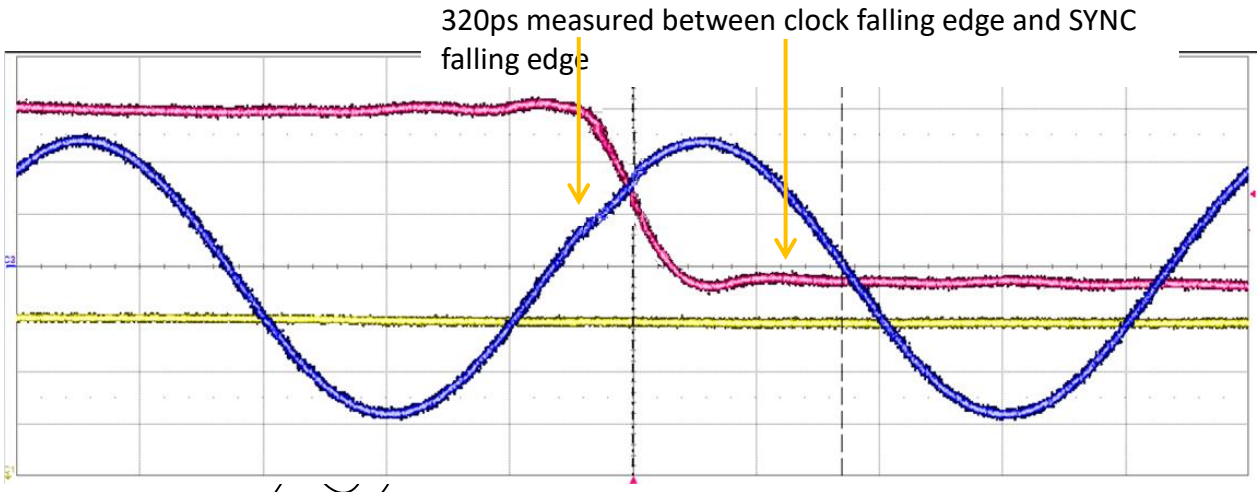

Figure 12: Measure of T1 - clock falling edge reference to SYNC falling edge

Figure 5 and figure 6 allowed us to state that SYNC rising edge and falling edge can be taken indifferently.
At room temperature, measures have been performed on two samples for a range of frequencies starting at 500MHz to 3GHz.
The measures are presented in the table below :

Part	Clock frequency	T1: SYNC rising edge to CLK falling edge
Board A 17-212-A03	500MHz	320ps
	1GHz	346ps
	2GHz	350ps
	3GHz	348ps
Board C	500MHz	310ps

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22-212-C03	1GHz	350ps
	2GHz	350ps
	3GHz	366ps

Table 1: Measures of T1 values for two parts at different clock frequencies

At room temperature on two parts, timing measured are the same (approximation of the reading error).

Measures of time T1 versus clock frequency and versus temperature have been made on the two samples.
Results are presented in the graph figure 8 and figure 9 (modification of graph scale to perform a zoom)

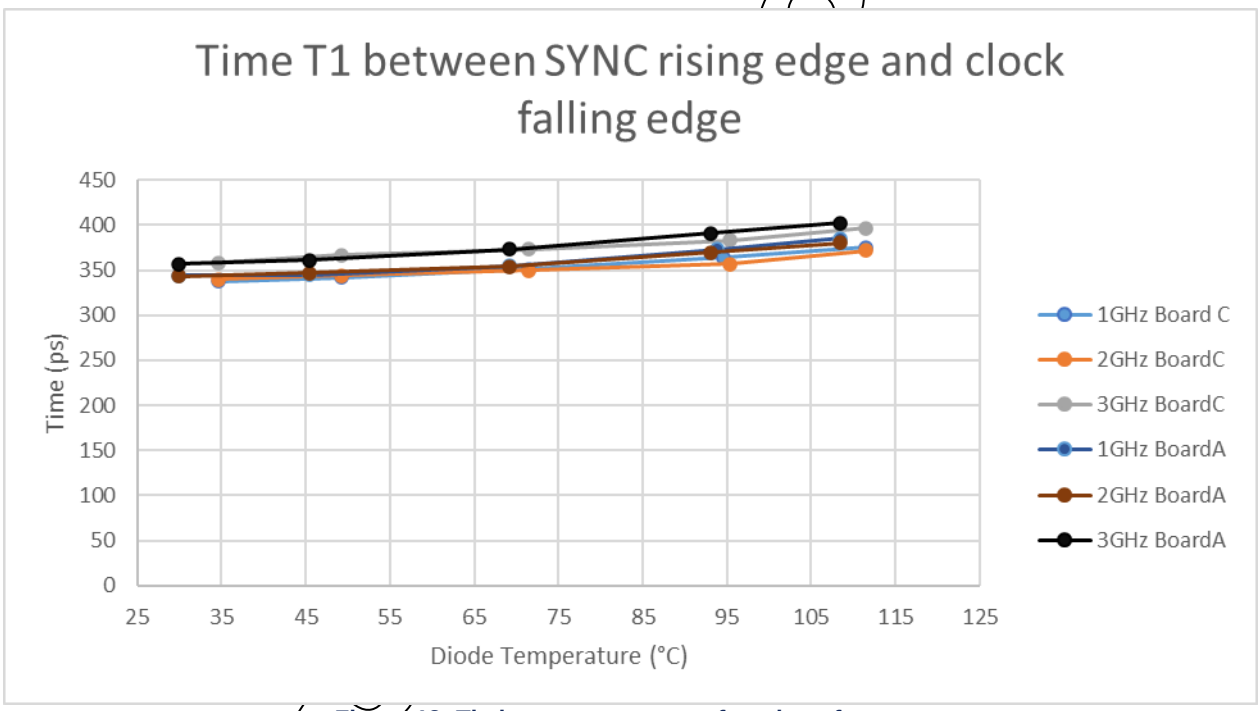

Figure 13: Timing measurements function of temperature

Application Note

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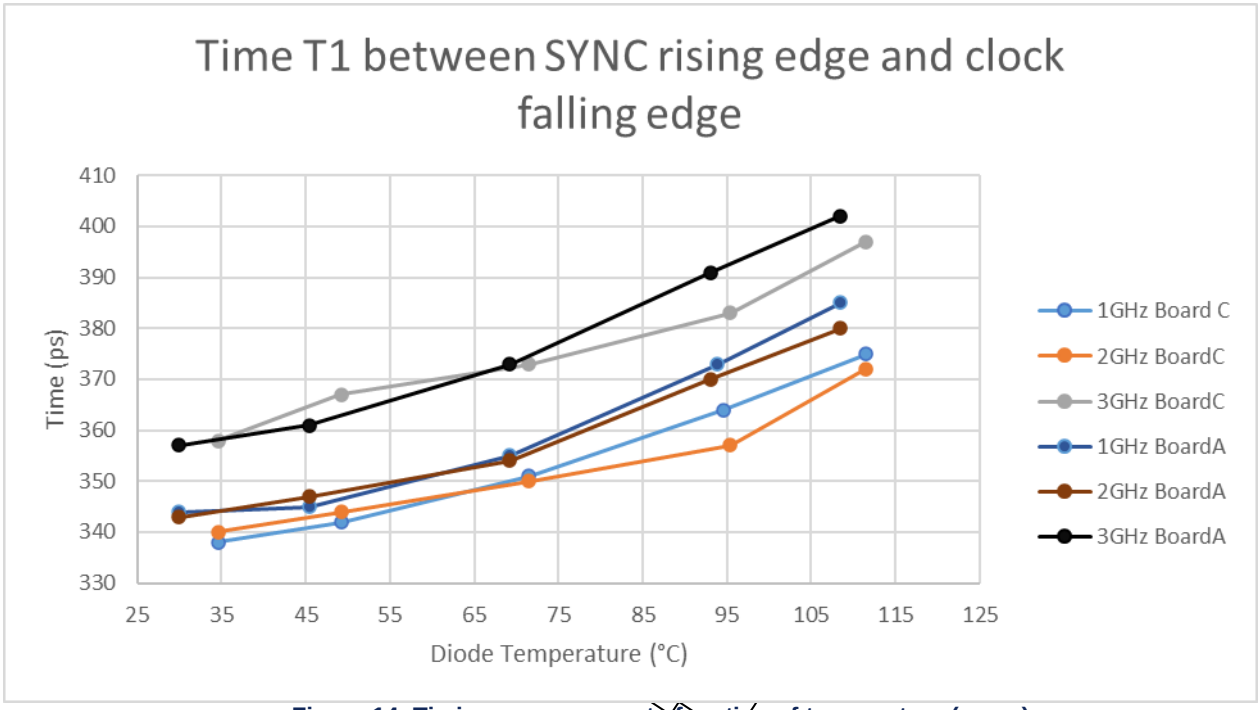

Figure 14: Timing measurements function of temperature (zoom)

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