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ADC EV10AS150A Evaluation Board

User Guide

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Section 1
Introduction

1.1 Scope

The ADC EV10AS150A-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the different versions of EV10AS150A ADC with 1:2/4 DMUX up to its 5 GHz full power input bandwidth.

The ADC EV10AS150A-EB Evaluation Kit includes:

- The EV10AS150A with 1:2/4 DMUX Evaluation board including one version of the EV10AS150A ADC device soldered on the board
- Six SMA caps for CLK, CLKN, VIN, VINN, DRR and ASYNCRST signals
- Six jumpers DMUX function settings (RS, BIST, DRTYPE, SLEEP, STAGG), CLKTYPE jumper is not used
- 3-wire serial link to control ADC functionality

The user guide uses the EV10AS150A Evaluation Kit as an evaluation and demonstration platform and provides guidelines for its proper use.

1.2 Description

The ADC EV10AS150A Evaluation board is very straightforward as it only implements the EV10AS150A ADC/DMUX device, SMA connectors for the sampling clock, analog inputs and reset inputs accesses and HE14 double row 2.54 mm pitch connectors compatible with high speed acquisition system probes.

To achieve optimal performance, the ADC EV10AS150A-EB Evaluation board was designed in a 8-metal-layer board with RO4003 200 µm and FR4 HTG epoxy dielectric materials. The board implements the following devices:

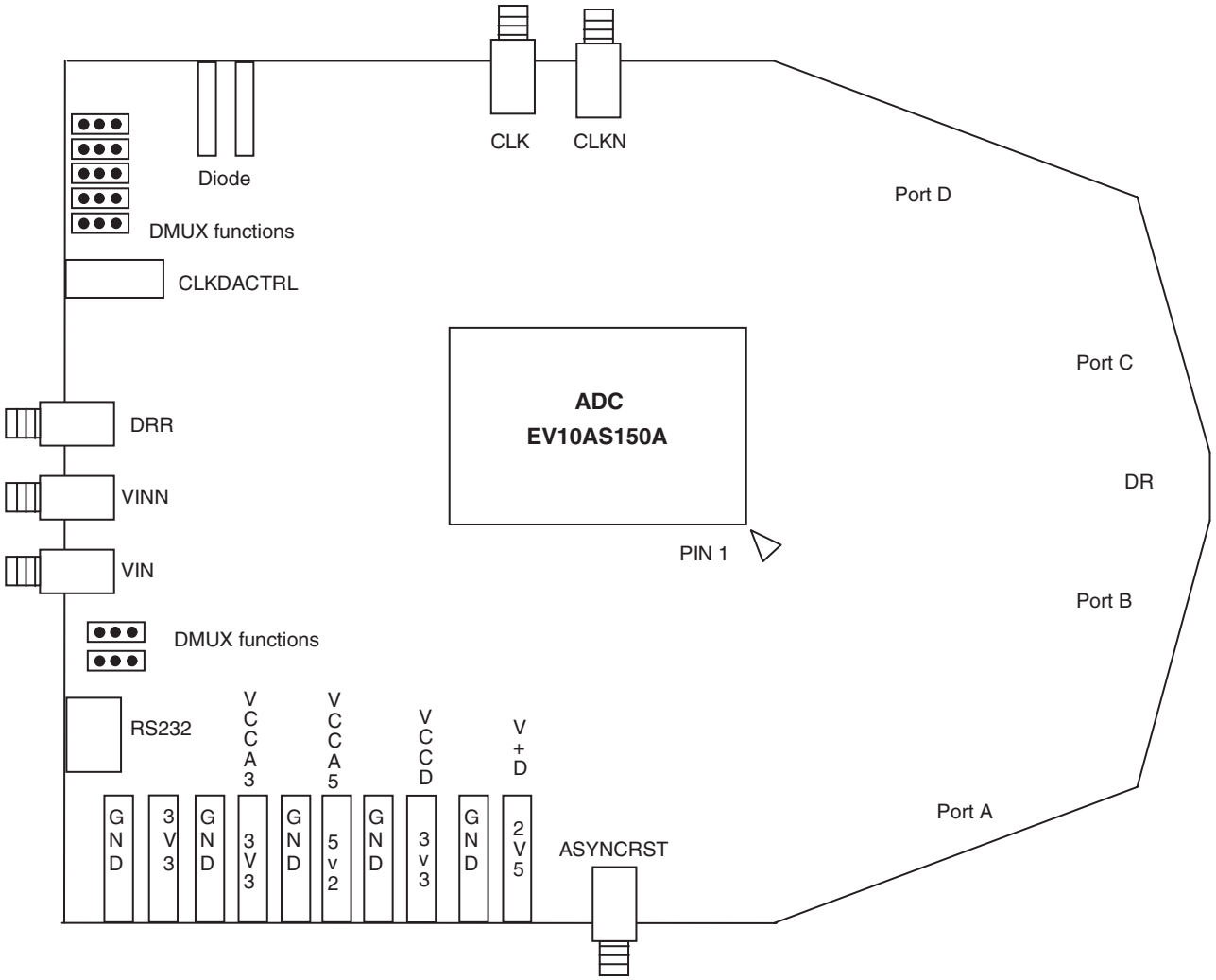
- The ADC EV10AS150A with 1:2/4 DMUX Evaluation board with one version of the EV10AS150A ADC soldered on the board
- Six SMA caps for CLK, CLKN, VIN, VINN, DRR and ASYNCRST signals
- Six jumpers DMUX function settings (RS, BIST, DRTYPE, SLEEP, STAGG), CLKTYPE jumper is not used
- 3-wire serial link to control ADC functionality via RS232
- 2.54 mm pitch connectors for the digital outputs, compatible with high speed acquisition system probes
- Banana jacks for the power supply accesses and the die junction temperature monitoring functions (2 mm)
- Potentiometers for the DMUX functions

The board is composed of eight metal layers for signal traces, ground and power supply layers, and seven dielectric layers featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain.

The board dimensions are 220 mm x 240 mm.

The board comes fully assembled and tested, with one version of the EV10AS150A ADC installed.

Figure 1-1. ADC EV10AS150A-EB Evaluation Board Simplified Schematic



As shown in Figure 1-1, different power supplies are required:

- V_{CCA5} = 5.0V analog positive power supply
- V_{CCA3} = 3.3V analog positive power supply
- V_{CCD} = 3.3V digital positive power supply
- V_{PLUSD} = 2.5V digital output power supply
- 3.3V power supply for the board functions

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Section 2
Hardware Description

2.1 Board Structure

In order to achieve optimum full speed operation of the ADC EV10AS150A with 1:2/4 DMUX, a multilayer board structure was retained for the evaluation board. Eight copper layers are used, respectively dedicated to the signal traces, ground planes, power supply planes and DC signals traces.

The board is made in RO4003 200 µm and FR4 HTG epoxy dielectric materials. Table 2-1 gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 µm AC signals traces = 50Ω microstrip lines DC signals traces (DMUX functionality etc.)
Layer 2 RO4003 dielectric layer (Hydrocarbon/wovenglass)	Layer thickness = 200 µm Dielectric constant = 3.4 at 10 GHz –0.044 dB/inch insertion loss at 2.5 GHz –0.318 dB/inch insertion loss at 18 GHz
Layer 3 Copper layer	Copper thickness = 35 µm Upper ground plane = reference plane 50Ω microstrip return
Layer 4 FR4 HTG/dielectric layer	Layer thickness = 170 µm
Layer 5 Copper layer	Copper thickness = 35 µm Power planes = V_{CCA5}
Layer 6 FR4 HTG/dielectric layer	Layer thickness = 200 µm
Layer 7 Copper layer	Copper thickness = 35 µm Power planes = V_{CCD} and 3.3V
Layer 8 FR4 HTG/dielectric layer	Layer thickness = 170 µm

Table 2-1. Board Layer Thickness Profile (Continued)

Layer 9 Copper layer	Copper thickness = 35 µm Power planes = V_{CCA3}
Layer 10 FR4 HTG/dielectric layer	Layer thickness = 200 µm
Layer 11 Copper layer	Copper thickness = 35 µm Power planes = V_{PLUSD}
Layer 12 FR4 HTG/dielectric layer	Layer thickness = 170 µm
Layer 13 Copper layer	Copper thickness = 35 µm Ground plane = reference plane (identical to layer 3)
Layer 14 FR4 HTG/dielectric layer	Layer thickness = 200 µm
Layer 15 Copper layer	Copper thickness = 40 µm DC signals traces and Serial Interface (AVR) signals Ground plane

The board is 1.6 mm thick.

The clock, analog input, reset and digital data output signals occupy the top metal layer while the ADC and DMUX functions are located both on the top.

The ground planes occupy layer 3, 13 and 15 (partly).

Layer 5, 7, 9 and 11 are dedicated to the power supplies.

2.2 Analog Inputs/Clock Input

The differential active inputs (Clock, Analog) are provided by SMA connectors.

Reference: VITELEC 142-0701-8511

Special care was taken for the routing of the analog input and clock input signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between V_{IN} and V_{INN} and between CLK and CLKN
- 50 mm max line length
- 1.27 mm pitch between the differential traces
- 400 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the V_{IN}, V_{INN}, CLK and CLKN ball footprints

Figure 2-1. Figure 2-1.Board Layout for the Differential Analog and Clock Inputs

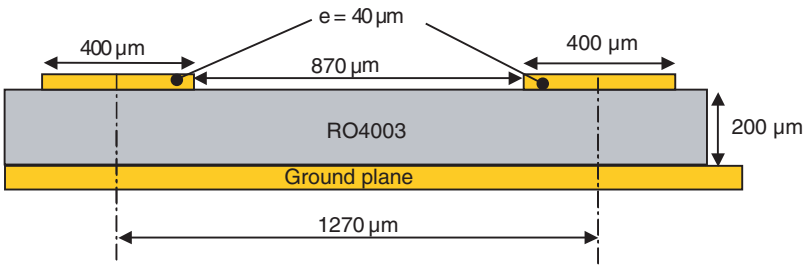


Figure 2-2. Differential Analog Inputs Implementation

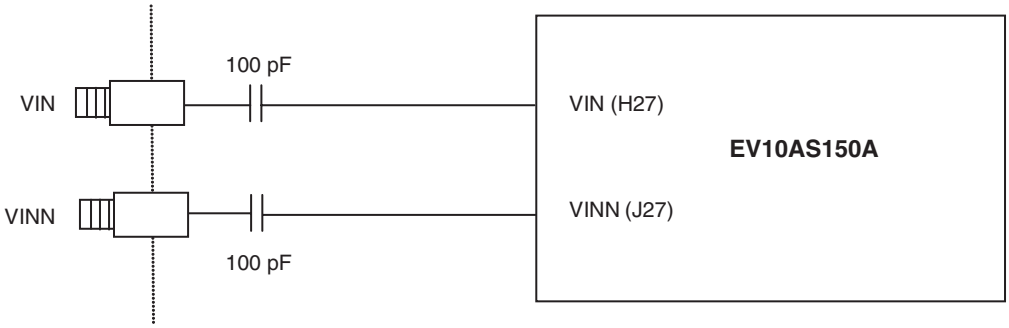
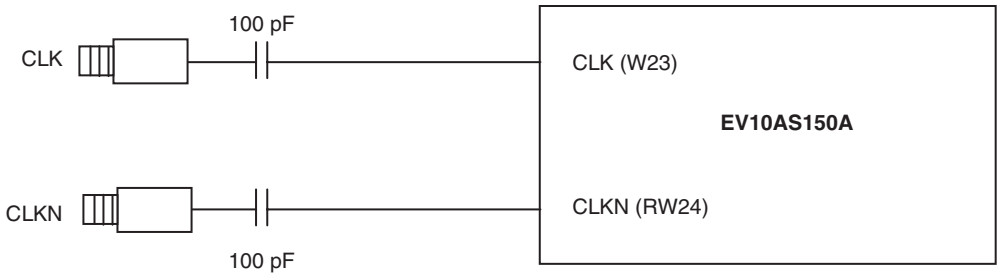


Figure 2-3. Differential Clock Inputs Implementation

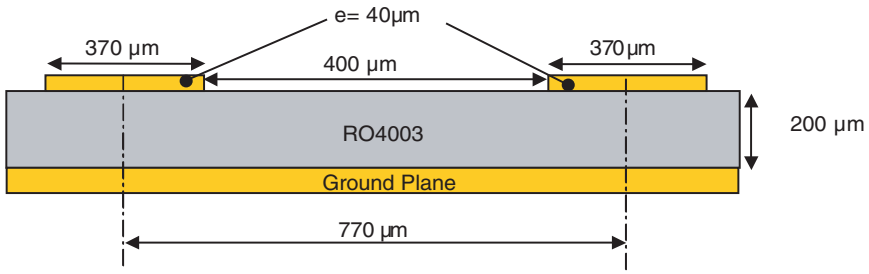


2.3 Digital Output

The digital output lines were designed with the following recommendations:

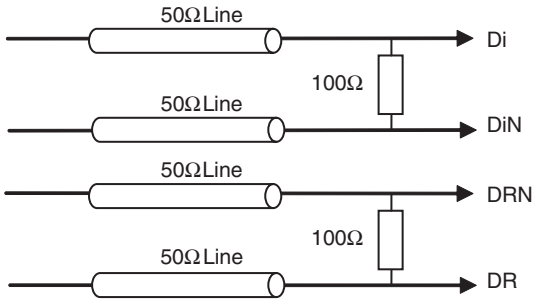
- 50Ω lines matched to ±0.5 mm (in length) between signal of the same differential pair
- 80 mm max line length
- ±1 mm line length difference between signals of two ports
- ±1.5 mm max line length difference between all signals
- 770 µm pitch between the differential traces
- 370 µm line width
- 40 µm thickness

Figure 2-4. Board Layout for the Differential Digital Outputs



The digital outputs are compatible with LVDS standard. They are on-board 100Ω differentially terminated as described in Figure 2-5.

Figure 2-5. Differential digital Outputs Implementation



HE14 Double row 2.54 mm pitch connectors are used for the digital output data. The upper row is connected to the signal while the lower row is connected to Ground, as illustrated in Figure 2-6.

Figure 2-6. Differential Digital Outputs 2.54 mm Pitch Connector (Example Port A)

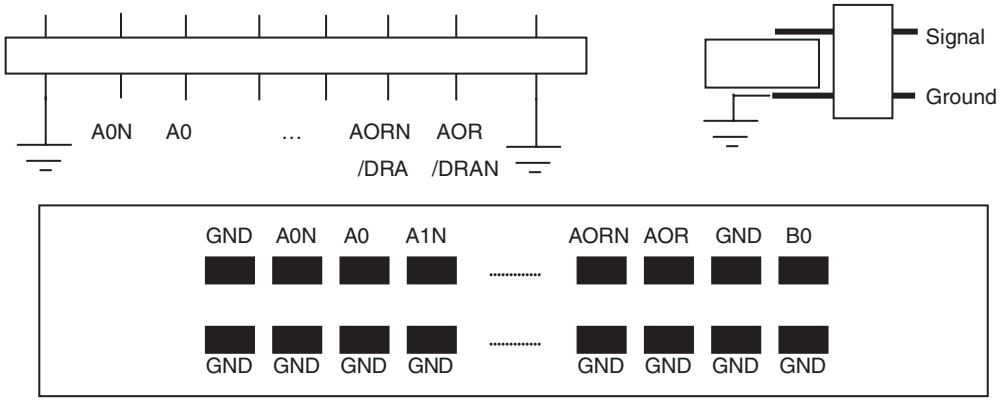


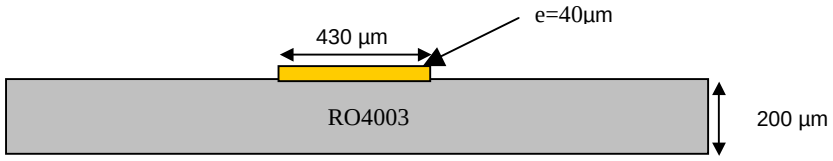
Figure 2-7. Differential Digital Clock Outputs 2.54 Mm Pitch Connector

2.4 Reset Lines

The reset line (DRR and ASYNCRST) were designed with the following recommendations:

- 50Ω lines
- 80 mm max line length
- 430 µm line width
- 40 µm thickness

Figure 2-8. Board Layout for the Single Reset Lines



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Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the ADC EV10AS150A with 1:2/4 DMUX.

The analog input signal can be entered either in differential or single ended. Refer to the datasheet for the impact of driving analog input in single or in differential. The clock input signal must be differentially driven.

ADC EV10AS150 clock inputs should be fed with balanced signals (use a balun or hybrid junction to convert a single signal to a differential signal).

3.2 Operating Procedure

1. Connect the power supplies and ground accesses through the dedicated banana jacks.

V_{CCA5} = 5.0V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V, V_{PLUSD} = 2.5V,
V_{CCA3} = 3.3V, V_{CCD} = 3.3V and 3.3V have separated planes but can be reunited via a short-cable.

2. Connect the clock input signals. Use a low-phase noise high frequency generator.

The clock input level is typically 1dBm (on 100Ω differential input). The clock frequency can range from 500 MHz up to maximum speed.

3. Connect the analog input signal. Use a low-phase noise high frequency generator.

The analog input full scale is 500 mV peak-to-peak (±250 mV on each single ended input) around 0V (AC coupling). It is recommended to use the ADC with an input signal of –1 dBFS max (to avoid saturation of the ADC).
The analog input frequency can range from DC up to 5 GHz. At 5 GHz, the ADC attenuates the input signal by 3 dB.

4. Connect the high-speed acquisition system probes to the output connectors.

The digital data are differentially terminated on-board (100Ω) however, they can be probed either in differential or in single-ended mode.

5. Connect the DMUX function jumpers:

All instrumentation and connectors are now connected.

6. Switch on the power supplies (No specific power supplies sequencing required during power on/off).
7. Turn on the RF clock generator.
8. Turn on the RF signal generator.

9. Perform an asynchronous Reset (DRR active) on the device and maintain this Reset active.
10. Perform an asynchronous Reset ((push button) ASYNCRST active) on the board.
11. Then, ASYNCRST inactive on the board.
12. DRR inactive on the device.
13. Started 3 Wire Serial interface (refer to Section 4)
14. Reset button allows to configure ADC (Mode 0)

3.3 Electrical Characteristics

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Analog 5.0V Power Supply voltage	V_{CCA5}	GND to 6.0	V
Analog 3.3V Power Supply voltage	V_{CCA3}	GND to 3.6	V
Digital 3.3V Power Supply Voltage	V_{CCD}	GND to 3.6	V
Output 2.5V Power Supply voltage	V_{PLUSD}	GND to 3.0	V
Minimum Analog input peak voltage (with differential input)	V_{IN} or V_{INN}	2.0	V
Maximum Analog input peak voltage (with differential input)	V_{IN} or V_{INN}	4.0	V
Maximum difference between V_{IN} and V_{INN} (with differential input)	$\lvert V_{IN} - V_{INN} \rvert$	2.0 (4 Vpp = +13 dBm in 100 Ω)	V
Minimum Analog input peak voltage (with single ended input)	VIN with VINN = 50Ω to GND or VINN with VIN = 50Ω to GND	2.0	V
Maximum Analog input peak voltage (with single ended input)	V_{IN} with V_{INN} = 50Ω to GND or V_{INN} with V_{IN} = 5 Ω to GND	4.0	V
Maximum amplitude on V_{IN} or V_{INN} (with single ended input)	$\lvert V_{IN} \rvert$ or $\lvert V_{INN} \rvert$	(2 Vpp = +10 dBm in 50Ω)	V
Minimum Clock input peak voltage (with differential clock)	V_{CLK} or V_{CLKN}	1.5	V
Maximum Clock input peak voltage (with differential clock)	V_{CLK} or V_{CLKN}	4.0	V
Maximum difference between V_{CLK} and V_{CLKN} (with differential clock)	$\lvert V_{CLK} - V_{CLKN} \rvert$	1.5 (3 Vpp)	V
3WSI input voltage	SDATA, SLDN, SCLK, RESET	–0.3 to V_{CCA3} + 0.3	V
ADC Reset Voltage	DRR	–0.3 to V_{CCA3} + 0.3	V
DMUX function input voltage	RS, DRTYPE, SLEEP, STAGG, BIST	–0.3 to V_{CCD} + 0.3	V
DMUX Asynchronous Reset	ASYNCRST	–0.3 to V_{CCD} + 0.3	V

Table 3-1. Absolute Maximum Ratings (Continued)

DMUX Control Voltage	CLKDACTRL	–0.3 to V_{CCD} + 0.3	V
Maximum input voltage on DIODE	DIODE ADC	700	mV
Maximum input current on DIODE	DIODE ADC	1	mA
Max Junction Temperature	T_J	135	°C
Storage temperature	Tstg	–55 to 150	°C
ESD protection (HBM)		≥500 on ADC inputs 500 on DMUX outputs	V

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
All integrated circuits should be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure, including reliability degradation.

Table 3-2. Electrical Characteristics for Supplies

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
POWER REQUIREMENTS						
Power Supply voltages	1					
Analog 5.0V		V_{CCA5}	4.75	5.0	5.15	V
Analog 3.3V		V_{CCA3}	3.15	3.3	3.45	V
Digital 3.3V		V_{CCD}	3.15	3.3	3.45	V
Output 2.5V		V_{PLUSD}	2.4	2.5	2.6	V
Power Supply current in 1:2 DMUX	1					
Analog V_{CCA5} = 5.0V		I_{VCCA5}		160	205	mA
Analog V_{CCA3} = 3.3V		I_{VCCA3}		840	990	mA
Digital V_{CCD} = 3.3V		I_{VCCD}		400	500	mA
Output V_{PLUSD} = 2.5V		I_{VPLUSD}		420	580	mA
Power Supply current in 1:4 DMUX	1					
Analog V_{CCA5} = 5.0V		I_{VCCA5}		160	205	mA
Analog V_{CCA3} = 3.3V		I_{VCCA3}		840	990	mA
Digital V_{CCD} = 3.3V		I_{VCCD}		450	575	mA
Output V_{PLUSD} = 2.5V		I_{VPLUSD}		450	620	mA
Power Supply current in NAP and SLEEP mode	1					
Analog V_{CCA5} = 5.0V		I_{VCCA5}		140	180	mA
Analog V_{CCA3} = 3.3V		I_{VCCA3}		590	880	mA
Digital V_{CCD} = 3.3V		I_{VCCD}		145	170	mA
Output V_{PLUSD} = 2.5V		I_{VPLUSD}		390	535	mA
Power dissipation	1	P_D				
- 1:2 DMUX				5.9	7.7	W
- 1:4 DMUX				6.2	8.1	W
- NAP & SLEEP mode (1:4 or 1:2)				4.2	5.9	W

3.4 Digital Output Coding

Table 3-3. Digital Output Coding

Differential Analog Input	**Voltage Level**	**Digital Output**		
		Natural Binary[1] MSB…….LSB OR	Binary 2's Complement[1] MSB…….LSB OR	Gray Coding[1] MSB……..LSB OR
> 250.25 mV	>Top end of full scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 1	0 1 1 1 1 1 1 1 1 1 1
250.25 mV	Top end of full scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 0
249.75 mV	Top end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 1	0 1 1 1 1 1 1 1 1 1 0
125.25 mV	$^3/_4$ full scale + ½ LSB	0 0 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1 1 1 1	0 1 0 1 1 1 1 1 1 1 0
124.75 mV	$^3/_4$ full scale - ½ LSB	0 1 0 0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 1 1 0
0.25 mV	Mid scale + ½ LSB	0 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1 0
–0.25 mV	Mid scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 0
–124.75 mV	$^1/_4$ full scale + ½ LSB	1 0 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1 1	1 0 0 1 1 1 1 1 1 1 0
–124.25 mV	$^1/_4$ full scale - ½ LSB	1 1 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0	1 1 0 1 1 1 1 1 1 1 0
–249.75 mV	Bottom end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 0 0	0 1 1 1 1 1 1 1 1 0 0	1 1 1 1 1 1 1 1 1 0 0
–250.25 mV	Bottom end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1 1 1 0
<–250.25 mV	< Bottom end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1

MSB bit 9 and LSB bit 0.

Notes: 1. Refer to chap. 4.4.4 and 4.4.5 for selection between natural binary, binary 2's complement or Gray coding.
2. Be aware that code 0x000 is obtained for positive full scale analog input and code 0x3FF for negative full scale analog input.

Section 4

Software Tools

4.1 Overview

The ADC EV10AS150A evaluation user interface software is a C++ compiled graphical interface.

No license is required to run on a W98, NT, W2000 and XP PC.

The software uses intuitive push buttons and popup menus to write data from the hardware.

4.2 Configuration

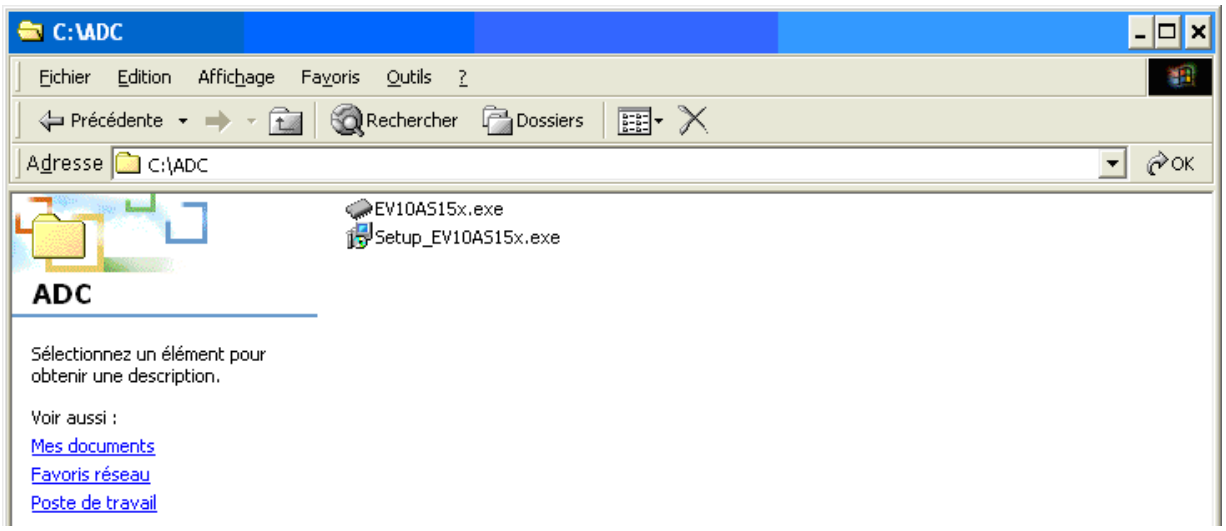
Advised configuration for Win2000:

- PC Pentium >100 MHz
- Memory 24Mo
- For other versions of Windows OS, use the recommended configuration from Microsoft
- Two COM ports are necessary to use two boards simultaneously

4.3 Getting Started

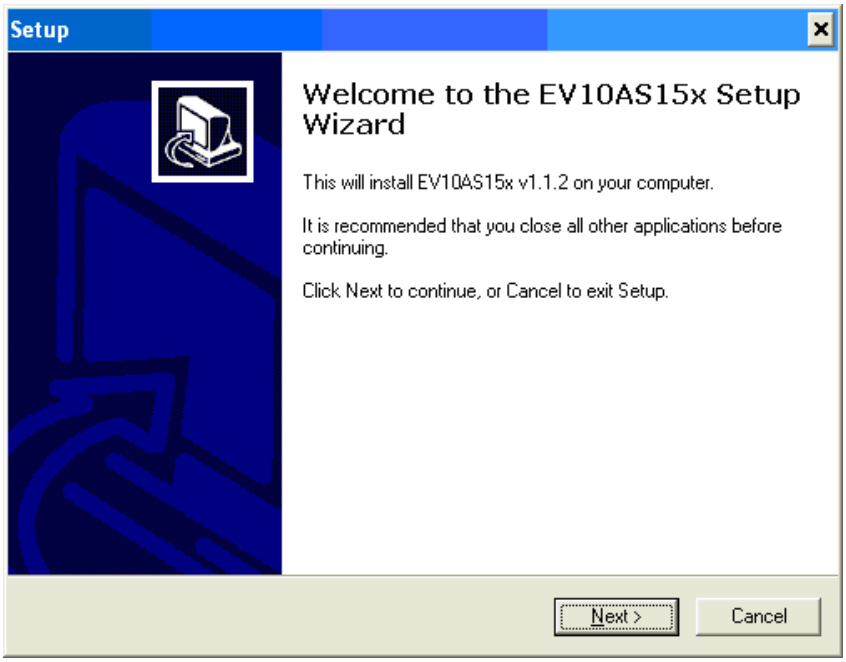
Install the ADC EV10AS15x application on your computer by launching the EV10AS15x exe installer.

Figure 4-1. Install Window



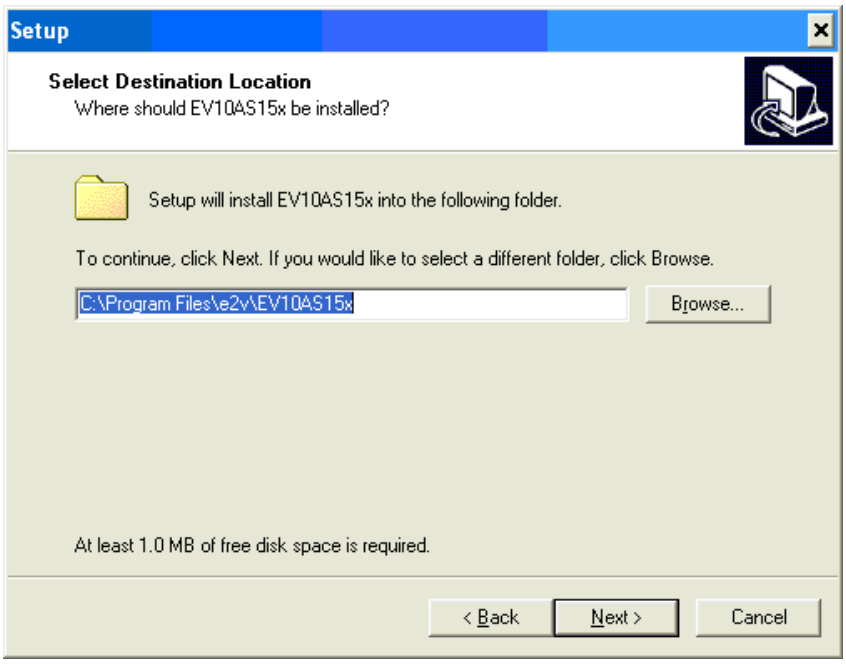
Start the Setup_EV10AS15x (v1.1.2)

Figure 4-2. EV10AS150A Application Set up Wizard Window



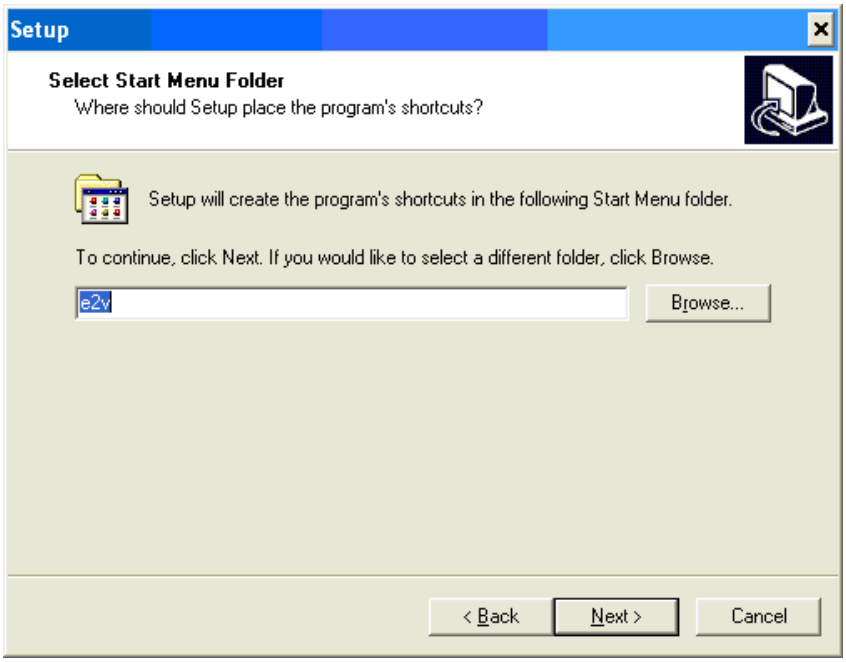
Next step: Select Destination Directory.

Figure 4-3. EV10AS150A select Destination Directory Window



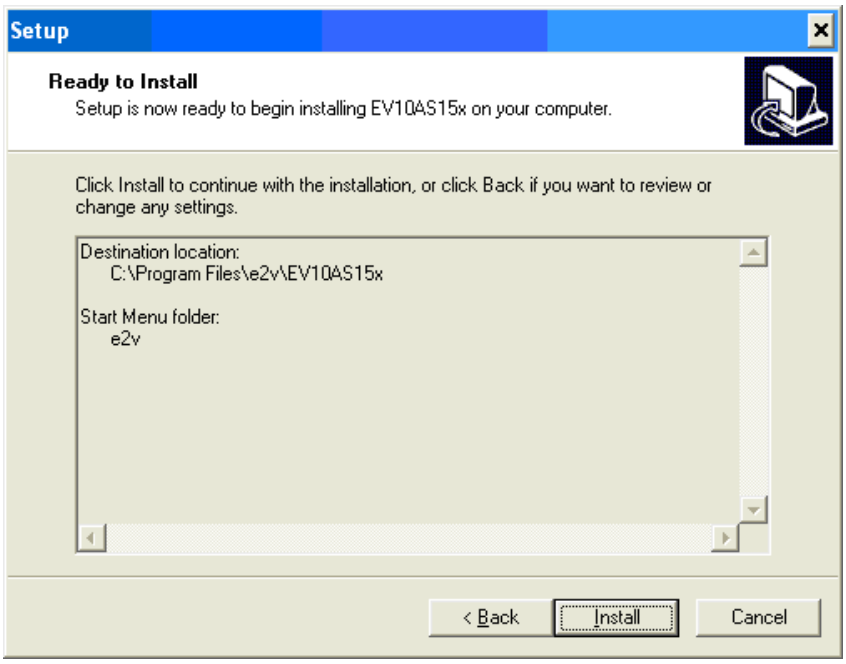
Next step: Start Menu Folder.

Figure 4-4. EV10AS150A select Start Menu Window



Next step: verification of the install configuration.

Figure 4-5. EV10AS150A Ready to Install Window

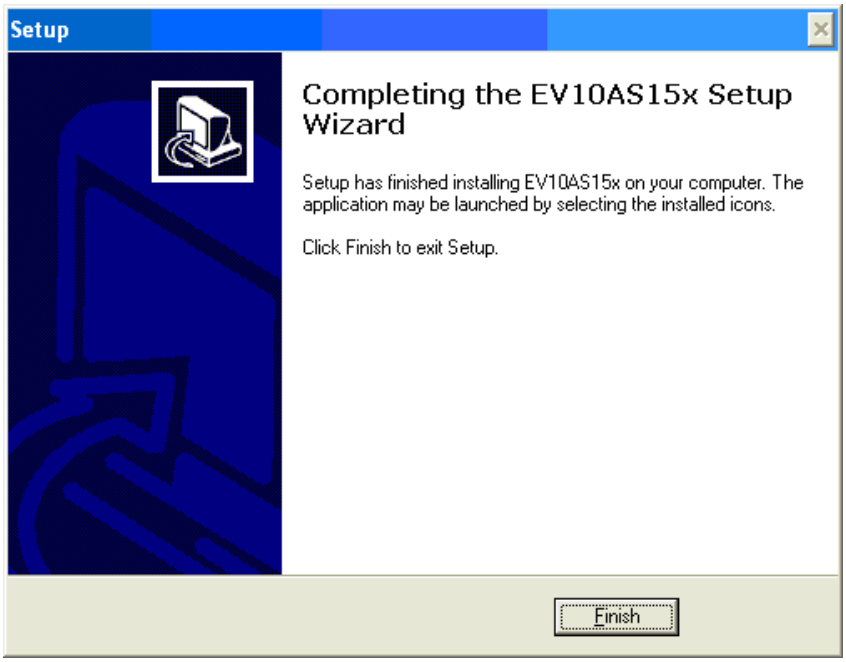


If you agree with the install configuration press *Install.*

Figure 4-6. EV10AS150A Application Setup Install Push Button

The software is completing installation.

Figure 4-7. EV10AS150A Completing Setup Wizard Window



Now you can launch the ADC10Bit series software from its icon; the following screen will be displayed:

Figure 4-8. ADC EV10AS150A User Interface Window

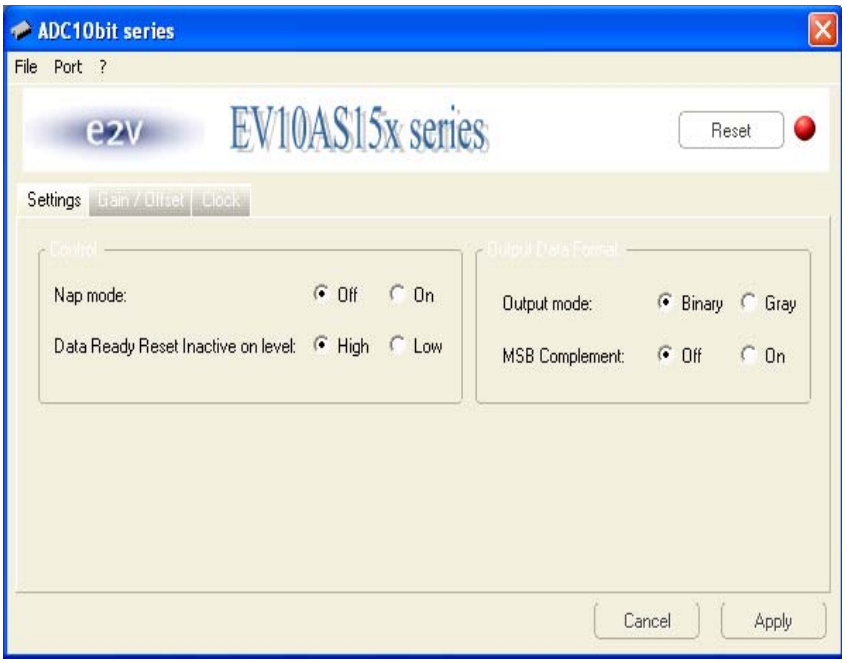
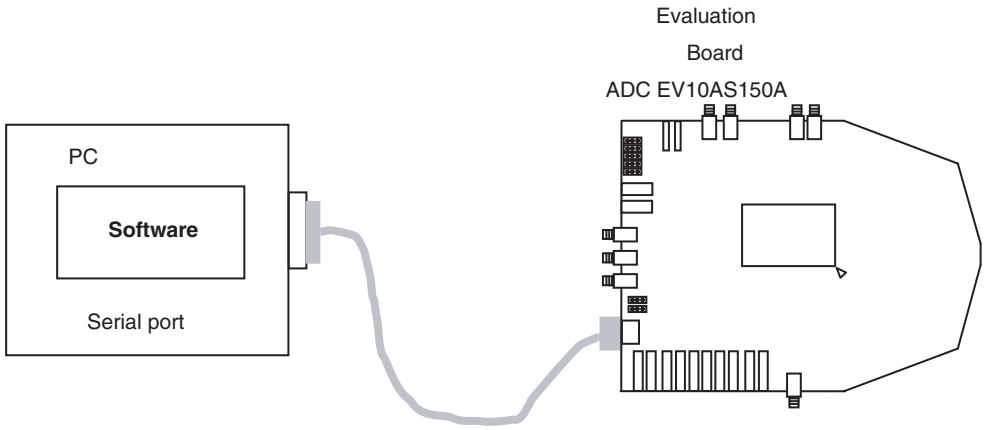


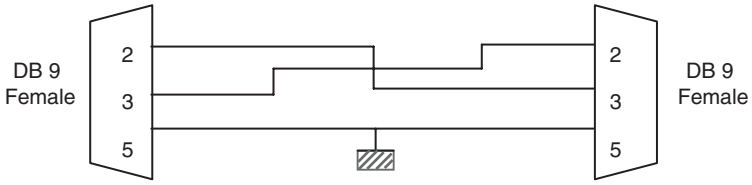
Figure 4-9. ADC10-bit User Interface Hardware Implementation



Use a RS 232 port to send data to ADC.

Connect the crossed DB9 9 (F/F) cable between your PC and your evaluation board.

Figure 4-10. Crossed RS232 Cable



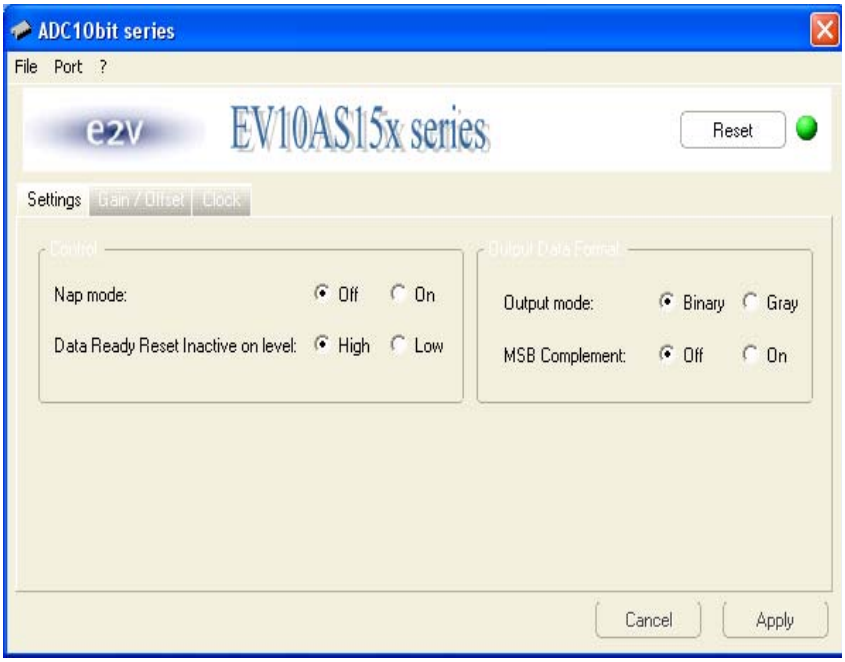
Serial Port Configuration:

- Bit rate: 19200
- Data coding: 8 bit
- 1 start bit, 1 Stop bit
- No parity check

4.3.1 Installation Software

At startup, the application automatically checks all RS 232 ports available on the computer and tries to find the evaluation board on them.

Figure 4-11. ADC EV10AS150A User Interface



The *Port* menu shows all available ports on your computer. The port currently used has a check mark on its left. By clicking another port item, the application will try to connect to an evaluation board via the selected port. If a board is successfully detected on the new port, the LED is green (or orange depending on the serial interface switch) and the new port gets the check mark. If the application is not able to find a board on this port, an error message is displayed and the LED turns to red.

4.3.2 Troubleshooting

If the ADC EV10AS150A evaluation board is not connected or not powered, a red LED appears on the right of the Reset button and the application is grayed

Figure 4-12. ADC EV10AS150A User Interface

Check the connection to the PC and restart the application.

If the serial interface is not active the LED appears in orange and the application is grayed too.

Figure 4-13. ADC EV10AS150A User Interface

Turn ON the switch on the demo board, the application should become available and the LED turns to green.

Troubleshooting:

- Check your rights to write in the directory
- Check for the available disk space
- Check that at least one RS232 serial port is free and properly configured.
- Check that the DB9 connector is properly inserted
- Check that all supplies are ON
- Check that the serial mode is active (green LED ON)

4.4 Operating Modes

4.4.1 Overview

The software provides a graphical user interface to configure the ADC.

Push buttons, popup menus and capture windows allows playing with:

- Control Mode,
- Switch analog and Switch clock
- Standby
- Gain
- Offset
- DDA

Always click on *Apply* to validate any command

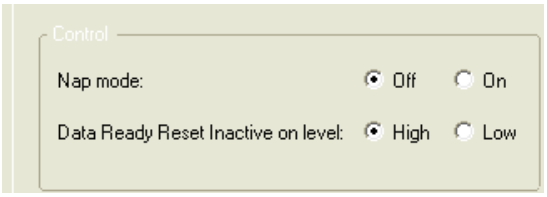
Each setting must be validated in its own tab.

Clicking on *Cancel* will restore last settings sent with *Apply* button.

Reset button allows to configure ADC (Mode 0)

4.4.2 Control Mode

The control mode allows controlling the NAP mode and Data Ready Reset Inactive mode.

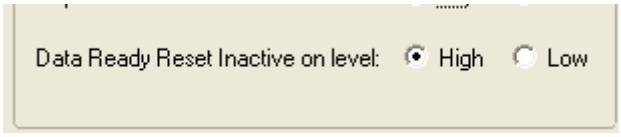


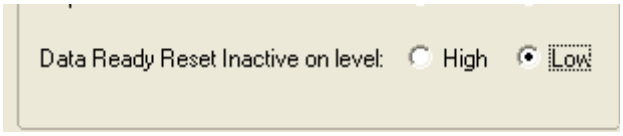
4.4.2.1 NAP Mode

NAP mode configurable Off or On

4.4.2.2 Data Ready Reset Inactive on Level

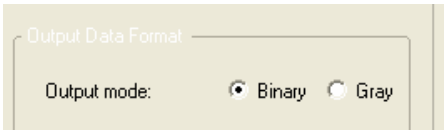
Data Ready Reset is inactive on High level or on Low level





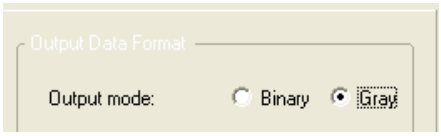
4.4.3 ADC Output Data Format (Binary-Gray)

ADC Output Data Format: Binary



ADC Output Data Format: Gray

Note: In this mode, MSB complement is not available.

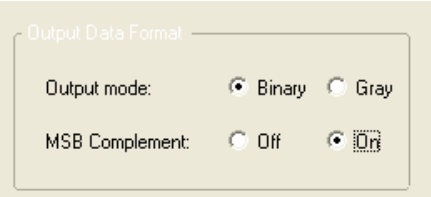


4.4.4 ADC Output Data Format (MSB Complement)

ADC Output Data Format: MSB complement Off

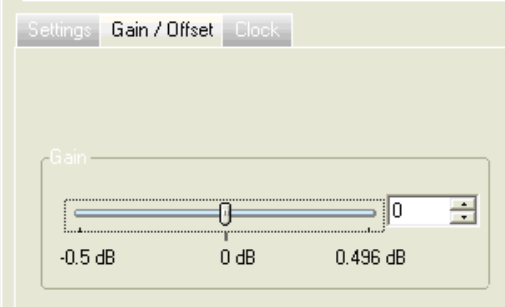
ADC Output Data Format: MSB complement On

Note: Mode MSB complement is available if ADC output data format is binary



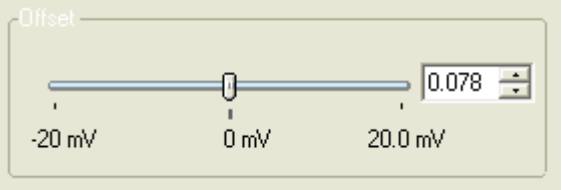
4.4.5 ADC Gain Adjust

ADC Gain adjustment is from –0.5 to 0.5 dB.



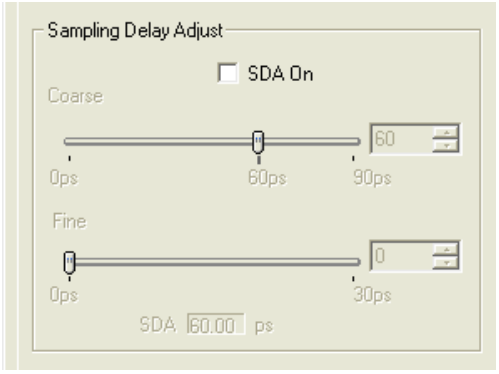
4.4.6 ADC Offset Adjust

ADC Offset adjustment is from –20 mV to 20 mV.

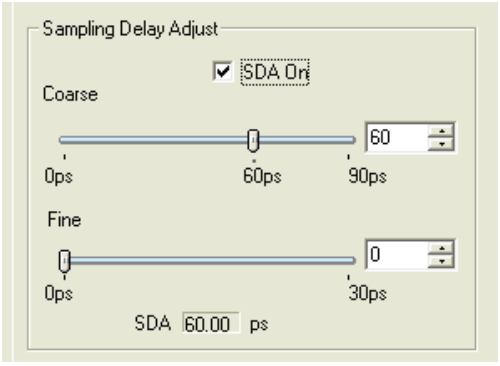


4.4.7 Sampling Delay Adjust

Sampling Delay Adjustment Off

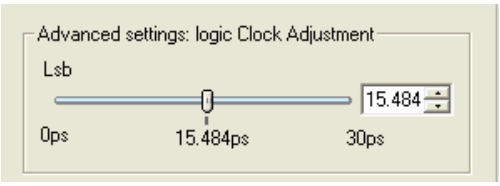


- Sampling delay adjustment On
- Coarse adjustment: 0 to 90 ps by step of 30 ps
- Fine adjustment: 0 to 30 ps by step of 0.118 ps
- Maximum delay: 120 ps



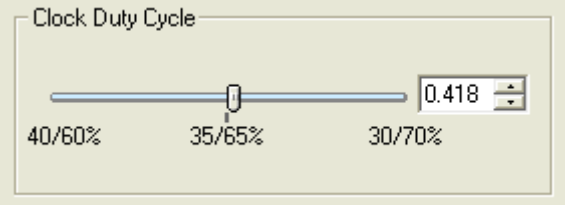
4.4.8 Advanced Setting: Logic Clock Adjustment

Internal logic clock adjustment 0 to 30 ps on Lsb register



4.4.9 Clock Duty Cycle (Track - Hold)

ADC Duty Cycle (Track-Hold): 40%-60% to 30%-70%



Note: Reset value 35%-65%

Section 5
Application Information

5.1 Introduction

For this section, refer also to the product chapter 4 of the datasheet.

5.2 Analog Inputs

The analog input can be entered either single ended or differentially. Refer to the datasheet to see the impact on dynamic performances.

It is recommended to use a filter to optimize the dynamic performance and the spectral response of the ADC.

5.3 Clock Inputs

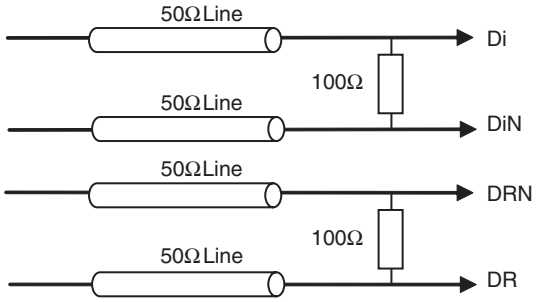
The clock inputs should be differentially driven using a balun or hybrid junction.

The clock input is AC coupled.

5.4 Digital Outputs

The digital outputs (data and Data Ready) are LVDS compatible. 100Ω differential termination is provided on-board.

Figure 5-1. Differential Digital Outputs Implementation



5.5 ADC Functions

5.5.1 DRR (Data Ready Reset)

The Data Ready Reset signal is accessed via an SMA connector.

DRR is CMOS/LVCMOS compatible:

- V_{IL} = 0 (typical)
- V_{IH} = V_{CCA3} (typical)

The active level depends on the Data Ready Reset of 3WSI function (refer to section 4.4.2)

This signal acts as an internal Reset of the device. It is not mandatory for proper operation of the device. It is only used to determine exactly the first data to be sampled.

When applied, the clock outputs are Reset. The Reset pulse should last at least 3.5 ns.

An asynchronous Reset (ASYNCRST push button) should be applied while DRR is active (high) in order to Reset properly the whole device.

In most cases (single channel application, no need to know which data will be the first one to be sampled), this Reset can be left unused.

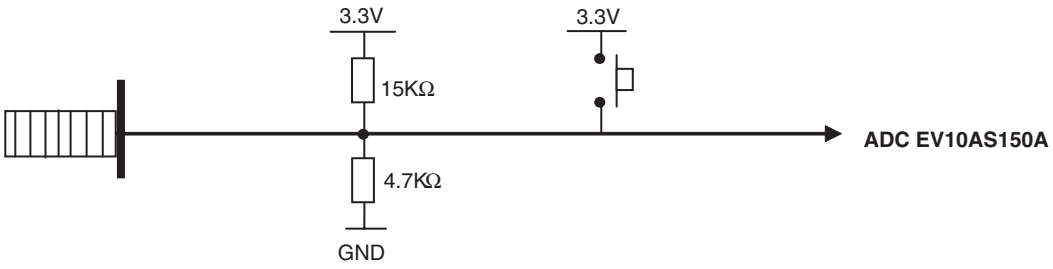
5.6 DMUX Functions

5.6.1 ASYNCRST

The asynchronous Reset is mandatory to start the device properly. It should be applied after power up of the device.

A push button is provided to perform this Reset and pull-up and pull-down resistors allow to keep the ASYNCRST signal inactive.

Figure 5-2. ASYNCRST



If the DRR Reset is also used, it is recommended to apply the asynchronous Reset while the DRR Reset is active.

The first data is available at the device output after TOD + N cycles (with $4.5 \leq N \leq 7.5$ depending on DEMUX mode).

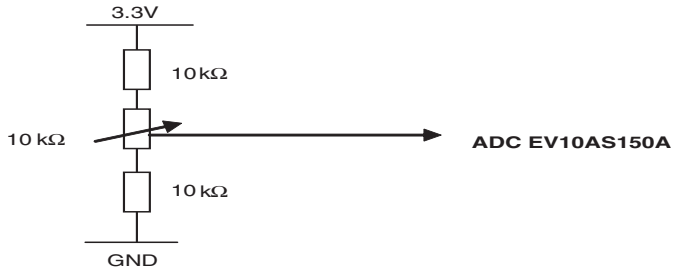
5.6.2 CLKDACTRL

A delay cell is provided to allow the user to tune the delay between the Clock and Data at the DMUX input. The delay is controlled via the CLKDACTRL potentiometer.

This cell allows you to delay the internal DMUX clock via the CLKDACTRL potentiometer (varying from $V_{CCD}/3$ to $(2 \times V_{CCD})/3$).

This pin must be biased and it is recommended to set CLKDACTRL at VCCD/3. With this value it is normally not necessary to tune CLKDACTRL voltage over the full specified clock rate.

Figure 5-3. CLKDACTRL Potentiometer



5.6.3 RS, DRTYPE, BIST, SLEEP, STAGG

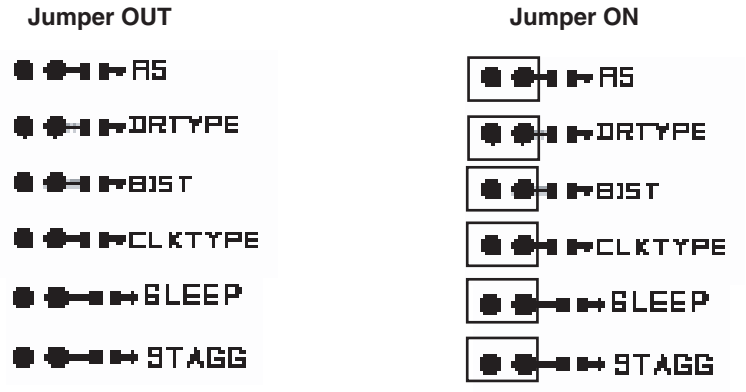
Seven jumpers are provided for the RS, DRTYPE, BIST, SLEEP and STAGG functions.

Table 5-1 describes each function.

Table 5-1. DMUX Function Settings and Description

Function	Description	Jumper Settings
RS	Ratio selection: - 1:2 - 1:4	1:2: Jumper ON 1:4: Jumper OUT
DRTYPE	Output clock mode: - DR = data valid on each rising edge of the DR/DRN signal - DR/2 = data valid on both rising and falling edges of the DR/DRN signal	DR: Jumper OUT DR/2: Jumper ON
BIST	Built-In Self Test: - Active: checker board pattern available at the device outputs - BIST inactive: normal mode	BIST: Jumper ON No BIST: Jumper OUT
SLEEP	Sleep mode - Active: the device is in a partial standby mode - SLEEP inactive: normal mode	SLEEP: Jumper ON SLEEP inactive: Jumper OUT
STAGG	Simultaneous or Staggered output mode - STAGG active: staggered output data - STAGG inactive: simultaneous output data	STAGG: Jumper ON STAGG inactive: Jumper OUT

Figure 5-4. DMUX Functions Jumper Positions



Jumper CLKTYPE can be placed in any position: it has no effect.

5.6.4 Additional OR Bits

In simultaneous mode, the out-of-range signal of the ADC is demultiplexed by the DMUX and output on all ports as the (AOR/DRAN, AORN/DRA), (BOR/DRBN, BORN/DRB), (COR/DRCN, CORN/DRC) and (DOR/DRDN, DORN/DRD) signals.

These signals can be used to detect if the input of the ADC is above the full scale.

In staggered mode, these signals correspond to the output clock for each port:

DRA, DRAN for Port A (pins A6, B6)

DRB, DRBN for Port B (pins J2, H1)

DRC, DRCN for Port C (pins W5, V5)

DRD, DRDN for Port D (pins W17, V17)

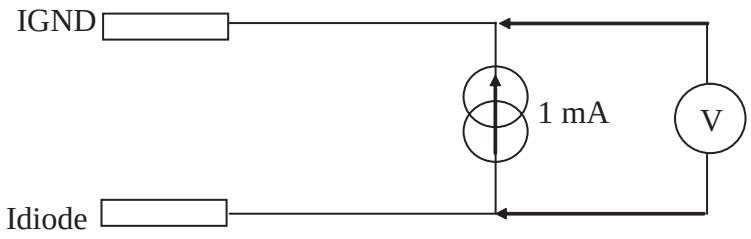
5.7 Diode for Die Junction Temperature Monitoring

Two diodes for die junction temperature measurement are available, for maximum junction temperature monitoring (hot point measurement) of both the ADC and the DMUX.

The measurement method consists in forcing a 1 mA current into a diode mounted transistor.

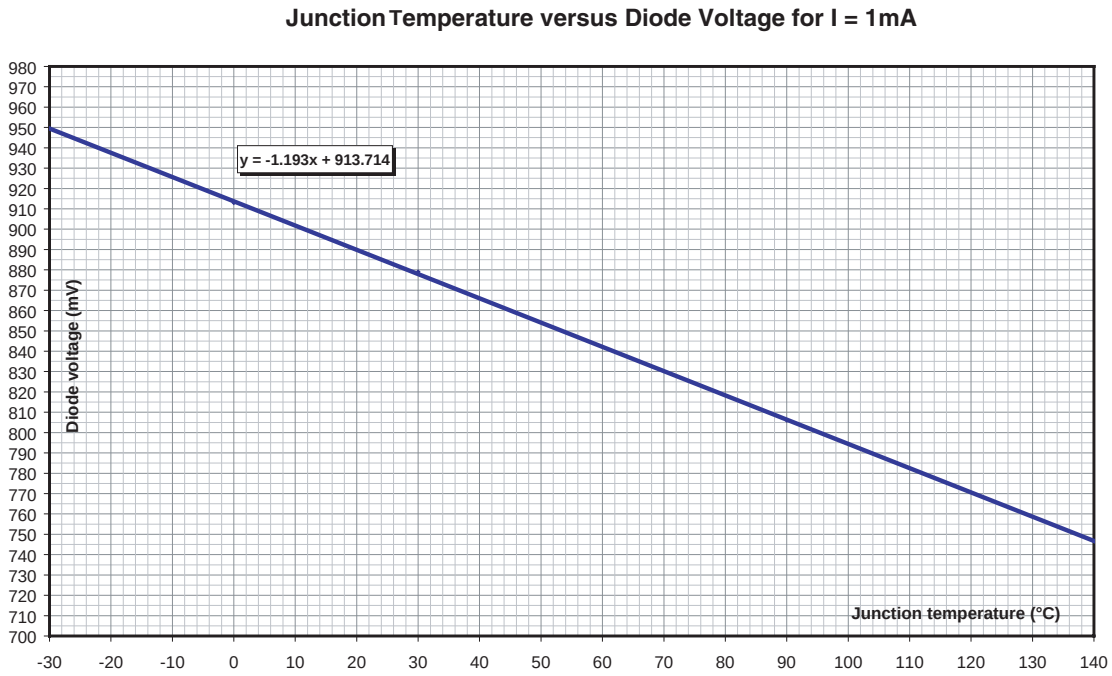
The measurement setup is described in Figure 5-5.

Figure 5-5. ADC DIODE Measurement Setup



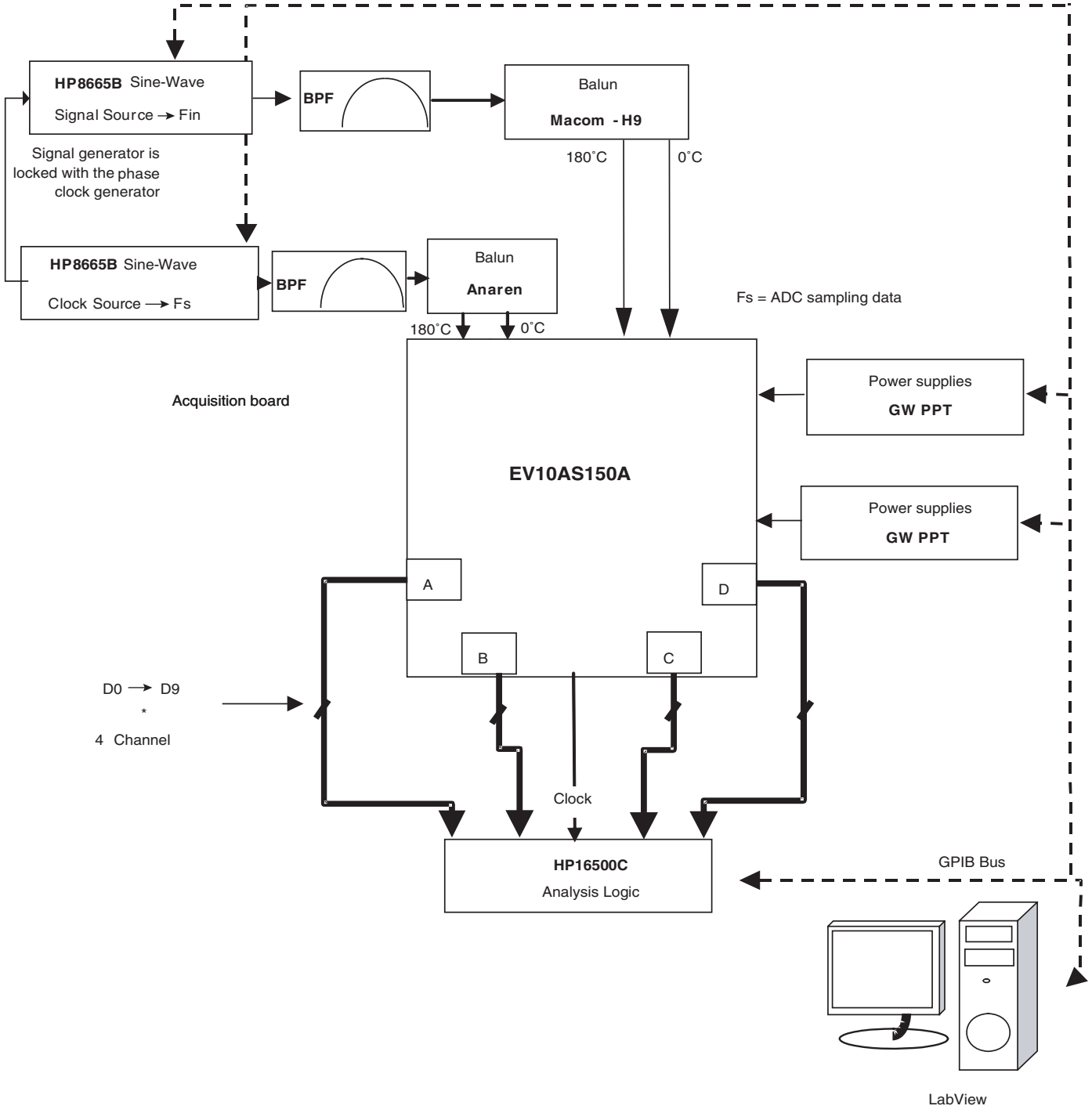
Note: The 1 mA current can be supplied by a multimeter set in this specific current source mode: in this case, the voltage measured between the diode pin and ground is displayed on the multimeter.

Figure 5-6. ADC DIODE Characteristics



5.8 Test Bench Description

Figure 5-7. Test Bench Description



Section 6

Package Information

6.1 Thermal Characteristics

Table 6-1. Thermal Resistance (No air, pure conduction, no radiation)

Thermal Resistance	ADC Alone	DMUX Alone
RTHj-top-of-case	4.11 °C/Watt	1.48 °C/Watt
RTHj-bottom-of-balls	6.94 °C/Watt	3.89 °C/Watt
RTHj-board	7.98 °C/Watt	4.88 °C/Watt
RTHj-ambient	17.13 °C/Watt	13.88 °C/Watt

Note: No external heatsink is mandatory.

Section 7

Ordering Information

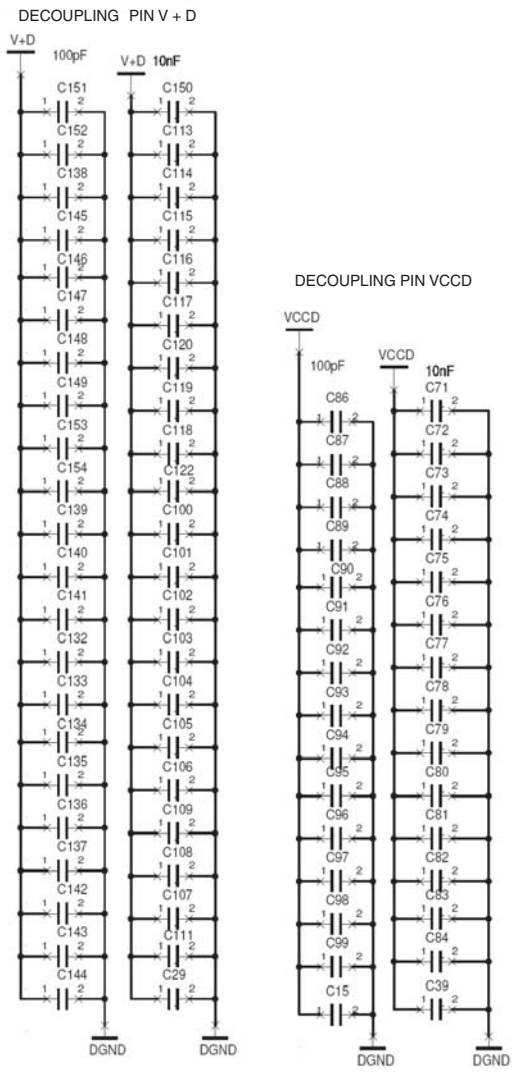
Part Number	Package	Temperature Range	Screening	Comments
EV10AS150ATP-EB	EBGA 317	Ambient	Prototype	For availability, contact your local e2v sales office.
EV10AS150ACTP	EBGA 317	Commercial grade	T_{amb} > 0°C, T_J < 90°C	For availability, contact your local e2v sales office.
EV10AS150AVTP	EBGA 317	Industrial grade	T_{amb} > –40°C, T_J < 110°C	For availability, contact your local e2v sales office.
EV10AS150ACTPY	EBGA 317	Commercial grade RoHS	T_{amb} > 0°C, T_J < 90°C	For availability, contact your local e2v sales office.
EV10AS150AVTPY	EBGA 317	Industrial grade RoHS	T_{amb} > –40°C, T_J < 110°C	For availability, contact your local e2v sales office.

Section 8

Appendix

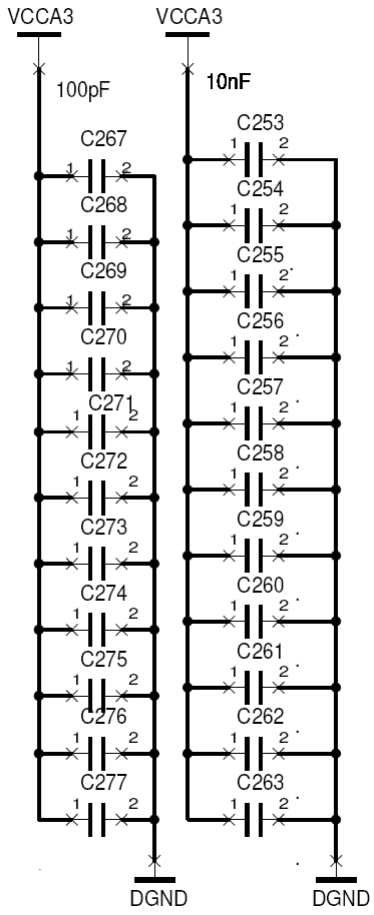
8.1 EV10AS150A-EB Electrical Schematics

Figure 8-1. Decoupling PIN



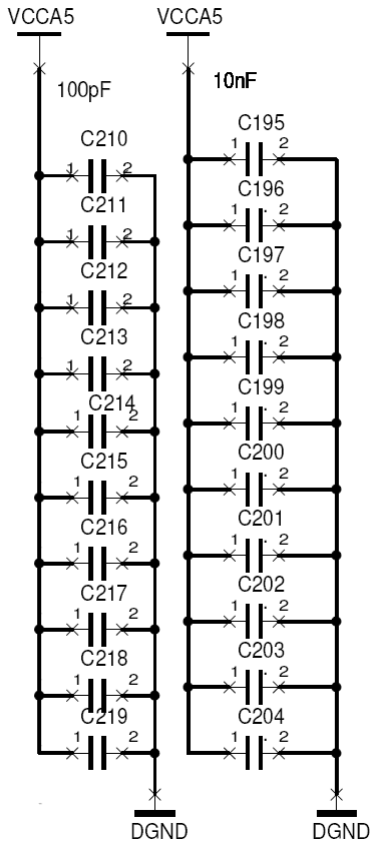
Note: 1. For ADC decoupling strategy, please do not take into account the current decoupling implemented on current evaluation board which is purely experimental. Refer to Datasheet for recommended decoupling strategy.

Figure 8-2. Decoupling PIN V_{CCA3}



Note: 1. For ADC decoupling strategy, please do not take into account the current decoupling implemented on current evaluation board which is purely experimental. Refer to Datasheet for recommended decoupling strategy.

Figure 8-3. Decoupling PIN V_{CCA5}



Note: 1. For ADC decoupling strategy, please do not take into account the current decoupling implemented on current evaluation board which is purely experimental. Refer to Datasheet for recommended decoupling strategy.

Figure 8-4. Power Supplies Connections

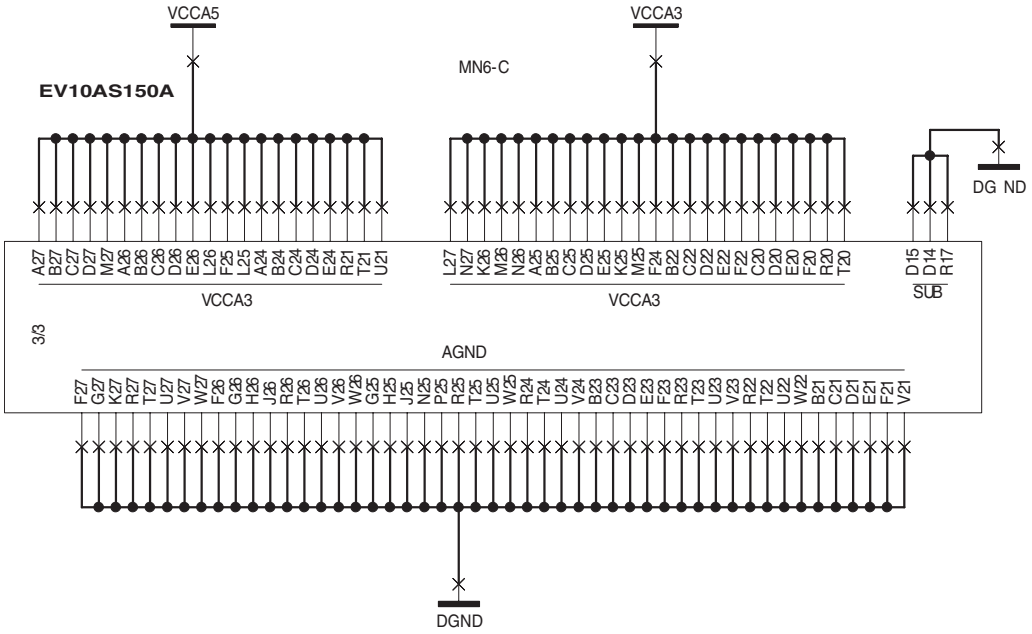


Figure 8-5. Power Supplies Bypassing

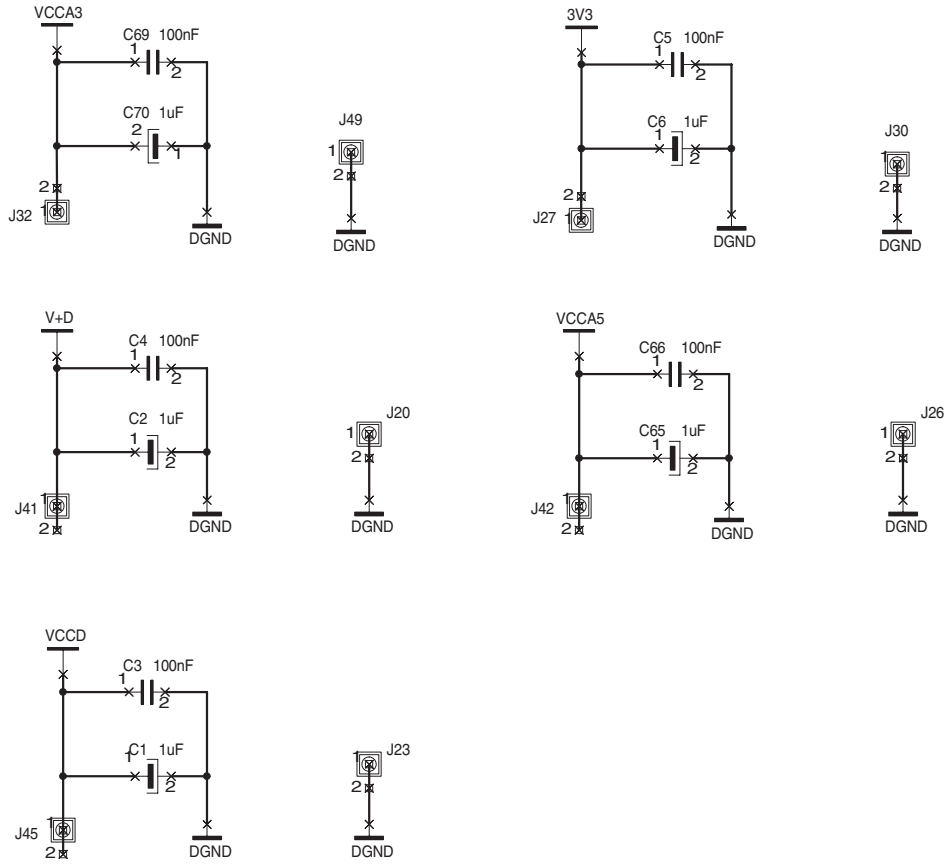


Figure 8-6. EV10AS150A-EB Electrical Schematic (ADC DMUX)

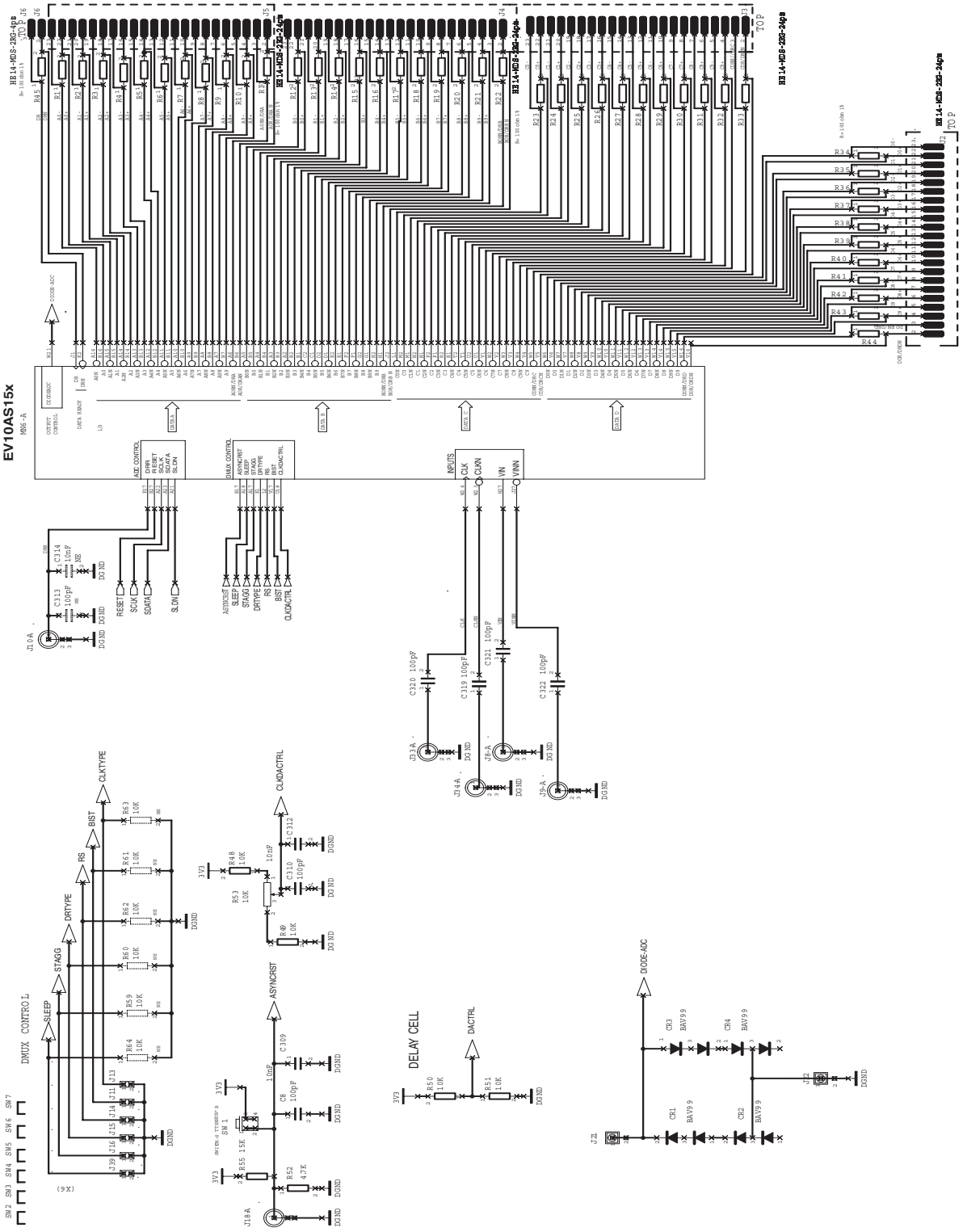
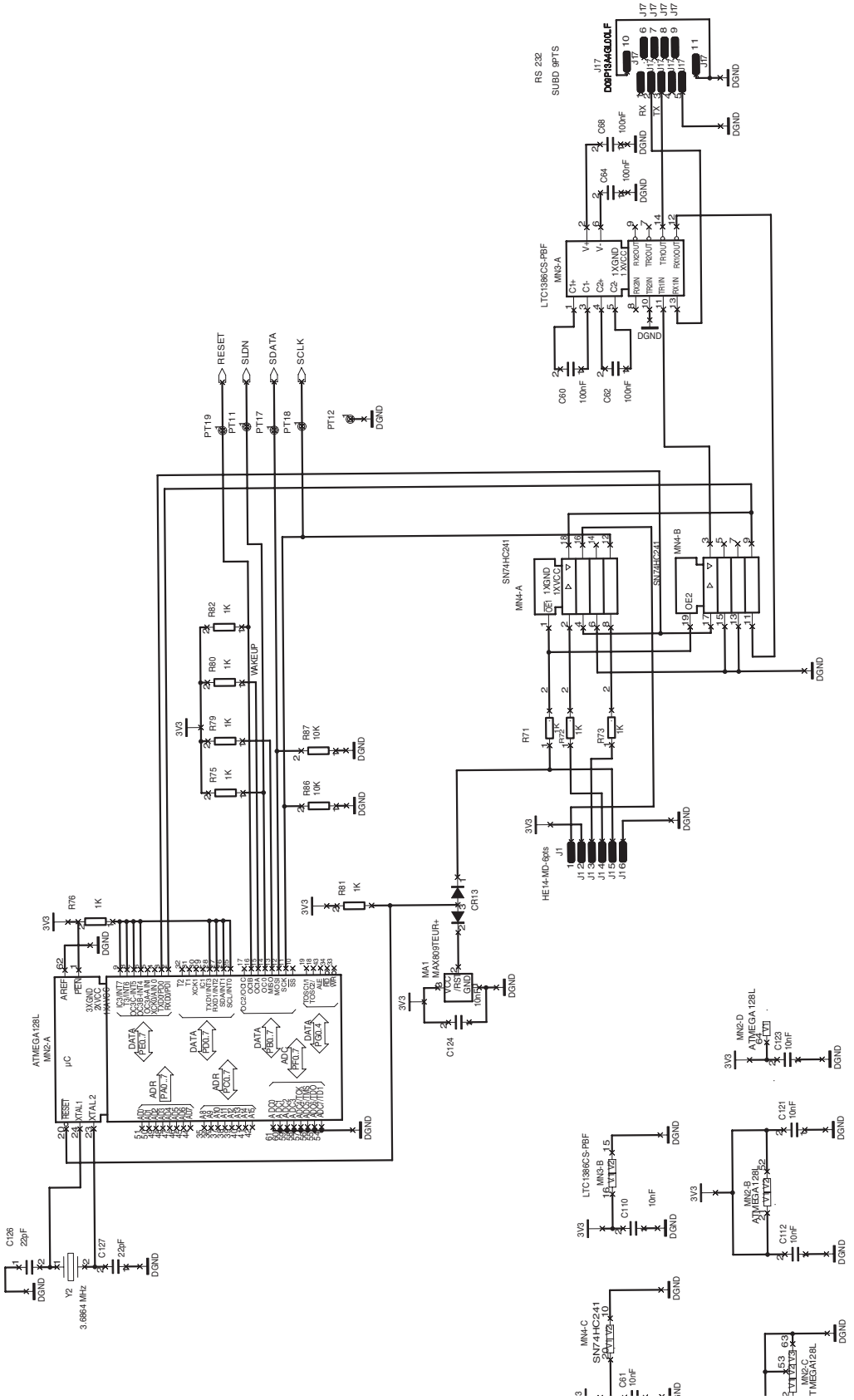


Figure 8-7. EV10AS150A-EB Electrical Schematic (AVR)



8.2 EV10AS150A-EB Board Layers

Figure 8-8. Top Layer

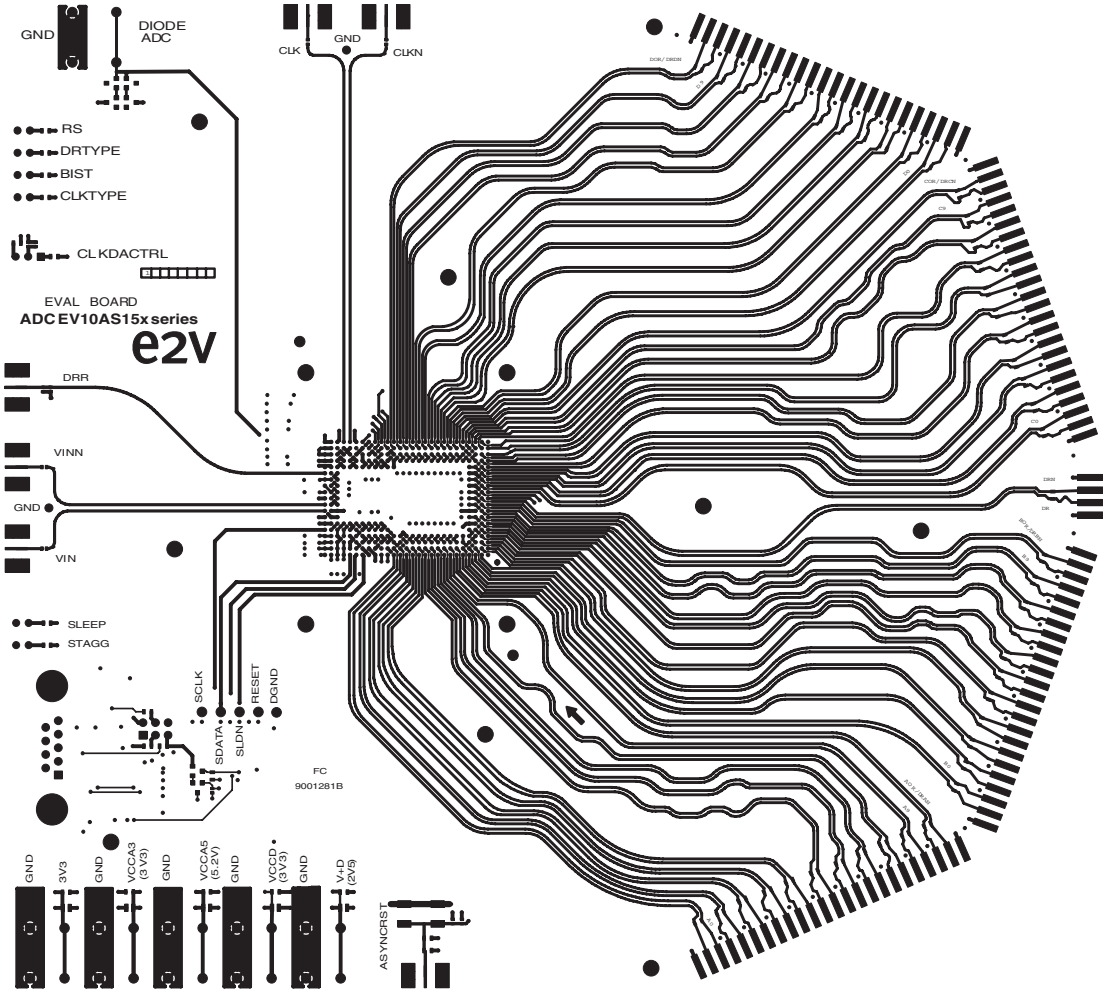


Figure 8-9. Bottom Layer

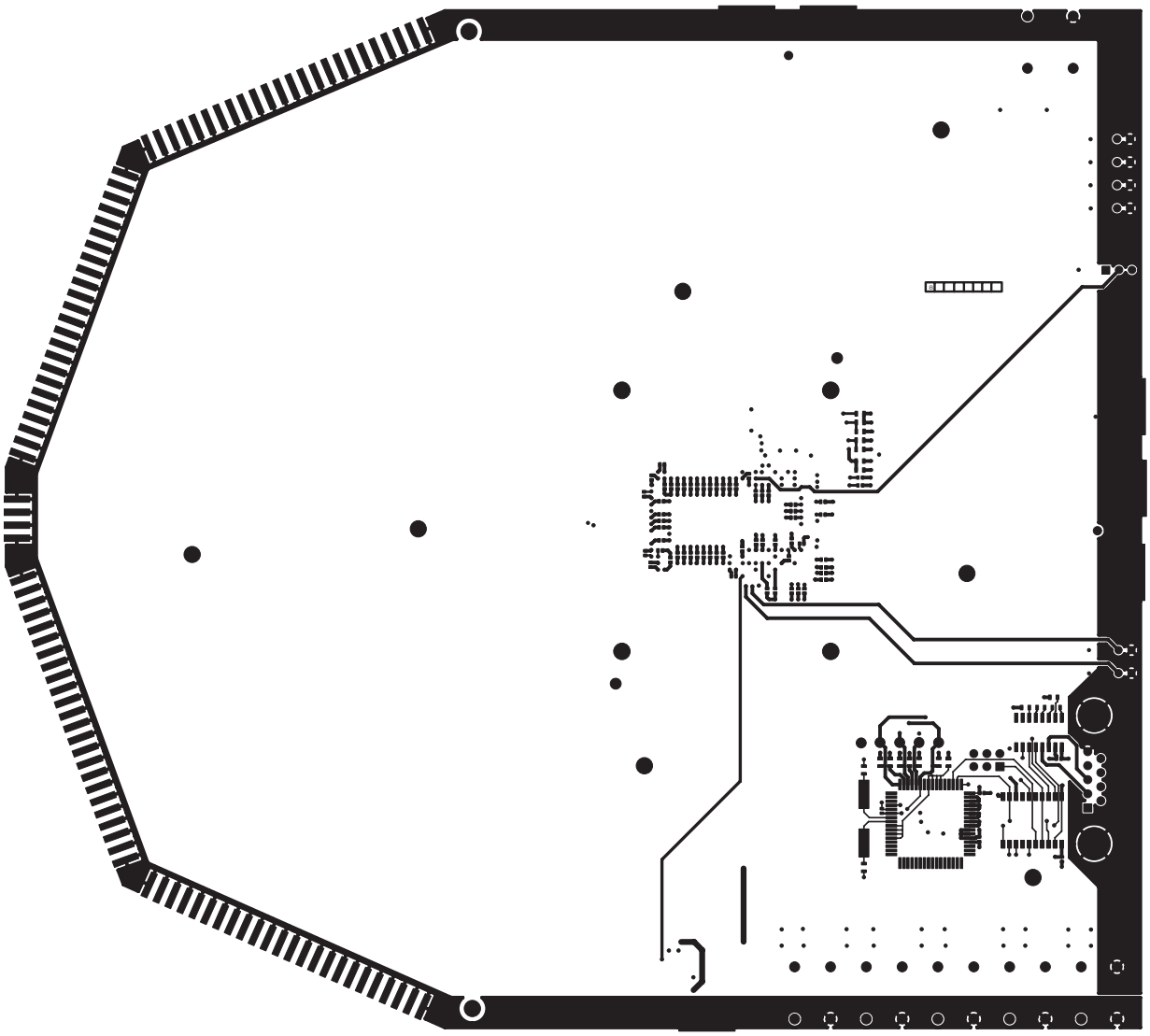


Figure 8-10. Board Equipped with Socket (Top)

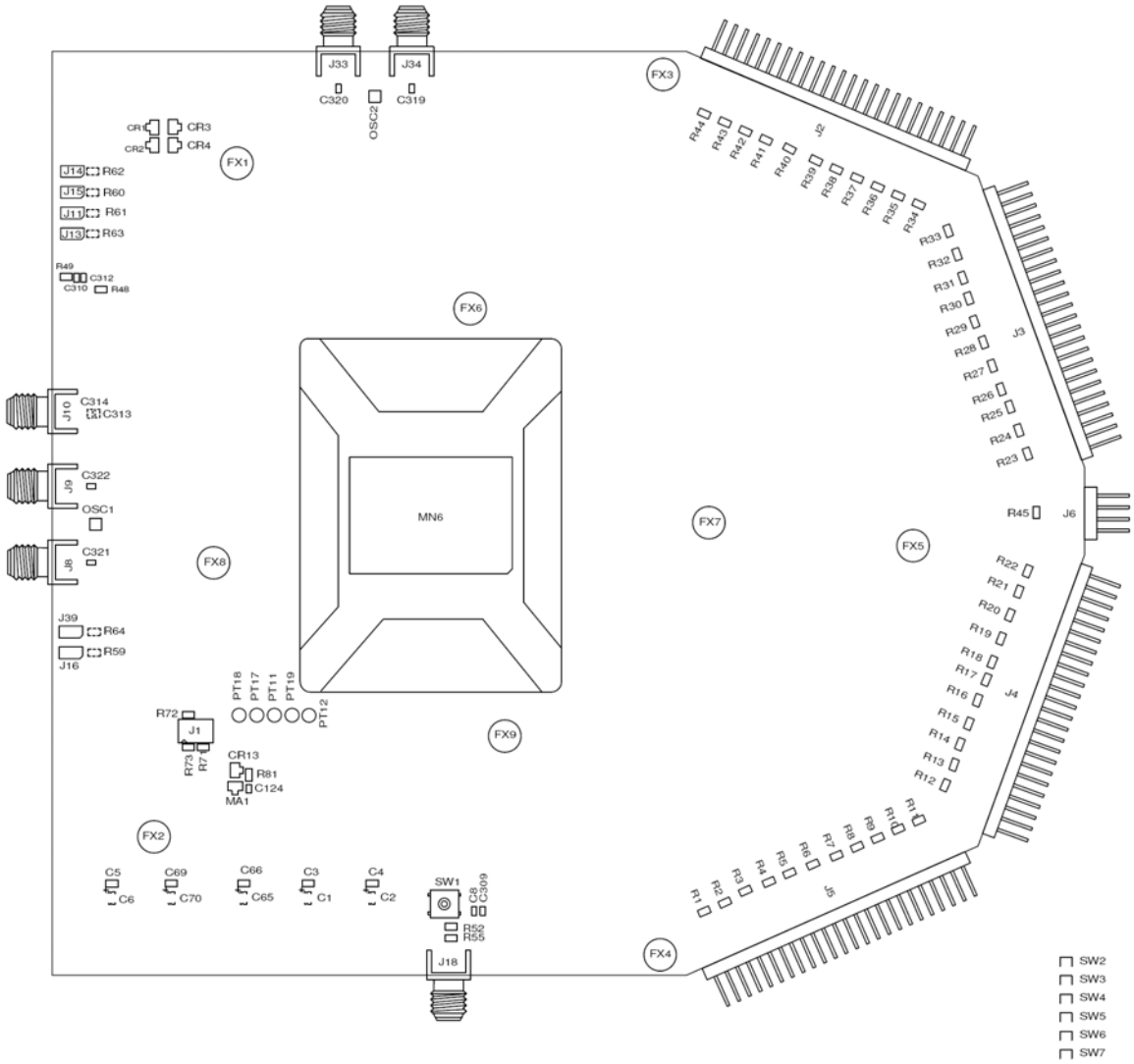
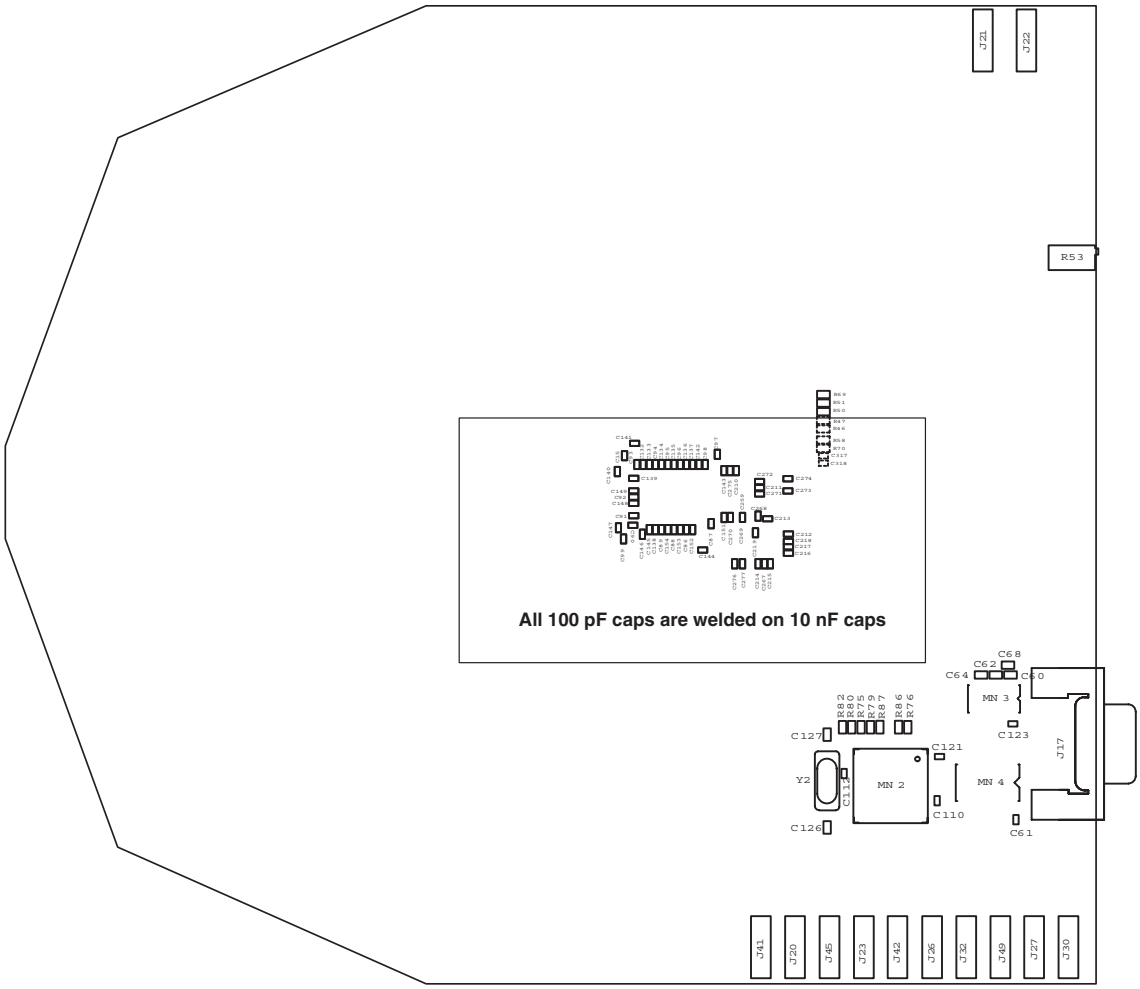


Figure 8-11. Equipped Board (Bottom)



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