TECHNICAL NOTE

TELEDYNE e2v
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March 2019

SYNCHRONIZATION CHAINING, Simplifying Multi-channel Synchronization in Gigahertz Data Converters.

OBJECTIVE

This document explains the relative ease with which deterministic operation of Teledyne-e2v's giga-sample broadband ADCs can be established to facilitate sample synchronization across multiple ADC channels especially in massively parallel sampling systems.
Or more straightforwardly, this is a simple guide to using the SYNC chain functionality.
Information provided is pertinent to systems using digital beam-forming or those used in MIMO antenna systems. This information should be read in conjunction with the product data sheet.

PRODUCT COVERED: EV12AQ600

This discussion focuses on the following pin designations:

- Differential pairs SYNCTRIGP & SYNCTRIGN found at pins 14A/15A
- Differential pairs SYNCOP & SYNCON found at pins 8A/7A

KEY DEFINITIONS

- Deterministic latency: the need for data to propagate through a system with a known and consistent time delay from power cycle to power cycle throughout a system's lifecycle.
- Synchronization: the method to ensure that digital samples are time aligned across multiple signal channels so that signal phase relationships are maintained.
- Metastability: undesirable zone of uncertainty in a digital signals' state that synchronous design deliberately aims to mitigate.

LIST OF FIGURES

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INTRODUCTION

Sample synchronization across multiple ADCs to enable RF, microwave and millimeter-wave beam-steering in complex parallel digital sampling systems relies on preserving temporal precision. With high speed data converters this is a particularly challenging task since timing margins become highly compressed.

Intricate digital sampling systems rely on the complex signal timing relationships brought about by digital system latencies that must be precisely accounted for to ensure sample alignment. Moreover, high speed ADCs are complex systems requiring advanced clocking circuitry (especially frequency dividers) complicating the synchronization job.

This note intends to ease design concerns in respect to achieving synchronization in complex, multi-channel systems. Deterministic operation has often proven a tough task to get right and alternative approaches to achieving it, like JESD204B sub-class 1, have not always left designers with a positive impression given the challenge of getting it to work properly.

A robust and easy to implement method to synchronize timing is thus to be welcomed by designers and is discussed here. At Teledyne-e2v, deterministic synchronization is built around a pair of event driven, differential electrical signals. Between them, these signals ensure that the timing system of a target converter can be reset, and that all digital sub-systems are properly locked to the reference master clock. Moreover, this synchronization can be extended to further ADCs throughout the system.

The benefits of this approach are that it guarantees synchronization across a large number of parallel channels over the lifetime of the system. Once a design has been finalized and is ready for production, a single training cycle is all that is required to establish correct system synchronization. Training establishes characteristic system timing parameters that can be flashed into local memory. If part to part variation and environmental conditions change such as temperature or voltage, the timing parameters remain fixed. The SYNC chain provides a rock solid, guaranteed for life, synchronization source - a major benefit when moving into mass production.

Initially, the need for synchronization as a counter to metastability is discussed, before moving on to the implementation of the SYNC chain which requires some understanding of the ADC's clock management unit. Advice is provided on how to train the system to account for variable signal latencies both between devices on a common board or those incurred passing across a backplane. Phase adjustments will be detailed in terms of coarse and fine control incurred when using interleaved converters typified by the EV12AQ600. The document concludes with some frequently asked questions (FAQs) summarizing the key themes covered.

THE CHALLENGE OF SYNCHRONIZING GIGAHERTZ SAMPLING SYSTEMS

The principle of interference as applied in digital beamforming to radio systems requires antenna arrays whose low-level signals are sampled simultaneously (or synchronously). This is necessary to preserve spatial (or signal phase) information as signals arrive at each antenna node. Though there's a penalty in terms of added complexity and power consumption with such an approach, several worthwhile benefits arise from an electrical and mechanical standpoint:

- For the Electrical part, the radio link efficiency and capacity can be improved thanks to higher Signal to Noise Ratio (SNR) due to multi-channel and reduced interferer level; higher directivity allowing frequency reuse; and the possibility to have multiple beams simultaneously.

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- On the mechanical side, this approach reduces the number of mechanical parts in scanning systems and reduce mechanical maintenance costs; it allows faster scanning response.

Today many applications already use beamforming, but as the demand for bandwidth rises inexorably, sampling precision goes up as do the pressures on system design and the reference sample clock.

At gigahertz frequencies, signal propagation times become important both at an integrated circuit (IC) and board level. Printed circuit board (PCB) traces act as transmission lines and it is critical that signal trace lengths are matched to retain phase information in multi-channel environment. Consider that a centimetre of trace adds between 60 to 75ps of travel time. Compare that to the clock period of 166ps for a 6 GHz sample clock. Board level effects will clearly influence design choices.

Moreover, complex ICs are now considerably faster, and it is not uncommon that usable bandwidths in the multi-gigahertz domain are used. Board and IC design demands place an emphasis on managing the analog side of design. But another issue falls within the digital domain at such high frequencies, namely metastability.

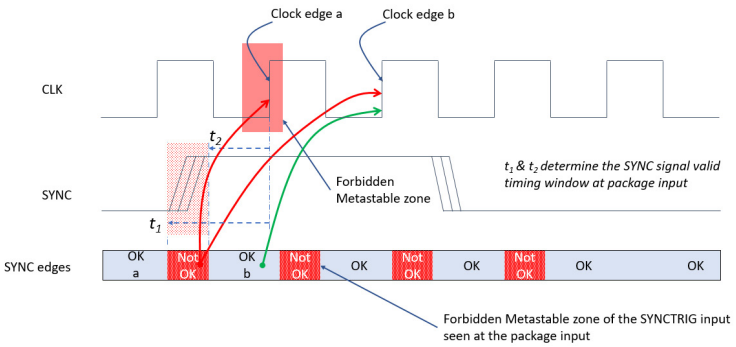
METASTABILITY DRIVES THE NEED FOR SYNCHRONIZATION.

Metastability is not a frequency related effect. However, as clock periods shrink with increasing frequency, avoiding metastability becomes increasingly difficult.

Metastability describes behaviour of a digital system that, for a short time period, sits in an unstable equilibrium. This is undesirable and synchronous logic design specifically aims to avoid metastable zones. It arises primarily as complex digital systems feature many processing blocks with more than one independent clock domain. Metastability is mitigated by ensuring the input set-up and hold times for internal flip-flops are satisfied across the system.

Pictorially this is described in the following diagram.

Figure 1 - Forbidden metastable zone



The master clock is identified as CLK and t1 and t2 are the set-up and hold times respectively for a given digital block. The lower trace shows the forbidden metastable zone (between t1 -t2) for each rising clock edge. t1 & t2 determine the SYNC signal valid timign window at package input. Note that the lower trace (SYNC edges) shows the forbidden zone as seen at the SYNCTRIG input pins of the ADC. This added delay compensates for clock and input signal routing within the IC. Synchronous design ensures the forbidden zone is avoided when asserting the SYNC signal. Two possible SYNC transitions are shown on the clock signal. The one to avoid (labelled a) in figure 1) is that where the rising edge occurs within the forbidden zone.

THE CMU GENERATES A SYNC PULSE FOR DETERMINISTIC OPERATION

Inspecting the on-chip clock management unit (CMU) shows the origin of the SYNCTRIG and SYNCO signals together with the various control signals associated with the SPI interface. The behaviour of this block is tightly coupled to the digital control system accessed via the SPI interface.

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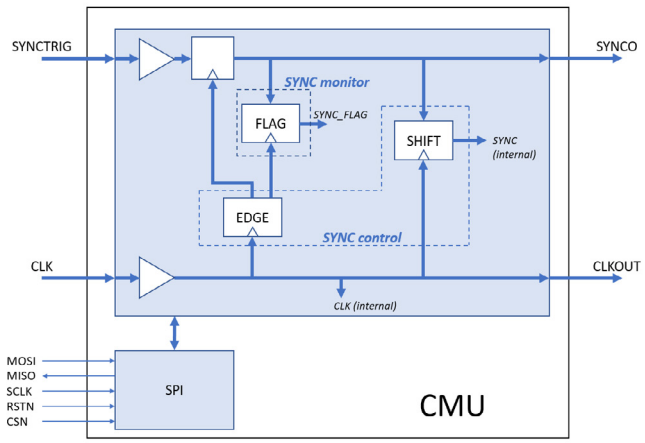
Figure 2 - Clock Management Unit (CMU)



The generation of the first SYNCTRIG output (SYNCO) ensures the following timing conditions are met:

- Edges of the SYNCTRIG pulse are kept outside the forbidden area highlighted in figure 1 previously. Pay careful attention to the device specified set-up and hold timing
- SYNCTRIG pulse rise and fall time falls within the specified slew rate specification

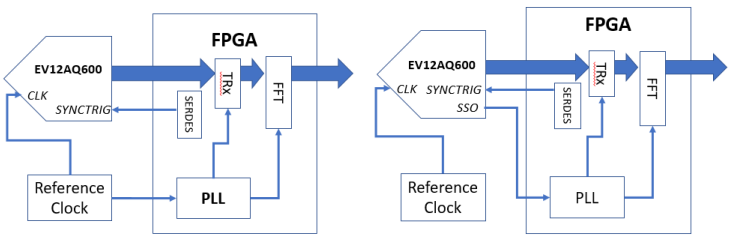
The CMU monitors the position of the SYNCTRIG pulse edge. As part of edge monitoring, several controls are available through the SPI interface that help gain deterministic control over either individual converters or even multiple parts. The control features specific to synchronization include the following three SYNC registers:

- SYNC_FLAG (address = 0x000D) – is a detection flag indicating a timing violation. The flag is asserted if the rising edge of SYNC falls within the forbidden zone.
- SYNC_FLAG_RST (address = 0x000E) – on detecting an active SYNC_FLAG as above this register should be read to reset it prior to re-sending a new SYNC pulse.
- SYNC_CTRL (address = 0x000C) – this 3-bit register provides two control options as follows:
  - Bit[0] or sync_edge indicates on which edge of the system master clock the SYNCTRIG is sampled
    - > Bit[0] = 0 then the positive edge is selected
    - > Bit[0] = 1 then the negative edge is selected
  - Bits [2:1] or sync_shift delays by one or more system clock periods the internal reset process for a given ADC. This is tied to the 6.4GHz master reference clock and the quad core architecture.
    - > Bits [2:1] = 00 - No additional clock period added
    - > Bits [2:1] = 01 – One extra clock period added
    - > Bits [2:1] = 10 – Two extra clock periods added
    - > Bits [2:1] = 11 – Three extra clock periods added

SYNCTRIG SIGNAL SOURCE

The synchronization signal supplied to and from an individual analog to digital convertor is an LVDS serial differential signal which is easily generated from within a digital signal processing block such as an FPGA. Two obvious signal generation approaches are shown in figure 3. The first (on the left) uses a precision master clock to drive both the FPGA and the ADC block. On the right-hand side, the FPGA is shown clocked by the slow synchro output (SSO) – which is a data serialization clock provided by the ADC which is dependent on the reference clock but runs 32x slower.

Figure 3 - Two approaches to generating SYNCTRIG



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ALIGNING SYNCTRIG AND SYNCO

Once deterministic operation has been established within an individual converter, you can be sure that SYNCO is aligned to the master clock, whereas the SYNCTRIG signal can arrive at the first ADC asynchronously to the master clock. This is the real benefit of the SYNC chain approach since SYNCO is re-sampled by the system master reference clock and becomes a perfect SYNCTRIG source for the next ADC in the chain.

CALCULATING SYNC CHAIN DELAY

The mathematics for calculating the SYNC chain delay is fixed by the master clock phase delay as it travels between individual ADCs (in multiples of sample clock, T_{CLK}). To fully account for the clock's propagation delay, the total number of T_{CLK} periods N needs to be measured. However, with interleaved operation of the EV12AQ600, the sample clock is divided by factors 1, 2 or 4 depending on the specific clock mode selected (see details on interleaving in the EV12AQ600 data sheet). Therefore, the best expression for SYNC chain delay is given as:

$$SYNC\ chain\ delay = n.T_s + SYNC\_shift$$

$$T_S = 4\,.T_{CLK} \qquad SYNC\_shift = k\,.T_{CLK}$$

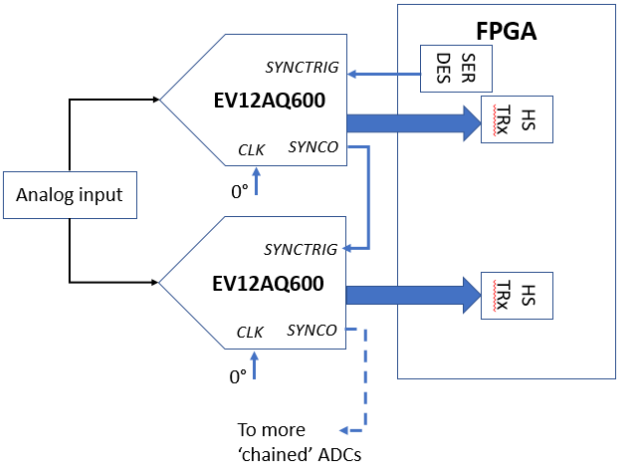
$$SYNC\ chain\ delay = (4.n. + k).T_{CLK} \qquad where\ k\ \in (0, 1, 2, 3)$$

SYNC chain delay is seen here as comprising an integer multiple of the master clock periods plus up to three SYNC shifts, controlled by the SYNC_CTRL (address = 0x000C) register previously described.

PRACTICAL IMPLEMENTATION FOR SYNCHRONOUS OPERATION

To achieve synchronization in large multi-ADC systems the SYNC chain takes the SYNC output (SYNCO) signal and daisy chains it on to further ADCs in the system as shown in figure 4.

Figure 4 - SYNC chaining implementation



Two steps must be taken to guarantee synchronous operation using the SYNC features of the ADC.

- Configuring the chained ADC to avoid SYNC assertion during metastability on its SYNCTRIG input
- Configuring the ADC so that all internal clocks are time aligned and therefore synchronous

This is achieved using a simple training sequence which is detailed here. Two situations can arise on SYNCTRIG assertion:

- The first SYNCTRIG pulse arrives asynchronously (user defined) to the sample clock which is a relatively low probability event.
- The first SYNCTRIG pulse arrives synchronously to the sample clock

In the asynchronous case, SYNCTRIG will need to be resent until it is correctly received by the first converter. Correct reception is identified by monitoring the SYNC_FLAG and its reset signal (SYNC_FLAG_RST). The probability of hitting a metastable state is low. Consider that on the current process technology, set-up and hold times of a few pico-seconds are usual. With a 6.4GHz reference clock that's a 156ps period so the probability of metastability is in the order of a couple of percent. This means it is only necessary to send SYNCTRIG a couple of times before synchronous operation is guaranteed.

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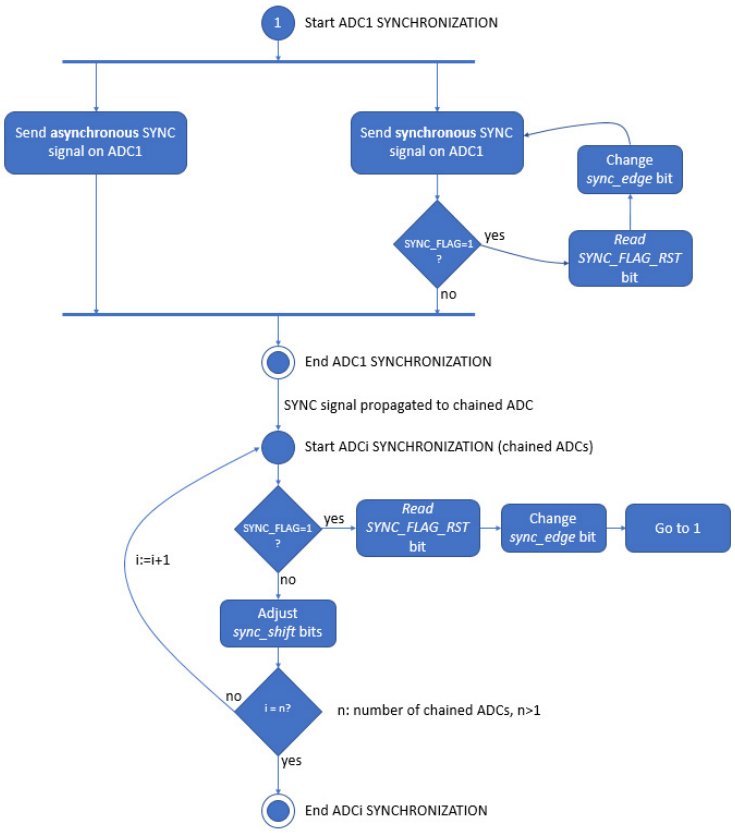
SYNC TRAINING ALGORITHMS

The SYNC training algorithm for multiple ADCs is provided in figure 5.

Figure 5 - SYNC training algorithm (1 device)



Training a complete system is a little more involved than discussed so far, primarily as its likely there are variable latencies between individual ADC channels. Highly parallel systems need to transmit synchronization across a backplane as well as between devices on individual boards. So, in this case, it becomes imperative that the individual delays throughout the system are mapped. Assuming system synchronization then time alignment of samples is performed in the digital domain by the digital signal processing system. In common with most serial data systems, a flexible elastic data buffer is used for this purpose.

System training demands that latencies between channels be measured. Teledyne-e2v sees three techniques by which this can be achieved, each with their independent pros and cons as summarized below.

Methods	Requires	Pros	Cons
Manual	An input signal with sharp edges (e.g. square-wave or ramp)	- Proven - Allows trimming of other parameters at the same time	- Need access to a specific hf waveform - Need visual data interface
Auto & cross correlation	A FS analog input signal	- Can be automated - No FFT computation needed	- Need to interleave data
FFT approach	Performing an FFT	- Can be automated - Only one core of each ADC need be available for testing	- Needs an FFT computation (all be it a single point)

Of the three approaches outlined, only two suit automation and thus use within a modern production environment. It is worth considering these in a little more detail.

THE CORRELATION METHOD

Establish system operation to have the ADCs in full interleaved mode and apply a full-scale input sinewave to each ADC core. Interleave resulting data at the maximum sample rate (6.4 Gsps or lower depending on user need). This ensures measurement data will have granularity down to the master clock (TCLK) rate. Auto and cross-correlate the sampled data from adjacent ADCs (ADC1 & ADC2). Compare the resultant maximum outputs for both the auto and cross-correlated results. The difference in maxima is the phase shift required to correct the SYNC chain delay.

THE FFT METHOD

Apply a sinewave test signal to the system and acquire data from a single core in each ADC. Compute the FFT phase term for the fundamental frequency. Compare the phase terms for each ADC. The phase information can be directly related

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to the necessary SYNC shift value for each. The number of TCLK shifts can be computed from the following equation.

$$n = \frac{\left[FFT_{\varphi ADC1} - FFT_{\varphi ADC2}\right] \cdot \frac{1}{F_{in}}}{360.T_{CLK}}$$

SYNC CHAINING IN ACTION ACROSS A MULTI-ADC SYSTEM

Figure 6a - SYNChronization (pre-training)

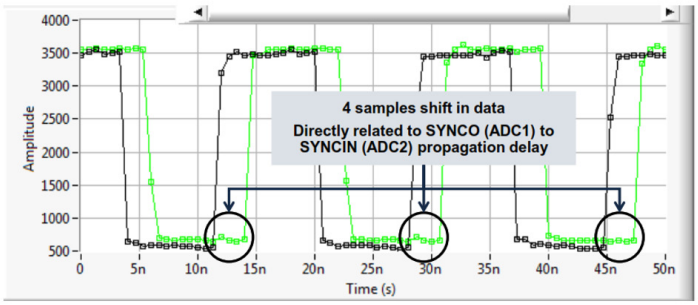


Figure 6b - SYNC training (coarse adjust) at reference clock rate, T_{CLK}

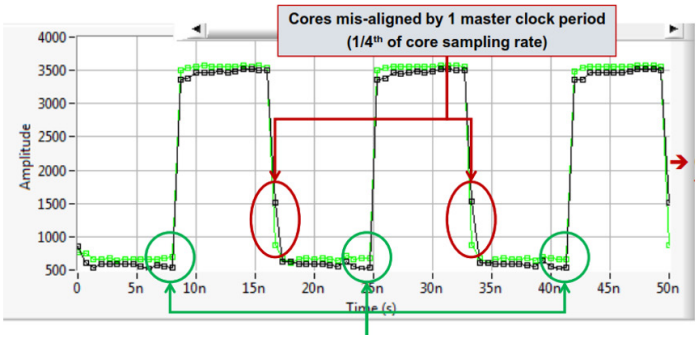
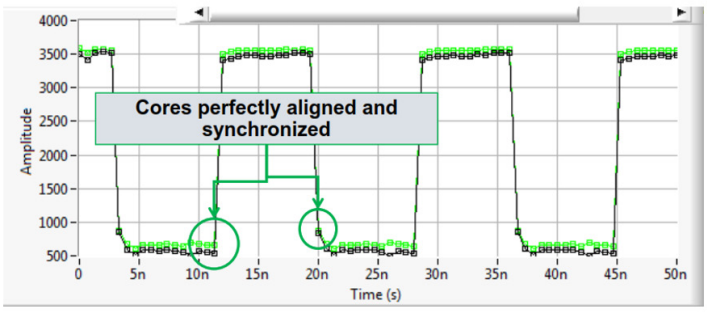


Figure 6c - SYNC training (fine adjust) with *sync_shift* at sub-reference clock rate, $T_{CLK}/4$



BENEFITS OF SYNC CHAINING

The SYNC chain function has no direct impact on the master system clock, adding no extra jitter and ensuring optimal dynamic range. Moreover, Teledyne-e2v has shown that the SYNC chain is a robust approach to synchronize multi-channel systems. Once system time delays are determined in the training process, they can be flashed to memory and will remain constant over the lifetime of a system. Deterministic latency remains robust even in the face of changing environmental conditions such as process changes, voltage and temperature. This is an important step to simplifying manufacturing of complex multi-channel systems and reducing set-up costs.

CONCLUSION

The SYNC chaining feature described here as part of Teledyne-e2v's EV12AQ600 helps to reduce complexity in challenging, high performance multi-channel sampling systems in phased array systems employing digital beam-forming techniques and MIMO equipment.

Individual ADCs include dedicated circuitry to detect and mitigate metastability and supply a re-sampled SYNC signal in support of the SYNC chain. This event driven process can be remotely controlled via the devices' own SPI interface which further helps ease system set-up. A simple, one-time training sequence carried out during pre-production qualification is all that is needed to establish the system timing delay characteristics and thus establish synchronization throughout. Overall, SYNC chaining brings multiple advantages, of which rock-solid system synchronization at power-up is the most helpful customer benefit. The SYNC chaining approach preserves clock dynamic performance, so no additional jitter or phase noise is added as a result.

Finally, SYNC chaining has been proven to be highly robust in the face of changing operating

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environments meaning it is an excellent choice in high reliability applications. This technique will feature in the EV12AQ605 and other future Teledyne-e2v devices.

FREQUENTLY ASKED QUESTIONS

How does SYNC chaining compare to other synchronization methods?

Converters designed with JEDEC serial link technology were first able to guarantee deterministic latency when JESD204B sub-class 1 was published. This uses what may seem, at first glance, to be a similar approach to that offered by Teledyne-e2v's open source ESIstream system combined with the SYNC chain. For JESD204B sub-class 1, synchronization is facilitated using the SYSREF clock. What this approach lacks in comparison to the SYNC chain is the provision of the re-sampled SYNC output (SYNCO). This critical difference is the secret to the SYNC chain's simplicity. As SYNCO is re-sampled by the reference sample clock, then it can be relied upon to form the SYNCTRIG input signal for the next ADC along the chain. SYSREF adopts a timing tree distribution approach and requires careful board layout and additional components to handle the output fanout demands. Moreover, it must be treated similarly to the input signal and reference clock in respect to PCB routing.

ESIstream with SYNC or JESD204B with SYSREF?

Both systems have specific benefits depending on application needs. That said, JESD204B carries some significant extra technology overheads that add to its complexity, power demands and potentially sways the economic argument towards the open source ESIstream approach. Incidentally, a few sources including suppliers of JESD204B products acknowledge that:

'JESD204B can be a complicated interface standard, with many operational subtleties. Finding out why it is not working requires a good understanding of likely scenarios....'

SYNC training versus calibration used with other synchronization techniques?

The training sequence is a one-time event performed when a system design using the SYNC chain feature of the EV12AQ600 is complete. Once timing characteristics are derived from the training sequence, they remain constant over the lifetime of the system assuming no physical changes are made – such as cable lengths. This remains fixed even with part to part variations and voltage and temperature changes. Calibration is required by JESD204B sub-class 1 as well as other methods to ensure synchronization. In this case, a start-up sequence must be initiated each time the system is power cycled. This can impact system availability.

Does SYNC chaining ever require re-calibration?

No, given a fixed design. Once a system has been finalized and is production ready, a single training sequence is all that is required to establish correct sample synchronization. The training phase establishes characteristic system timing variables that can be flashed into local memory and loaded at system power-up. Even if part to part variation and environmental conditions change such as temperature or voltage, the timing parameters remain constant as they are characteristic of the physical design. The SYNC training step is a once in a lifetime step. This makes the SYNC chain a huge benefit moving into mass production.

What do I watch out for when using the SYNC chain?

SYNC chaining is an economic method to establish synchronous sample operation across massively parallel systems. However, considerable care is still required in routing RF, microwave or millimeter-wave input signals and the reference sample clock to ensure matched trace lengths. In comparison,

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routing the SYNC signal is straightforward as it's a relatively slow, single-shot signal.

Can I automate SYNC chain training?

Yes you can, and two techniques have been briefly described in this document. The simplest is the auto/cross-correlation method which requires that all devices be operated in 4-channel interleaved mode. Alternatively, a more complex approach derives phase information from Fast Fourier transforms (FFTs) performed on output frequency data between a single channel on each discrete converter core.

Is there a limit to the number of chained ADCs?

There is no practical limit since the SYNC signal is re-sampled within each device effectively eliminating the latency of the SYNC signal's propagation through a single device and even across the whole system. Obviously, the more converters connected in a chain will slow the training sequence though. Note that the ADCs can be configured in either a daisy chained, point to point approach or as a tree architecture to optimize initialization time.

Can I ignore input signal trace length matching given the benefit of SYNC chaining?

No. Trace lengths slow signals' propagation across printed circuit boards and since beamforming relies on the critical timing differences between those signals (phase information) the same care in board layout needs to be concentrated on relative timing between analog sampled signals and their sample clock. To system integrators, the benefit of the SYNC chain is that it is a relatively slow signal that does not bump up against the challenge of transmission line signal routing and is thus easily transmitted over boards and backplanes.

What timing constraints impact the setting of the SYNC pulse?

SYNC_FLAG and sync_edge controls ensure that metastable zones can be avoided in any design. To achieve this, each Teledyne-e2v converter deploys specific clock circuitry to monitor and determine when the SYNC signal coincides with a metastable zone. On identifying this, the SYNC signal can be advanced by one clock edge to move it out of the metastable forbidden zone by accessing the SYNC_CTRL register.