TS83102G0BMGS
10-bit 2 Gsps ADC MIL

Datasheet

Features

- **Up to 2 Gsps Sampling Rate**
- **Power Consumption: 4.6W**
- **500 mVpp Differential 100Ω or Single-ended 50Ω (±2%) Analog Inputs**
- **Differential 100Ω or Single-ended 50Ω Clock Inputs**
- **ECL or LVDS Output Compatibility**
- **50 Ω Differential Outputs with Common Mode not Dependent on Temperature**
- **ADC Gain Adjust**
- **Sampling Delay Adjust**
- **Offset Control Capability**
- **Data Ready Output with Asynchronous Reset**
- **Out-of-range Output Bit**
- **Selectable Decimation-by-32 function**
- **Gray or Binary Selectable Output Data; NRZ Output Mode**
- **Pattern Generator Output (for Acquisition System Monitoring)**
- **Radiation Tolerance Oriented Design (More Than 100 Krad (Si) Expected)**
- **CI-CGA152 Cavity Down Hermetic Package**
- **Evaluation Board TSEV83102G0BGL**
- **Companion Device: DMUX 8-/10-bit 1:2/4 2.2 Gsps AT84CS001TP**

Performance

- **3.3 GHz Full Power Input Bandwidth (–3 dB)**
- **Gain Flatness: ± 0.2 dB (from DC up to 1.5 GHz)**
- **Low Input VSWR: 1.2 Max from DC to 2.5 GHz**
- **SFDR = –59 dBc; 7.6 Effective Bits at F_S = 1.4 Gsps, F_{IN} = 700 MHz [–1 dBFS]**
- **SFDR = –53 dBc; 7.1 Effective Bits at Fs = 1.4 Gsps, F_{IN} = 1950 MHz [–1 dBFS]**
- **SFDR = –54 dBc; 6.5 Effective Bits at F_S = 2 Gsps, F_{IN} = 2 GHz [–1 dBFS]**
- **Low Bit Error Rate (10^{-12}) at 2 Gsps**

Application

- **Direct RF Down Conversion**
- **Wide Band Satellite Receiver**
- **Radar**

Screening

- **Temperature Range for Packaged Device:**
  - *M* Grade: –40°C<T_C; T_J<125°C
- **Standard Die Flow (upon Request)**

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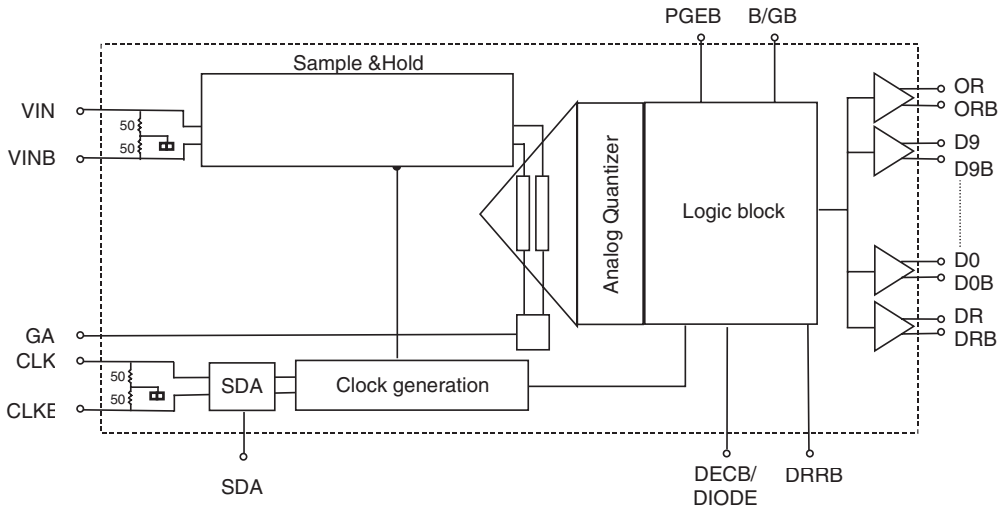
1. Description

The TS83102G0BMGS is a monolithic 10-bit analog-to-digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 2 Gsps. It uses an innovative architecture, including an on-chip Sample and Hold (S/H). The 3.3 GHz full power input bandwidth and band flatness performances enable the digitizing of high IF and large bandwidth signals.

Figure 1-1. Simplified Block Diagram



2. Functional Description

The TS83102G0BMGS is a 10-bit 2 Gsps ADC. The device includes a front-end master/slave Track and Hold stage (Sample and Hold), followed by an analog encoding stage (Analog Quantizer), which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuit and resynchronization stage, followed by 50Ω differential output buffers.

The TS83102G0BMGS works in a fully differential mode from analog inputs to digital outputs. A differential Data Ready output (DR/DRB) is available to indicate when the outputs are valid and an Asynchronous Data Ready Reset ensures that the first digitized data corresponds to the first acquisition.

The control pin B/GB (A11 of the CI-CGA package) is provided to select either a binary or gray data output format. The gain control pin GA (R9 of the CI-CGA package) is provided to adjust the ADC gain transfer function.

A Sampling Delay Adjust function (SDA) may be used to ease the interleaving of ADCs. A pattern generator is integrated on the chip for debug or acquisition setup. This function is activated through the PGEB pin (A9 of the CI-CGA package).
An out-of-range bit (OR/ORB) indicates when the input overrides 0.5 Vpp.
A selectable decimation by 32 functions is also available for enhanced testability coverage (A10 of the CI-CGA package), along with the die junction temperature monitoring function.
The TS83102G0BMGS uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allows enhanced radiation tolerance (over 100 kRad (Si) total dose expected tolerance).

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3. Specification

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6.0	V
Digital negative supply voltage	D_{VEE}		GND to –5.7	V
Digital positive supply voltage	V_{PLUSD}		GND – 1.1 to 2.5	V
Negative supply voltage	V_{EE}		GND to –5.5	V
Maximum difference between negative supply voltages	D_{VEE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		–1.5 to 1.5	V
Maximum difference between VIN and VINB	V_{IN} - V_{INB}		–1.5 to 1.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		–1 to 1	V
Maximum difference between VCLK and VCLKB	V_{CLK} - V_{CLKB}		–1 to 1	Vpp
Static input voltage	V_D	GA, SDA	–5 to 0.8	V
Digital input voltage	V_D	SDAEN, DRRB, B/GB, PGEB, DECB	–5 to 0.8	V
Digital output voltage	V_O		V_{PLUSD} min. operating –2.2 to V_{PLUSD} max. operating + 0.8	V
Junction temperature	T_J		130	°C

Note: Absolute maximum ratings are short term limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability. All integrated circuits have to be handled with appropriate care to avoid damage due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Table 3-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Positive supply voltage	V_{CC}		4.75	5	5.25	V
Positive digital supply voltage	V_{PLUSD}	Differential ECL output compatibility	–0.9	–0.8	–0.7	V
		LVDS output compatibility	1.375	1.45	1.525	V
		Grounded[1]				
		Maximum operating VPLUSD			1.7	V
Negative supply voltages	V_{EE}, D_{VEE}		–5.25	–5.0	–4.75	V
Differential analog input voltage (full-scale)	V_{IN}, V_{INB} V_{IN} - V_{INB}	50Ω differential or single-ended	±113 450	±125 500	±137 550	mV mVpp
Clock input power level (ground common mode)	P_{CLK}, P_{CLKB}	50Ω single-ended clock input or 100Ω differential clock (recommended)	–4	0	4	dBm

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Table 3-2. Recommended Conditions of Use (Continued)

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Operating Temperature Range		Military *M* grade		$-40°C < T_C; T_J < 125°C$		°C
Storage Temperature	Tstg			–65 to 150		°C
Lead Temperature	Tlead			300		°C

Note: 1. ADC performances are independent of V_{PLUSD} common mode voltage and performances are guaranteed in the limits of the specified V_{PLUSD} range (from –0.9V to 1.7V)

Table 3-3. Electrical Operating Characteristics

V_{CC} = 5V ; V_{PLUSD} = 0V (unless otherwise specified). ADC performances are independent of V_{PLUSD} common mode voltage and performances are guaranteed within the limits of the specified V_{PLUSD} range (from –0.9V to 1.7V);
V_{EE} = D_{VEE} = –5V; V_{IN} - V_{INB} = 500 mVpp (full-scale single-ended or differential input);
clock inputs differential driven; analog-input single-ended driven.

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Resolution				10		Bits
Power Requirements						
Positive supply voltage - analog - digital (ECL) - digital (LVDS)	 1 1 4	 V_{CC} V_{PLUSD} V_{PLUSD}	 4.75	 5 –0.8 1.45	 5.25	 V V V
Positive supply current - analog - digital	 1 1	 I_{VCC} I_{VPLUSD}		 138 154	 205 200	 mA mA
Negative supply voltage - analog - digital	 1 1	 V_{EE} D_{VEE}	 –5.25 –5.25	 –5 –5	 –4.75 –4.75	 V V
Negative supply current - analog - digital	 1 1	 V_{EE} I_{DVEE}		 615 160	 750 200	 mA mA
Power dissipation - ECL - LVDS	 1 4	 P_D		 4.6 5.0	 5.2 5.7	 W W
Analog Inputs						
Full-scale input voltage range (differential mode) (0V common mode voltage)	4 4	$V_{IN,}$ V_{INB}	–125 –125		125 125	mV mV
Full-scale input voltage range (single-ended input option) (0V common mode voltage)	4 4	$V_{IN,}$ V_{INB}	–250	0	250	mV mV
Analog input power level (50Ω single-ended)	4	P_{IN}		–2		dBm
Analog input capacitance (die)	4	C_{IN}		0.3		pF
Input leakage current	4	I_{IN}		10		µA

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Table 3-3. Electrical Operating Characteristics (Continued)

V_{CC} = 5V ; V_{PLUSD} = 0V (unless otherwise specified). ADC performances are independent of V_{PLUSD} common mode voltage and performances are guaranteed within the limits of the specified V_{PLUSD} range (from –0.9V to 1.7V);
V_{EE} = D_{VEE} = –5V; V_{IN} - V_{INB} = 500 mVpp (full-scale single-ended or differential input);
clock inputs differential driven; analog-input single-ended driven. (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Input resistance - single-ended - differential	 4 4	 R_{IN} R_{IN}	 49 98	 50 100	 51 102	 Ω Ω
Clock Inputs						
Logic common mode compatibility for clock inputs	Differential ECL to LVDS					
Clock inputs common voltage range (V_{CLK} or V_{CLKB}) (DC coupled clock input) AC coupled for LVDS compatibility (common mode 1.2V)	4	V_{CM}	–1.2	0	0.3	V
Clock input power level (low-phase noise sinewave input) 50Ω single-ended or 100Ω differential	4	P_{CLK}	–4	0	4	dBm
Clock input swing (single ended; with CLKB = 50Ω to GND)	4	V_{CLK}	±200	±320	±500	mV
Clock input swing (differential voltage) - on each clock input	4	V_{CLK} V_{CLKB}	±141	±226	±354	mV
Clock input capacitance (die)	4	C_{CLK}		0.3		pF
Clock input resistance - single-ended - differential ended	 	 R_{CLK} R_{CLK}	 45 90	 50 100	 55 110	 Ω Ω
Digital Inputs (SDAEN, PGEB, DECB/Diode, B/GB, DRRB)	4	V_{IL} V_{IH}	–5 –2		–3 0	V V
Digital Inputs (DRRB only)						
Logic compatibility			Negative ECL			
- logic low - logic high	4	V_{IL} V_{IH}	–1.810 –1.165		–1.625 –0.880	V V
Digital Outputs (1)						
Logic compatibility (depending on V_{PLUSD} value)	Differential ECL (V_{PLUSD} = –0.8 V typical)					
Output levels 50Ω transmission lines, 10Ω (2 x 50Ω) differentially terminated - logic low - logic high - swing (each single-ended output) - common mode	 1 1 1 4	 V_{OL} V_{OH} V_{OH} - V_{OL}	 –0.98 200 –0.95	 –1.17 –0.94 230 –1.05	 –1.10 300 –1.15	 V V mV V

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Table 3-3. Electrical Operating Characteristics (Continued)

V_{CC} = 5V ; V_{PLUSD} = 0V (unless otherwise specified). ADC performances are independent of V_{PLUSD} common mode voltage and performances are guaranteed within the limits of the specified V_{PLUSD} range (from –0.9V to 1.7V); V_{EE} = D_{VEE} = –5V; V_{IN} - V_{INB} = 500 mVpp (full-scale single-ended or differential input); clock inputs differential driven; analog-input single-ended driven. (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Logic compatibility (depending on V_{PLUSD} value)	LVDS (V_{PLUSD} = 1.4 V typical)					
Output levels 50Ω transmission lines, 100Ω (2 x 50Ω) differentially terminated						
- logic low	4	V_{OL}	825	1090		mV
- logic high	4	V_{OH}		1310	1575	mV
- swing (each single-ended output)	4	V_{OH} - V_{OL}	200	230	300	mV
- common mode max. V_{PLUSD} = 1.525V	4				1275	mV
typ. V_{PLUSD} = 1.45V	4		1190	1200		mV
min. V_{PLUSD} = 1.375V	4		1125		1210	mV
DC Accuracy						
DNLrms [2]	4	DNLrms	0.50	0.53	0.55	LSB
Differential nonlinearity [3]	1	DNL+		1.5	2	LSB
Integral nonlinearity [3]	1	INL-	–4.0	–2.4		LSB
Integral nonlinearity [3]	1	INL+		2.4	4.0	LSB
Gain central value [4]	1		0.89	0.94	1.1	
Gain error drift	4			23	35	ppm/°C
Input offset voltage	1		–10		10	mV

Note:
1. Differential output buffers impedance = 100Ω differential (50Ω single-ended). See.Figure 9-7 on page 41
2. Histogram testing at Fs = 1 Gsps, Fin = 100 MHz, DNLrms is a component of quantization noise.
3. Histogram testing at Fs = 50 Msps, Fin = 25 MHz.
4. This range of gain can be set to *1* by using the gain adjust function.

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Table 3-4. AC Electrical Characteristics at Ambient and Hot Temperatures (T_J Max)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Analog Inputs						
Full power input bandwidth (1)	4	FPBW		3.3		GHz
Small signal input bandwidth (10% full-scale) (1)	4	SSBW		3.5		GHz
Gain flatness (2)	4	BF		± 0.2	± 0.3	dB
Input voltage standing wave ratio (3)	4	VSWR		1.1:1	1.2:1	
AC Performance: Nominal Condition at Ambient and Hot Temperatures T_J Max –1 dBFS single-ended input mode (unless otherwise specified); 50% clock duty cycle; 0 dBm differential clock (CLK, CLKB); binary output data format						
Signal-to-noise and distortion ratio						
Fs = 1 Gsps Fin = 100 MHz	4		47	50		
Fs = 1.4 Gsps Fin = 700 MHz	1	SINAD	44	48		dB
Fs = 1.4 Gsps Fin = 1950 MHz	4		43	45		
Fs = 2 Gsps Fin = 2 GHz	4		38	41		
Effective number of bits						
Fs = 1 Gsps Fin = 100 MHz	4		7.5	8.0		
Fs = 1.4 Gsps Fin = 700 MHz	1	ENOB	7.0	7.6		Bit
Fs = 1.4 Gsps Fin = 1950 MHz	4		6.8	7.1		
Fs = 2 Gsps Fin = 2 GHz	4		6.1	6.5		
Signal to noise ratio						
Fs = 1 Gsps Fin = 100 MHz	4		48	50		
Fs = 1.4 Gsps Fin = 700 MHz	1	SNR	45	48		dB
Fs = 1.4 Gsps Fin = 1950 MHz	4		44	45		
Fs = 2 Gsps Fin = 2 GHz	4		39	41		
Total harmonic distortion						
Fs = 1 Gsps Fin = 100 MHz	4		48	54		
Fs = 1.4 Gsps Fin = 700 MHz	1	ITHDI	48	53		dB
Fs = 1.4 Gsps Fin = 1950 MHz	4		44	50		
Fs = 2 Gsps Fin = 2 GHz	4		44	49		
Spurious-free dynamic range						
Fs = 1 Gsps Fin = 100 MHz	4		50	59		
Fs = 1.4 Gsps Fin = 700 MHz	1	ISFDRI	50	59		dBC
Fs = 1.4 Gsps Fin = 1950 MHz	4		45	53		
Fs = 2 Gsps Fin = 2 GHz	4		45	54		

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Table 3-4. AC Electrical Characteristics at Ambient and Hot Temperatures (T_J Max) (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Two-tone third-order intermodulation distortion Fs = 1.2 Gsps Fin1 = 995 MHz Fin2 = 1005 MHz [–7dBFS]	4	IMD3		65		dBFS
Fs = 1.4 Gsps Fin1 = 745 MHz Fin2 = 755 MHz [–7dBFS]	4			65		
Fs = 1.4 Gsps Fin1 = 995 MHz Fin2 = 1005 MHz [–7dBFS]	4			65		
Fs = 1.4 Gsps Fin1 = 1244 MHz Fin2 = 1255 MHz [–7dBFS]	4			65		

Note: 1. See “Definition of Terms” on page 33

2. From DC to 1.5 GHz

3. Specified from DC up to 2.5 GHz input signal. Input VSWR is measured on a soldered device. It assumes an external 50Ω ±2Ω controlled impedance line, and a 50Ω driving source impedance (S_{11} < – 30 dB)

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Table 3-5. AC Performance at Cold Temperature (T_C Min)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
AC Performance Condition –1 dBFS single-ended input mode; 50% clock duty cycle; 0 dBm differential clock (CLK, CLKB); binary output data format						
Signal-to-noise and distortion ratio						
Fs = 1 Gsps Fin = 100 MHz			38	40		
Fs = 1.4 Gsps Fin = 700 MHz	4	SINAD	37	38		dB
Fs = 1.4 Gsps Fin = 1950 MHz			37	38		
Fs = 2 Gsps Fin = 2 GHz			36	38		
Effective number of bits						
Fs = 1 Gsps Fin = 100 MHz			6.0	6.3		
Fs = 1.4 Gsps Fin = 700 MHz	4	ENOB	5.8	6.1		Bit
Fs = 1.4 Gsps Fin = 1950 MHz			5.8	6.1		
Fs = 2 Gsps Fin = 2 GHz			5.7	6.0		
Signal to noise ratio						
Fs = 1 Gsps Fin = 100 MHz			46	47		
Fs = 1.4 Gsps Fin = 700 MHz	4	SNR	45	47		dB
Fs = 1.4 Gsps Fin = 1950 MHz			45	46		
Fs = 2 Gsps Fin = 2 GHz			43	44		
Total harmonic distortion						
Fs = 1 Gsps Fin = 100 MHz			38	40		
Fs = 1.4 Gsps Fin = 700 MHz	4	ITHDI	37	39		dB
Fs = 1.4 Gsps Fin = 1950 MHz			37	39		
Fs = 2 Gsps Fin = 2 GHz			37	39		
Spurious free dynamic range						
Fs = 1 Gsps Fin = 100 MHz			39	42		
Fs = 1.4 Gsps Fin = 700 MHz	4	ISFDRI	38	40		dBC
Fs = 1.4 Gsps Fin = 1950 MHz			37	40		
Fs = 2 Gsps Fin = 2 GHz			37	40		

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Table 3-6. Transient and Switching Performances

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Transient Performance						
Bit error rate (1)	4	BER		10^{-12}		Error/ sample
ADC setting time (V_{IN} - V_{INB} = 400 mVpp)	4	TS		1		ns
Overvoltage recovery time	4	ORT			500	ps
ADC step response rise/fall time (10% to 90%)				80	100	ps
Overshoot				4		%
Ringback				2		%
Switching Performance and Characteristics						
Maximum clock frequency (2)		F_SMax	2		2.2	Gsps
Minimum clock frequency (2)	4	F_SMin		150	200	Msps
Minimum clock pulse width (high)	4	TC1	0.2	0.25	2.5	ns
Minimum clock pulse width (low)	4	TC2	0.2	0.25	2.5	ns
Aperture delay (2)	4	TA		160		ps
Aperture uncertainty (2)	4	Jitter		150	200	fs rms
Output rise/fall time for DATA (20% to 80%) (3)	4	TR/TF		150	200	ps
Output rise/fall time for DATA READY (20% to 80%) (3)	4	TR/TF		150	200	ps
Data output delay (4)	4	TOD		360		ps
Data ready output delay (4)	4	TDR		410		ps
	4	ITOD minus TDRI	0	50	100	ps
Output data to data ready propagation delay (5)	4	TD1	250	300	350	ps
Data ready to output data propagation delay (5)	4	TD2	150	200	250	ps
Output data pipeline delay	4	TPD		4.0		Clock cycles
Data ready reset delay	4	TRDR	1000			ps

Note:
1. Output error amplitude < ±6 LSB, Fs = 2 Gsps, T_J = 110°C
2. See “Definition of Terms” on page 33.
3. 50Ω // C_{LOAD} = 2 pF termination (for each single-ended output). Termination load parasitic capacitance derating value: 50 ps/pF (ECL). See “Timing Information” on page 35.
4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only. See “Propagation Time Considerations” on page 35.
5. Values for TD1 and TD2 are given for a 2 Gsps external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: TD1 = T/2 + (ITOD - TDRI) and TD2 = T/2 + (ITOD - TDRI), where T = clock period. This places the rising edge (True/False) of the differential data ready signal in the middle of the output data valid window. This gives maximum setup and hold times for external data acquisition.

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Table 3-7. Explanation of Test Levels

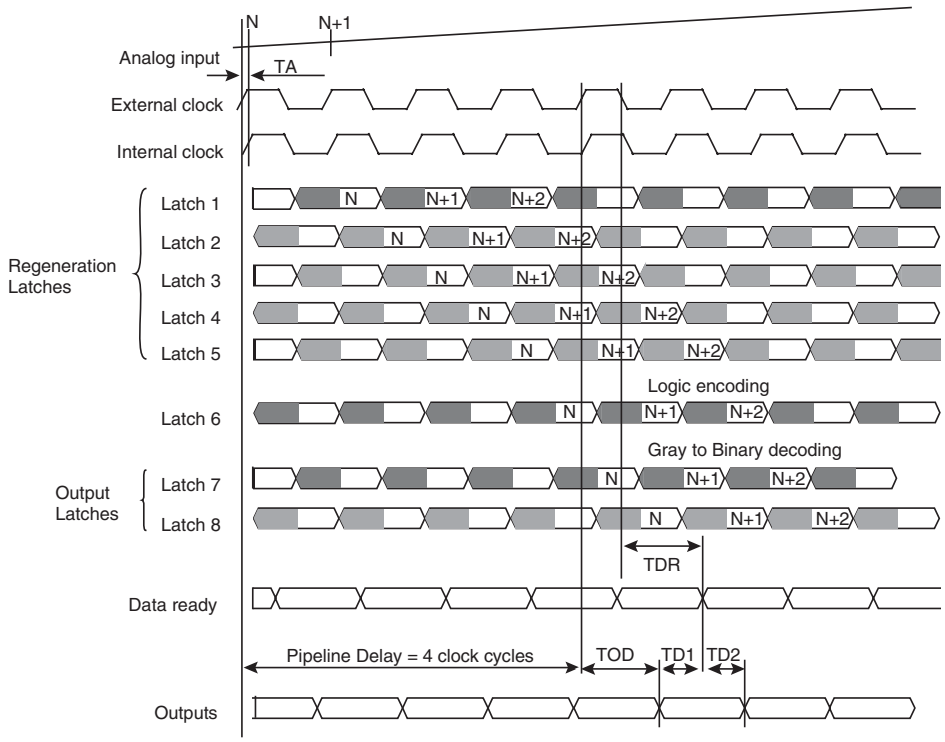
Level	Explanation
1	**100% production tested at 25°C (1) (for "C" temperature range) (2)**
2	100% production tested at 25°C (1) and sample tested at specified temperatures (for "M" temperature range (2))
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value guaranteed by design only
6	100% production tested over specified temperature range (for "B/Q" temperature range (2))

Note: 1. Unless otherwise specified

2. Refer to "Ordering Information" on page 52.

Only minimum and maximum values are guaranteed (typical values are issued from characterization results).

Figure 3-1. Timing Diagram



Note: Detailed timing diagrams are provided on page 37.

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Table 3-8. Digital Coding

Differential Analog Input	Voltage Level	Digital Output			
		Binary (B/GB = GND or floating) MSB……....LSB	Out-of-Range	GRAY (B/GB = V_{EE}) MSB……....LSB	Out-of-Range
> 250.25 mV	>Top end of full-scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1	1	1 0 0 0 0 0 0 0 0 0 0	1
250.25 mV	Top end of full-scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1	0	1 0 0 0 0 0 0 0 0 0 0	0
249.75 mV	Top end of full-scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 0	0	1 0 0 0 0 0 0 0 0 0 1	0
125.25 mV	3/4 full-scale + ½ LSB	1 1 0 0 0 0 0 0 0 0 0	0	1 0 1 0 0 0 0 0 0 0 0	0
124.75 mV	3/4 full-scale - ½ LSB	1 0 1 1 1 1 1 1 1 1 1	0	1 1 1 0 0 0 0 0 0 0 0	0
0.25 mV	Mid-scale + ½ LSB	1 0 0 0 0 0 0 0 0 0 0	0	1 1 0 0 0 0 0 0 0 0 0	0
-0.25 mV	Mid-scale - ½ LSB	0 1 1 1 1 1 1 1 1 1 1	0	0 1 0 0 0 0 0 0 0 0 0	0
–124.75 mV	1/4 full-scale + ½ LSB	0 1 0 0 0 0 0 0 0 0 0	0	0 1 1 0 0 0 0 0 0 0 0	0
–124.25 mV	1/4 full-scale - ½ LSB	0 0 1 1 1 1 1 1 1 1 1	0	0 0 1 0 0 0 0 0 0 0 0	0
–249.75 mV	Bottom end of full-scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 1	0	0 0 0 0 0 0 0 0 0 0 1	0
–250.25 mV	Bottom end of full-scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0	0
< –250.25 mV	< Bottom end of full-scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0 0 0 0	1

Table 3-9. Die Mechanical Information

Description	Data
Die size	3740 µm x 3820 µm (±15 µm)
Pad size - single pad - double pad	 90 µm x 90 µm 180 µm x 90 µm
Die thickness	380 µm ±25 µm
Back side metallization	None
Metallization - number of layers - material	 3 AlCu
Pad metallization	AlCu
Passivation	Oxyde nitride
Back side potential	–5V

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4. TS83102G0BMGS Package Description

Table 4-1. Pin Description (CI-CGA 152)

Symbol	Pin Number	Function
Power supplies		
V_{CC}, V_{CCTH}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	5V analog supply (connected to same power supply plane)
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analog ground
V_{EE}, V_{EETH}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	–5V analog supply (connected to same power supply plane)
V_{PLUSD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
DV_{EE}	A13, B13, C13, P13, Q13, R13, H14, J14	–5V digital supply
Analog inputs		
VIN	R5	In-phase (+) analog input signal of the differential Sample & Hold preamplifier
VINB	R6	Inverted phase (-) analog input signal of the differential Sample & Hold preamplifier
Clock Inputs		
CLK	E1	In-phase (+) clock input
CLKB	F1	Inverted phase (-) clock input
Digital Outputs		
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	D16, E16, F16, G16, J16, K16, L16, M16, N16, P16	In-phase (+) digital outputs D0 is the LSB, D7 is the MSB
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B	D15, E15, F15, G15, J15, K15, L15, M15, N15, P15	Inverted phase (-) digital outputs
OR	C16	In-phase (+) out-of-range output
ORB	C15	Inverted phase (-) out-of-range output
DR	H16	In-phase (+) data ready signal output
DRB	H15	Inverted phase (-) data ready signal output
Additional functions		
B/GB	A11	Binary or gray select output format control - Binary output format if B/GB is floating or connected to GND - Gray output format if B/GB is connected to V_{EE}

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Table 4-1. Pin Description (CI-CGA 152) (Continued)

Symbol	Pin Number	Function
DECB/DIODE	A10	Decimation function enable or die junction temperature measurement: - Decimation active when LOW (die junction temperature monitoring is not possible) - Normal mode when HIGH or left floating - Die junction temperature monitoring when current is applied
PGEB	A9	Active low pattern generator enable - Digitized input delivered at outputs according to B/GB if PGEB is floating or connected to GND - Checker board pattern delivered at outputs if PGEB is connected to V_{EE}
DRRB	N1	Asynchronous data ready reset function (active at ECL low level)
GA	R9	Gain adjust
SDA	A6	Sampling delay adjust
SDAEN	P1	Sampling delay adjust enable - Inactive if floating or connected to GND - Active if connected to V_{EE}

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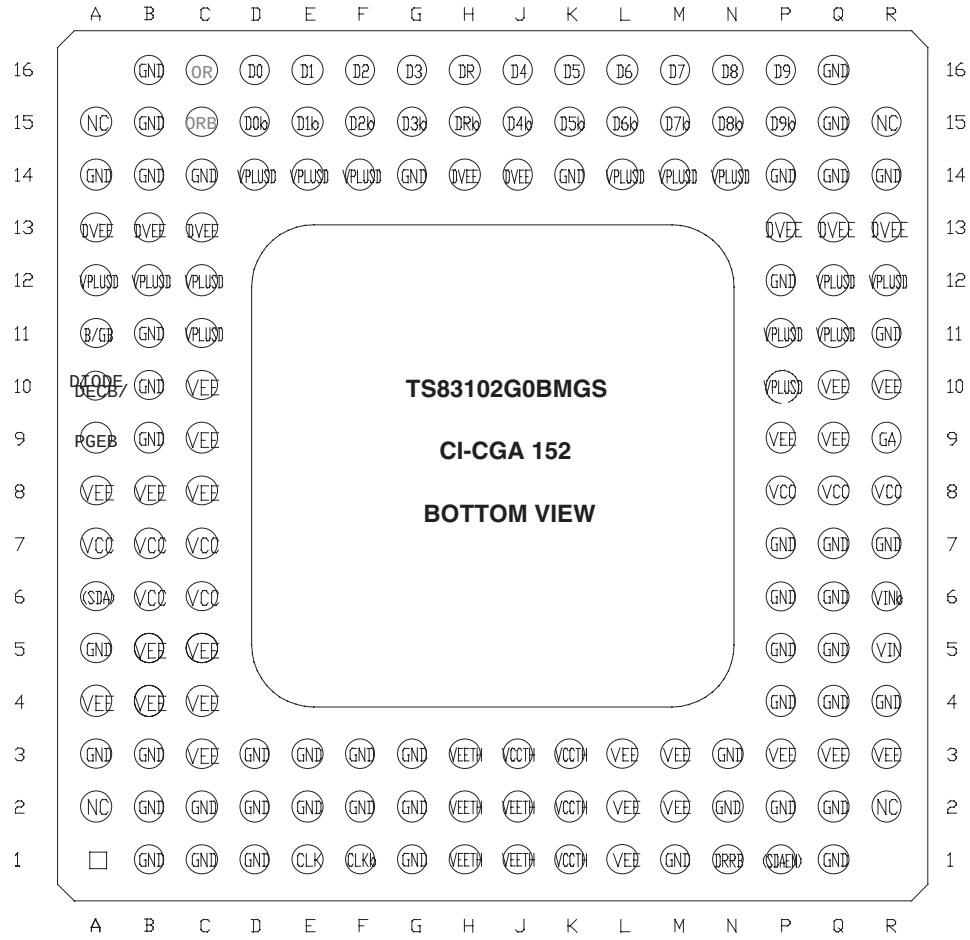
Figure 4-1. Pinout



Note: 1. To simplify PCB routing, the 4 NC columns can be electrically connected to the GND columns.

2. The pinout is shown from the bottom. The columns and rows are defined differently from the JEDEC standard.

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5. Thermal and Moisture Characteristics

5.1 Dissipation by Conduction and Convection

The thermal resistance from junction to ambient RTH_{JA} is around 30°C/W. Therefore, to lower RTH_{JA}, it is mandatory to use an external heat sink to improve dissipation by convection and conduction. The heat sink should be fixed in contact with the top side of the package (AI203 isolation over CuW heat spreader).

The heat sink does not need to be electrically isolated, because the top of the package is already electrically isolated thanks to a 0.30 mm AI203 layer.

Example:

The thermal resistance from case to ambient RTH_{CA} is typically 4.0°C/W (0 m/s air flow or still air) with the heat sink depicted in Figure 5-1 on page 17, of dimensions 50 mm x 50 mm x 28 mm (respectively L x l x H).

The global junction to ambient thermal resistance RTH_{JA} is:

– 4.8°C/W RTH_{JC} + 2.0°C/W thermal grease resistance + 4.0°C/W RTH_{CA} (case to ambient) = 10.8°C/W total (RTH_{JA}).

Assuming:

A typical thermal resistance from the junction to the top of the case RTH_{JC} of 4.35°C/W (finite element method thermal simulation results): this value does not include the thermal contact resistance between the package and the external heat sink (glue, paste, or thermal foil interface, for example). As an example, use a 2.0°C/W value for a
50 µm thickness of thermal grease.

Note: Example of the calculation of the ambient temperature T_A max to ensure T_J max = 110°C:
assuming RTH_{JA} = 10.8°C/W and power dissipation = 4.6 W, T_A max = T_J - (RTH_{JA} x 4.6 W) = 110 - (10.8 x 4.6) = 60.32°C. T_A max can be increased by lowering RTH_{JA} with an adequate air flow (2 m/s, for example).

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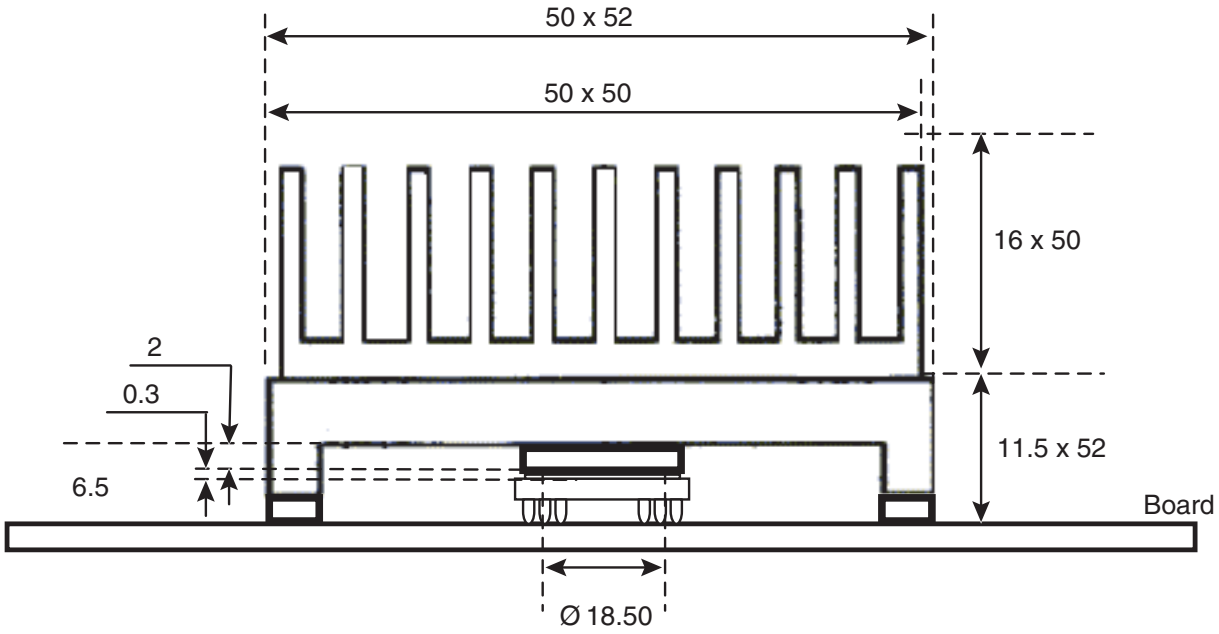
Figure 5-1. Black Anodized Aluminium Heat Sink Glued on a Copper Base Screwed on Board (all dimensions in mm)



Note: The cooling system efficiency can be monitored using the temperature sensing diodes, integrated in the device. Refer to "DECB/DIODE: Junction Temperature Monitoring and Output Decimation Enable" on page 44.

5.2 Thermal Dissipation by Conduction Only

When the external heat sink cannot be used, the relevant thermal resistance is the thermal resistance from the junction to the bottom of the columns: $RTH_{J\text{-}Bottom\text{-}of\text{-}columns}$.

The thermal path, in this case, is the junction, then the silicon, glue, CuW heat spreader, package Al2O3, and the columns (Sn10Pb90).

The Finite Element Method (FEM) with the thermal simulator leads to
$RTH_{J\text{-}bottom\text{-}of\text{-}columns}$ = 7.4°C/W. This value assumes pure conduction from the junction to the bottom of the columns (this is the worst case, no radiation and no convection is applied). With such an assumption, $RTH_{J\text{-}\ Bottom\text{-}of\text{-}columns}$ is user-independent.

To complete the thermal analysis, you must add the thermal resistance from the top of the board (on which the device is soldered) to the ambient resistance, whose values are user-dependent (the type of board, thermal, routing, area covered by copper in each board layer, thickness, airflow or cold plate are all parameters to consider).

In the case of the CI-CGA 152 package, the thermal resistance from the junction to the top of the package (via the CuW heat spreader covered by Al203) is
$RTH_{J\text{-}top\text{-}of\text{-}package}$ = 4.8°C/W.

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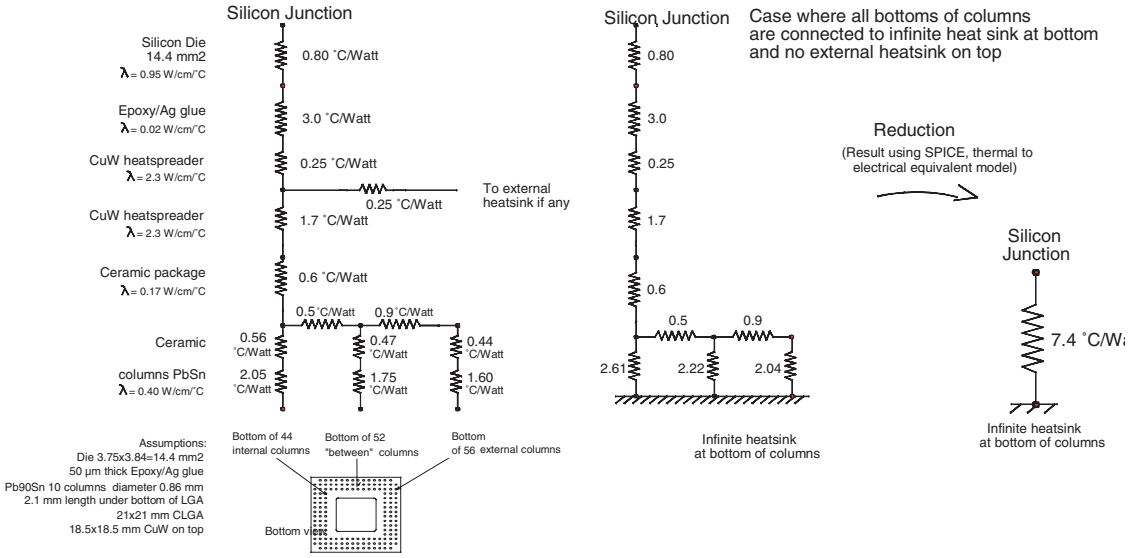
Figure 5-2. Thermal Net



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6. Typical Characterization Results

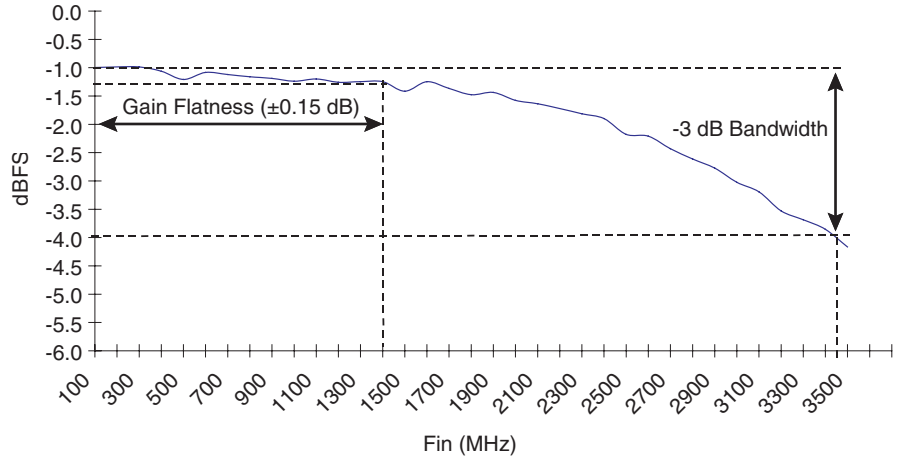
6.1 Nominal Conditions

V_{CC} = 5V; 50% clock duty cycle; binary output data format; T_J = 80°C; -1 dBFS, unless otherwise specified.

6.1.1 Typical Full Power Input Bandwidth

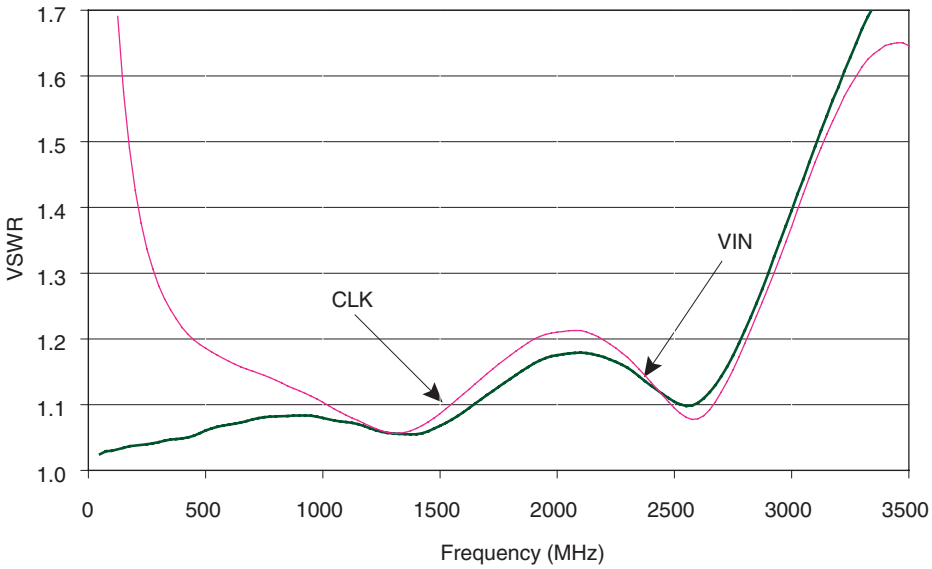
Vin = –1 dBFS
Gain flatness at ±0.15 dB from DC to 1.5 GHz
Full power input bandwidth at –3 dB > 3.3 GHz

Figure 6-1. Full Power Input Bandwidth at –3 dB



6.1.2 Typical VSWR vs. Input Frequency

Figure 6-2. VSWR Curve for VIN and CLK



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6.1.3 Typical Step Response

Tr measured = 90 ps = sqrt ($Tr_{PulseGenerator}^2$+Tr_{ADC}^2)
$Tr_{PulseGenerator}$ = 41 ps (estimated)
Actual Tr_{ADC} = 80 ps

Figure 6-3. Step Response (Random Interleaved Sampling Method Measure)

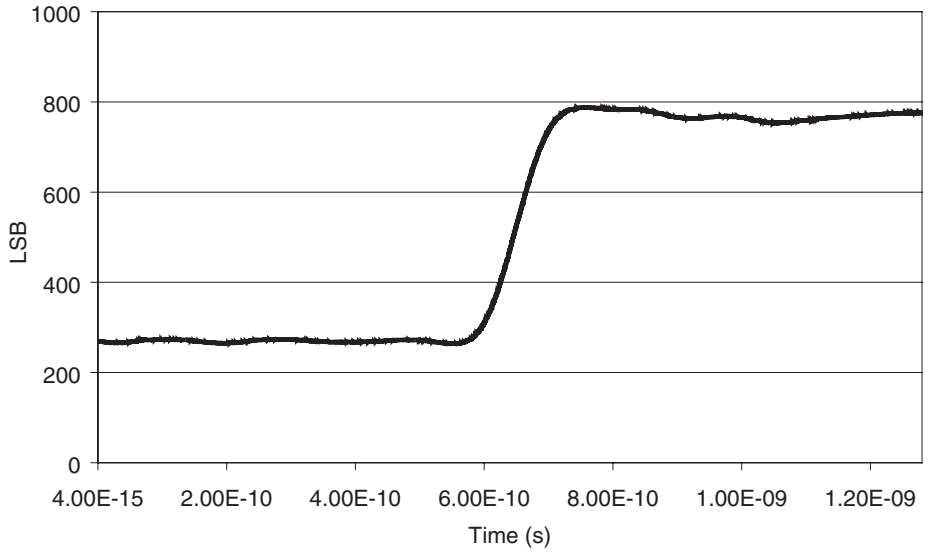
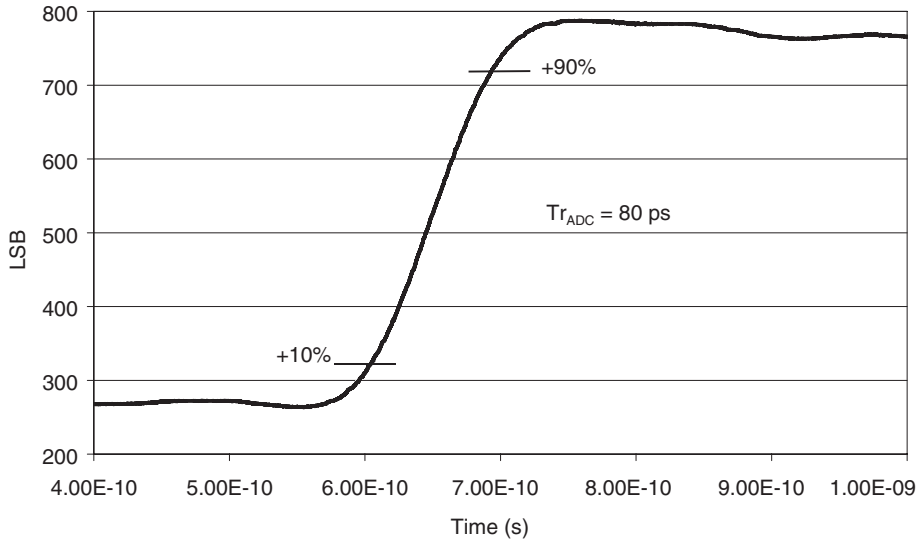


Figure 6-4. Zoom on Rise Time Step Response



Note: Overshoot and ringback are not measurable (estimated by simulation at 4% and 2% respectively).

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6.1.4 Typical Dynamic Performances vs. Sampling Frequency

Figure 6-5. ENOB vs. Sampling Frequency in Nyquist Conditions (Fin = Fs/2)

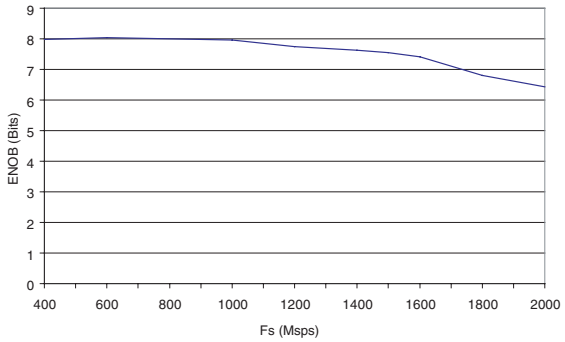


Figure 6-6. SFDR vs. Sampling Frequency in Nyquist Conditions (Fin = Fs/2)

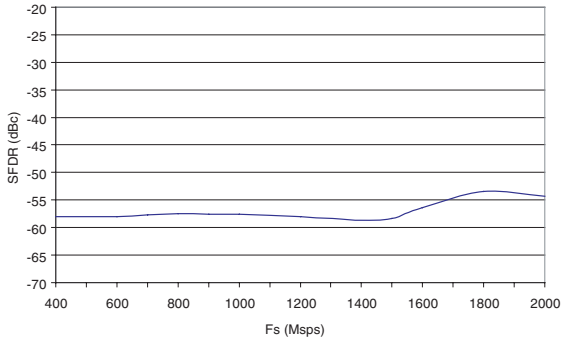


Figure 6-7. THD vs. Sampling Frequency in Nyquist Conditions (Fin = Fs/2)

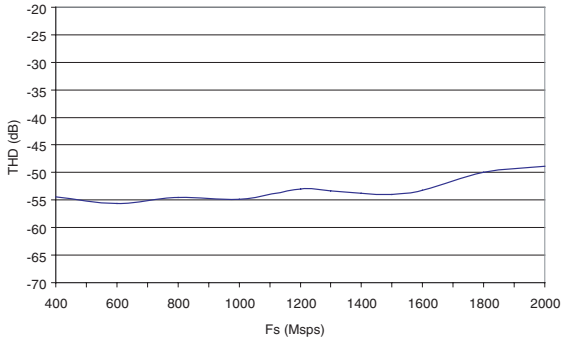
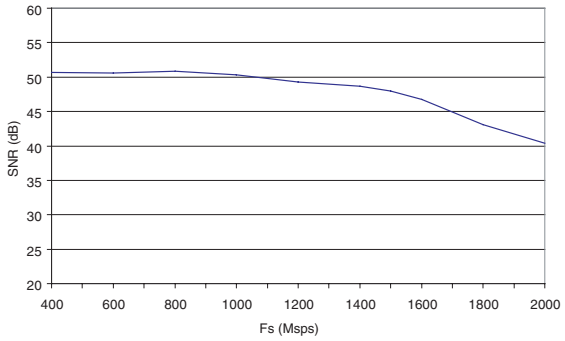


Figure 6-8. SNR vs. Sampling Frequency in Nyquist Conditions (Fin = Fs/2)



6.1.5 Typical Dynamic Performances vs. Fin

Figure 6-9. ENOB vs. Input Frequency at Fs = 1.4 Gsps and Fs = 1.7 Gsps

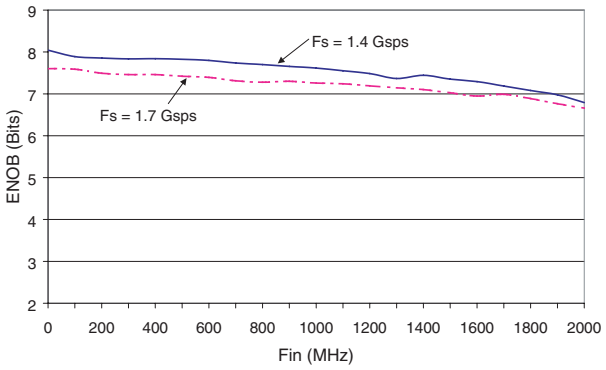


Figure 6-10. THD vs. Input Frequency at Fs = 1.4 Gsps and Fs = 1.7 Gsps

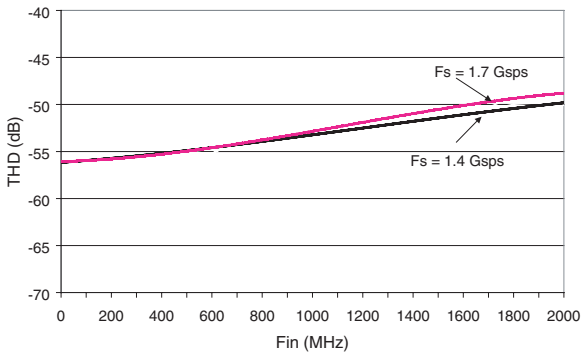


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Figure 6-11. SFDR vs. Input Frequency at Fs = 1.4 Gsps and Fs = 1.7 Gsps

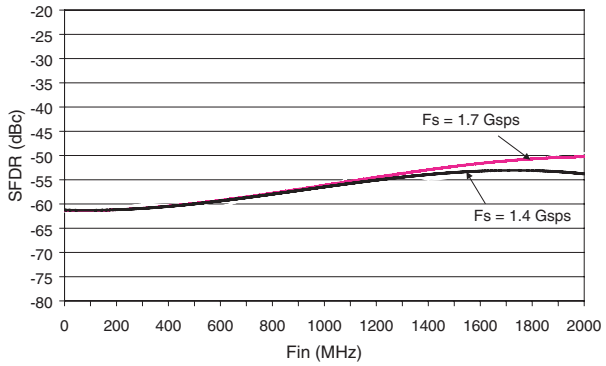
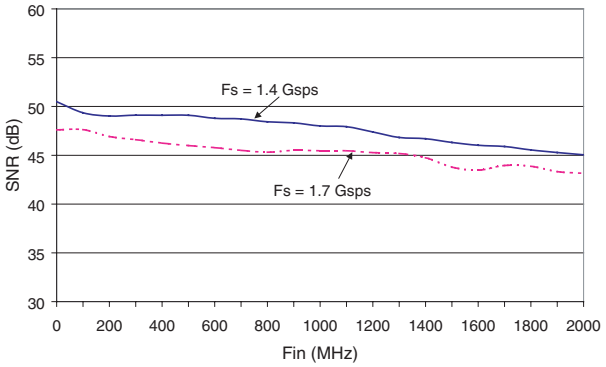


Figure 6-12. SNR vs. Input Frequency at Fs = 1.4 Gsps and Fs = 1.7 Gsps

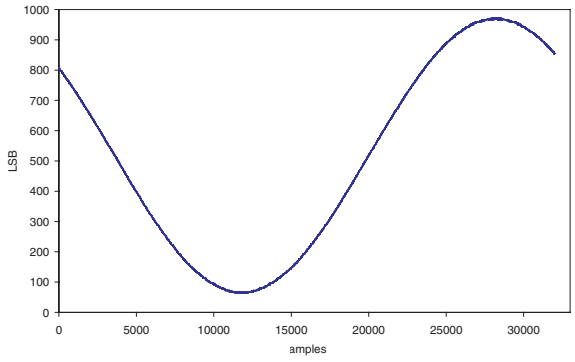


6.1.6 Typical Reconstructed Signals and Signal Spectrum

The ADC input signal is sampled at a full sampling rate, but the output data is 8 or 16 times decimated so as to relax the acquisition system data rate. As a consequence, the calculation software sees an effective frequency divided by 8 or 16, compared to the ADC clock frequency used (Fs).

This does not have any impact on the FFT spectral characteristics because of the ergodicity of the samples (time average = statistic average). The input frequency is chosen to respect the coherence of the acquisition. The spectrum is displayed from DC to Fs/2.

Figure 6-13. Fs = 1.4 Gsps and Fin = 702 MHz, –1 dBFS; Decimation Factor = 8, 32 kpoints FFT



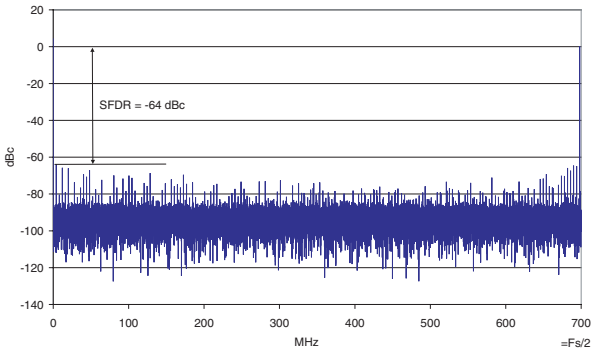


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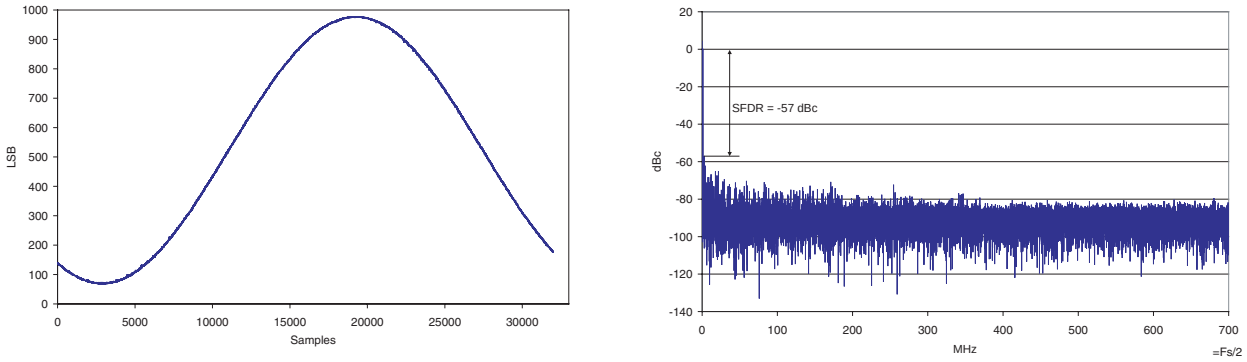
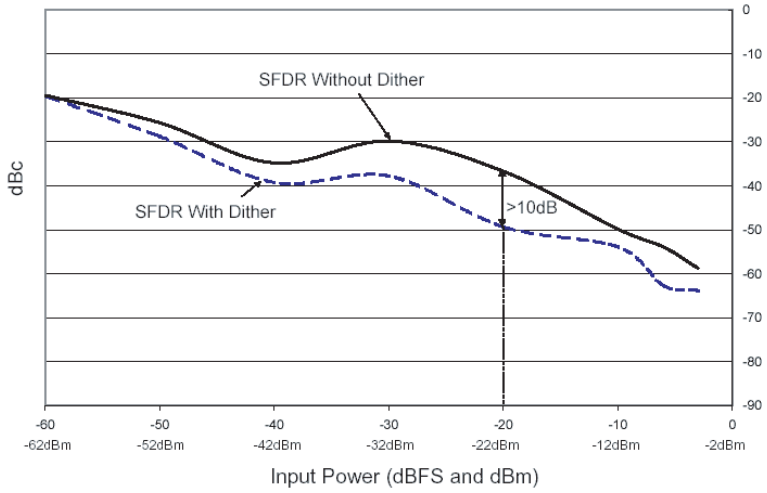
Figure 6-14. Fs = 1.4 Gsps and Fin = 1399 MHz, –1 dBFS; Decimation Factor = 8, 32 kpoints FFT



6.1.7 SFDR Performance with/without External Dither

Figure 6-15. SFDR (in dBC) With and Without Dither (–23 dBm DC to 5 MHz Out of Band Dither) Fs = 1.4 Gsps and Fin = 710 MHz



An increase in SFDR up to >10 dB with an addition of –23 dBrms DC to 5 MHz out-of-band dither is noted.

The dither profile has to be defined according to the ADC's INL pattern as well as the trade-off to be reached between the increase in SFDR and the loss in SNR.

Please refer to the Application Note reference 0868 on dither for more information on adding dither to an ADC.

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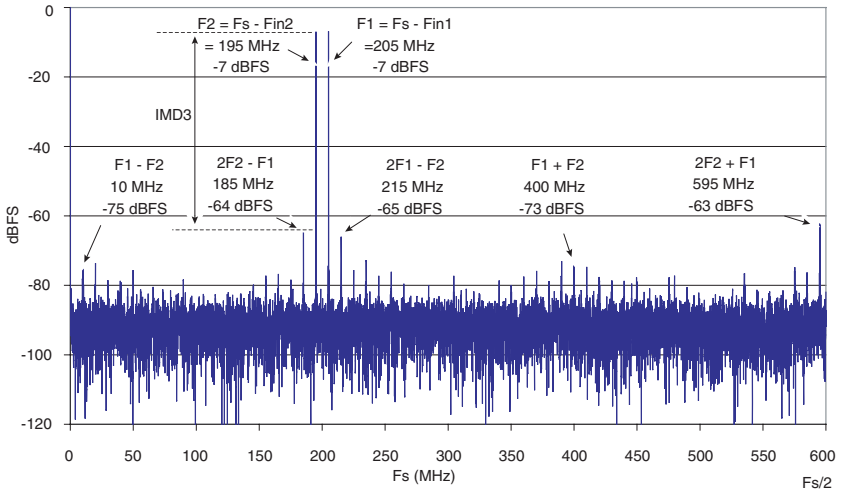
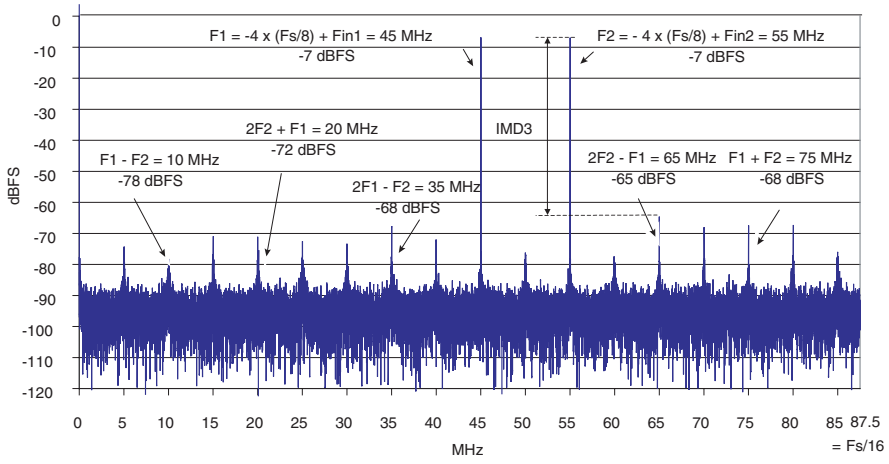
6.1.8 Typical Dual Tone Dynamic Performance

Figure 6-16. Dual Tone Reconstructed Signal Spectrum at Fs = 1.2 Gsps, Fin1 = 995 MHz, Fin2 = 1005 MHz (–7 dBFS), IMD3 = 64 dBFS



Note: The output data is not decimated. The spectrum is displayed from DC to 600 MHz.

Figure 6-17. Dual Tone Reconstructed Signal Spectrum at Fs = 1.4 Gsps, Fin1 = 745 MHz, Fin2 = 755 MHz (–7 dBFS), IMD3 = 65 dBFS



Note: The ADC input signal is sampled at 1.4 Gsps but the data acquisition is 8 times decimated. Thus, the spectrum is displayed from DC to Fs/2 divided by the decimation factor [(Fs/2)/8 = 87.5 MHz].

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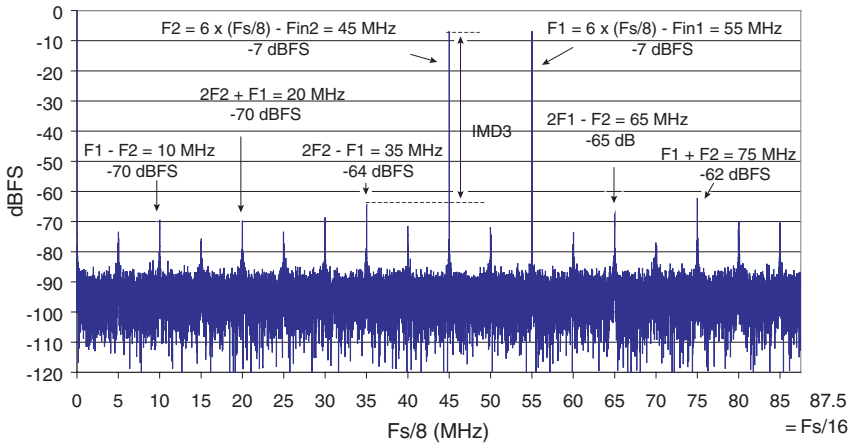
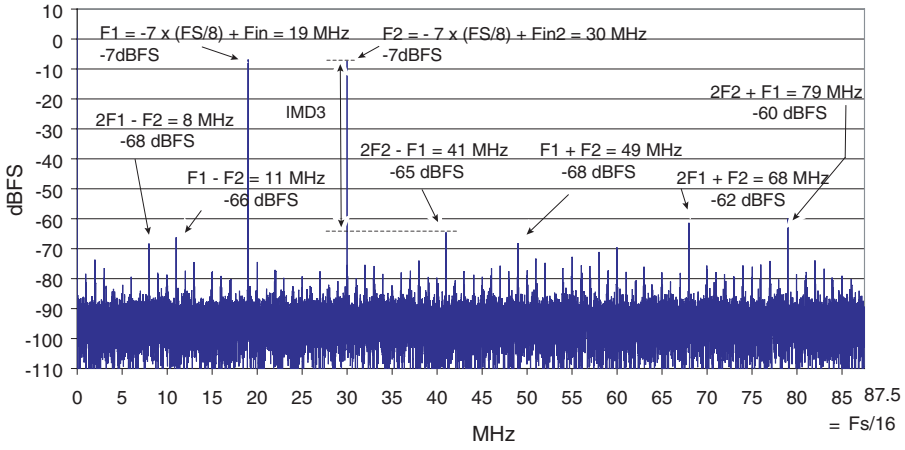
Figure 6-18. Dual Tone Reconstructed Signal Spectrum at Fs = 1.4 Gsps, Fin1 = 995 MHz, Fin2 = 1005 MHz (–7 dBFS), IMD3 = 64 dBFS



Note: The ADC input signal is sampled at 1.4 Gsps but the data acquisition is 8 times decimated. Thus, the spectrum is displayed from DC to Fs/2 divided by the decimation factor [(Fs/2)/8 = 87.5 MHz].

Figure 6-19. Dual Tone Reconstructed Signal Spectrum at Fs = 1.4 Gsps, Fin1 = 1244 MHz, Fin2 = 1255 MHz (–7 dBFS), IMD3 = 65 dBFS



Note: The ADC input signal is sampled at 1.4 Gsps but data acquisition is 8 times decimated. Thus, the spectrum is displayed from DC to Fs/2 divided by the decimation factor [(Fs/2)/8 = 87.5 MHz]. The dual tone IMD3 at 1.4 Gsps is around –65 dBFS for Fin = 1 GHz ± 250 MHz (Fin range is from 750 MHz to 1250 MHz).

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6.2 Typical Performance Sensitivity vs. Power Supply and Temperature

Figure 6-20. ENOB vs. Junction Temperature (Fs = 1.4 Gsps, Fin = 698 MHz, –1 dBFS)

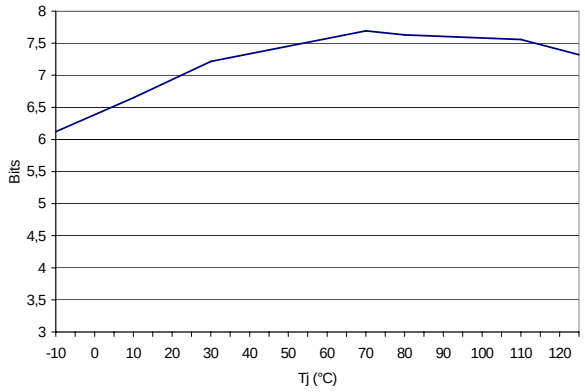


Figure 6-21. SFDR vs. Junction Temperature (Fs = 1.4 Gsps, Fin = 698 MHz, –1 dBFS)

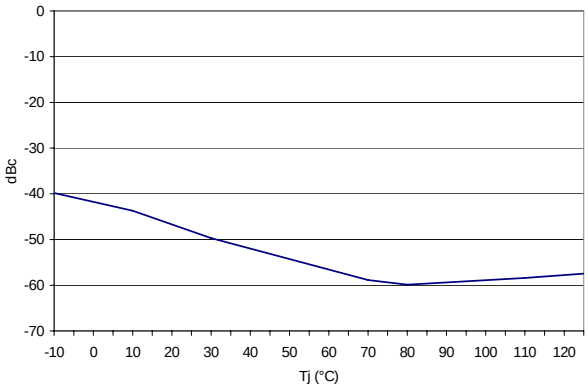


Figure 6-22. SNR vs. Junction Temperature (Fs = 1.4 Gsps, Fin = 698 MHz, –1 dBFS)

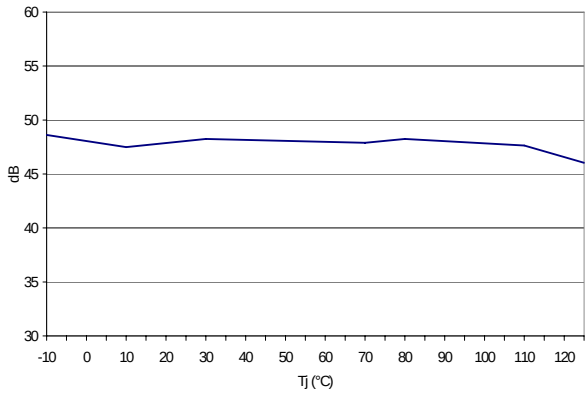


Figure 6-23. ENOB vs. V_{CC} and V_{EE}; Fs = 1.4 Gsps vs. Fin (V_{CC} = IV_{EE}I = 4.75V, 5V and 5.25V)

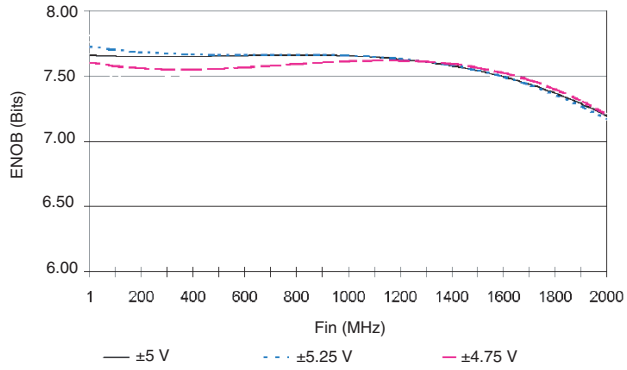


Figure 6-24. SFDR vs. V_{CC} and V_{EE}; Fs = 1.4 Gsps vs. Fin (V_{CC} = IV_{EE}I = 4.75V, 5V and 5.25V)

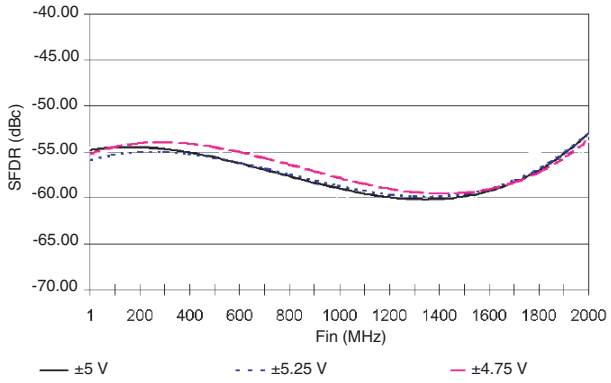
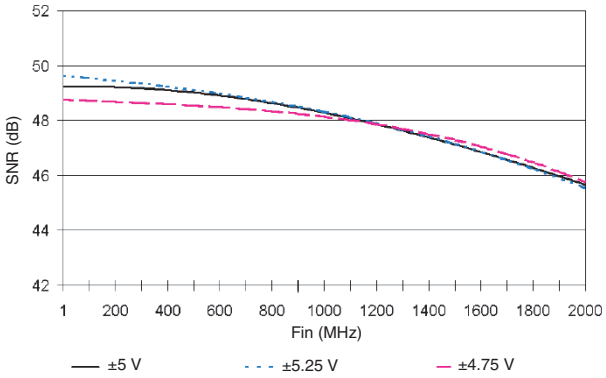


Figure 6-25. SNR vs. V_{CC} and V_{EE}; Fs = 1.4 Gsps vs. Fin (V_{CC} = IV_{EE}I = 4.75V, 5V and 5.25V)



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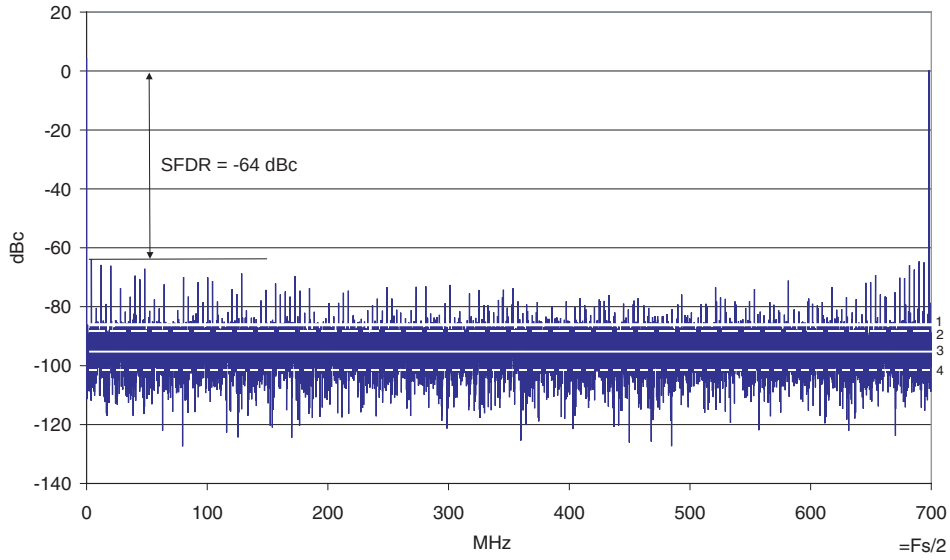
6.3 Considerations on ENOB: Linearity and Noise Contribution

Figure 6-26. Example of a 16-kpoint FFT Computation at Fs = 1.4 Gsps, Fin = 702 MHz, –1dBFS, T_J = 80°C; Bin Spacing = (Fs/2) / 16384 = 2.67 kHz



This is a 16384 points FFT. It is 16 times decimated since a DEMUX 1:8 is used to relax the acquisition system data rate, and data is captured on the rising edge of the data ready signal.

The spectrum is computed over the first Nyquist zone from DC to Fs/2.

Legend:

1. Ideal 10-bit quantization noise spectral density, peak value = –84 dB
2. Average SNR noise floor: 47 dB + 10 log ($N_{FFTpoint}$/2) = 86 dB including thermal noise
3. Average SNR noise floor: 57 dB + 10 log ($N_{FFTpoint}$/2) = 96 dB without thermal noise
4. Ideal 10-bit averaged SNR noise floor 6.02 x (N = 10) + 1.76 + 10 log ($N_{FFTpoint}$/2) = 101 dB

Note: The thermal noise floor is expressed in dBm/Hz (at T = 300 K, B = 1 Hz): 10 log (kTB/1 mW) = –174 dBm/Hz or –139.75 dBm/2.67 kHz. THD is calculated over the 25 first harmonics.

With ADC input referred thermal noise:

- ENOB = 7.8 bits
- THD = –55.4 dB (over 25 harmonics)
- SFDR = –64 dBc
- SNR = 48.8 dB

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Without ADC input referred thermal noise:

- ENOB = 9.2 bits
- SINAD = 57 dB
- THD = –55.7 dB (over 25 harmonics)
- SFDR = –62.6 dBc
- SNR = 57.3 dB

Conclusion:

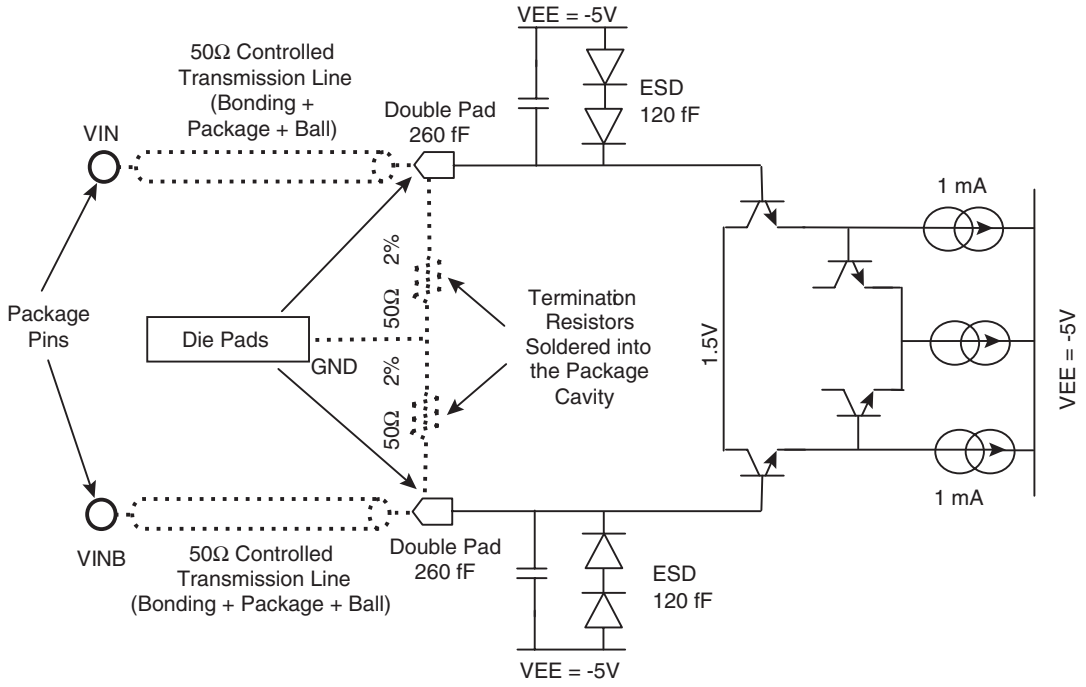
Though the ENOB is 7.8 bits (in this example at 1.4 Gsps Nyquist conditions), the ADC features a 10-bit linearity regarding the 60 dB typical SFDR performance.

However, it has to be pointed out that the ENOB is actually limited by the ADC's input referred thermal noise, which dominates the rms quantization noise. For certain applications (using a spread spectrum) the signal may be recovered below the thermal noise floor (by cross correlation since it is white noise).

Therefore, the thermal noise can be extracted from the ENOB: the ENOB without a referred input thermal noise is 9.2 instead of 7.8 in this example, only limited by the quantization noise and clock induced jitter.

7. Equivalent Input/Output Schematics

Figure 7-1. Equivalent Analog Input Circuit and ESD Protections



Note: 100Ω termination midpoint is located inside the package cavity and is DC coupled to ground.

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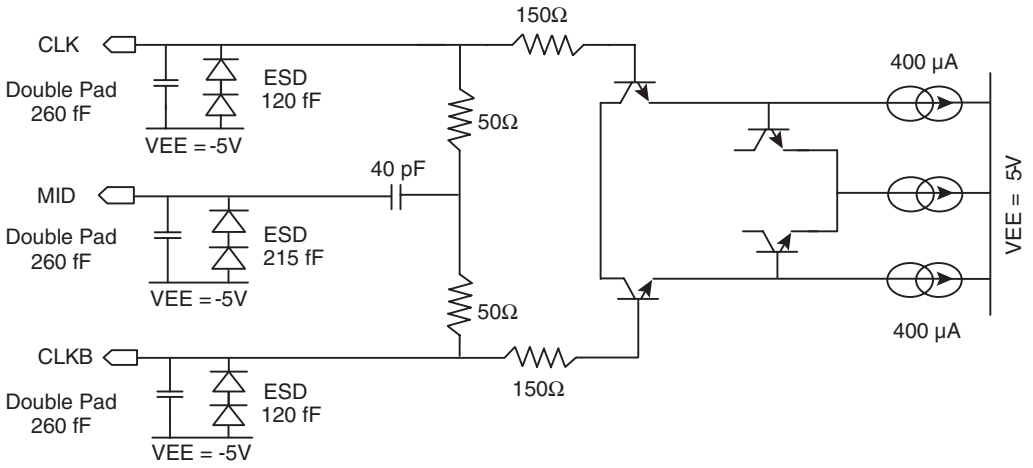
Figure 7-2. Equivalent Clock Input Circuit and ESD Protections



Note: 100Ω termination midpoint is on-chip and AC coupled to ground through a 40 pF capacitor.

Figure 7-3. Equivalent Data Output Buffer Circuit and ESD Protections

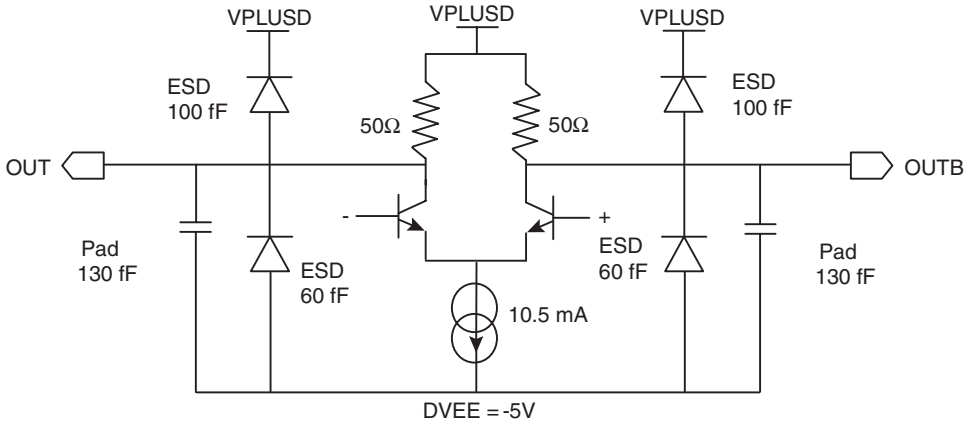


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Figure 7-4. ADC Gain Adjust Equivalent Input Circuits and Protections

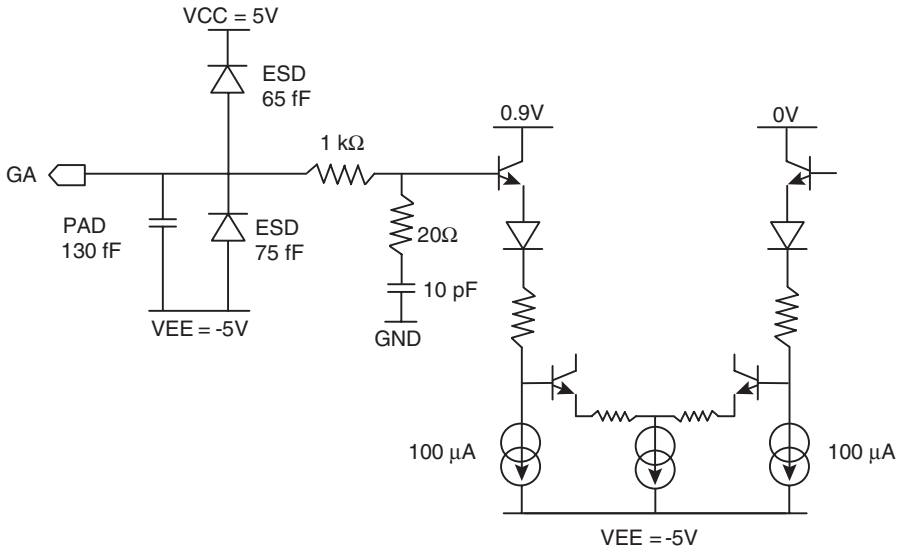


Figure 7-5. B/GB and PGEB Equivalent Input Schematics and ESD Protections

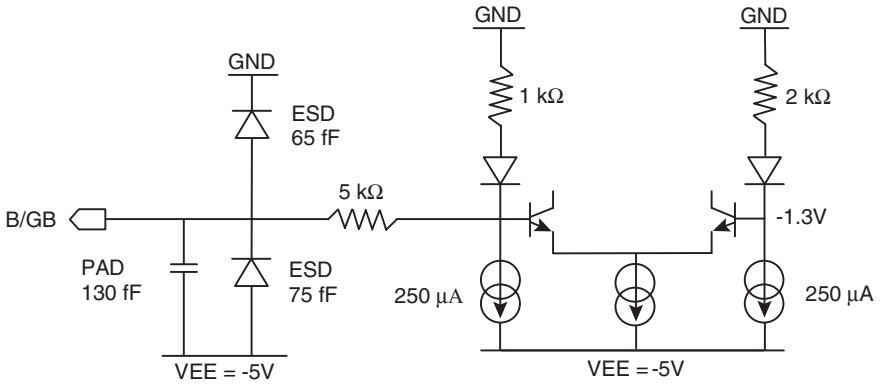
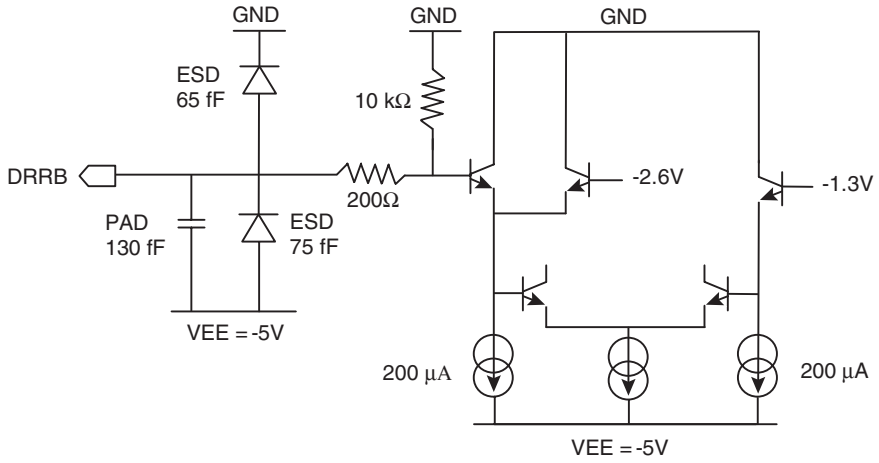


Figure 7-6. DRRB Equivalent Input Schematics and ESD Protections



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8. Definition of Terms

Table 8-1. Definitions of Terms

Term		Description
BER	Bit Error Rate	Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than ±4 LSB from the correct code
BW	Full-power Input Bandwidth	The analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale
DG	Differential Gain	The peak gain variation (in percent) at five different DC levels for an AC signal of 20% full-scale peak to peak amplitude. F_{IN} = 5 MHz (TBC)
DNL	Differential Nonlinearity	The differential nonlinearity for an output code (i) is the difference between the measured step size of code (i) and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic
DP	Differential Phase	The peak phase variation (in degrees) at five different DC levels for an AC signal of 20% full-scale peak to peak amplitude. F_{IN} = 5 MHz (TBC)
FS MAX	Maximum Sampling Frequency	Sampling frequency for which ENOB < 6 bits
FS MIN	Minimum Sampling Frequency	Sampling frequency for which the ADC gain has fallen by 0.5 dB with respect to the gain reference value. Performances are not guaranteed below this frequency
FPBW	Full Power Input Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale –1 dB (–1 dBFS)
ENOB	Effective Number of Bits	$ENOB = \frac{SINAD - 1{,}76 + 20\log\frac{A}{Fs/2}}{6{,}02}$ Where A is the actual input amplitude and V is the full-scale range of the ADC under test
IMD3	Intermodulation Distortion	The two tones third order intermodulation distortion (IMD3) rejection is the ratio of either input tone to the worst third order intermodulation products
INL	Integral Nonlinearity	The integral nonlinearity for an output code (i) is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all INL (i)
JITTER	Aperture Uncertainty	The sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point
NPR	Noise Power Ratio	The NPR is measured to characterize the ADC's performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise-to-Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test
NRZ	Non Return to Zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the out-of-range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the out-of-range bit is set to logic one (it is assumed that the input signal amplitude remains within the absolute maximum ratings)
ORT	Overvoltage Recovery Time	Time to recover 0.2% accuracy at the output, after a 150% full-scale step applied on the input is reduced to midscale
PSRR	Power Supply Rejection Ratio	PSRR is the ratio of input offset variation to a change in power supply voltage

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Table 8-1. Definitions of Terms (Continued)

SFDR	Spurious Free Dynamic Range	The ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (radar systems, digital receiver, network analyzer...). It may be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (i.e. always related back to converter full-scale)
SINAD	Signal to Noise and Distortion Ratio	The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components, including the harmonics except DC
SNR	Signal to Noise Ratio	The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components excluding the first five harmonics
SSBW	Small Signal Input Bandwidth	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale –10 dB (–10 dBFS)
TA	Aperture Delay	The delay between the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point), and the time at which (V_{IN}, V_{INB}) is sampled
TC	Encoding Clock Period	TC1 = minimum clock pulse width (high) TC = TC1 + TC2 TC2 = minimum clock pulse width (low)
TD1	Time Delay from Data to Data Ready	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period
TD2	Time Delay from Data Ready to Data	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period
TF	Fall Time	Time delay for the output data signals to fall from 80% to 20% of delta between low level and high level
THD	Total Harmonic Distortion	The ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component
TOD	Digital Data Output Delay	The delay from the falling edge of the differential clock inputs (CLK, CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with a specified load
TPD	Pipeline Delay	The number of clock cycles between the sampling edge of an input data and the associated output data being made available (not taking in account the TOD). For the JTS8388B the TPD is 4 clock periods
TR	Rise Time	Time delay for the output data signals to rise from 20% to 80% of delta between the low level and high level
TRDR	Data Ready Reset Delay	Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR)
TS	Settling Time	Time delay to achieve 0.2% accuracy at the converter output when an 80% full-scale step function is applied to the differential analog input
VSWR	Voltage Standing Wave	$VSWR = (1 + S_{11}) \div (1 - S_{11})$ Where S11 is the reflection coefficient of the scattering matrix. The VSWR over frequency measures the degree of mismatching between the packaged ADC input impedance (ideally 50 Ω or so) and the transmission line's impedance. The packaged ADC input impedance (transmission line and termination) is controlled so as to ensure VSWR < 1.2 :1 from DC up to 2.5 GHz. A VSWR of 1.2 :1 corresponds to a 0.039 dB insertion loss (20 dB return loss) that is 99% power transmitted and 1% reflected

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9. TS83102G0BMGS Operating Features

9.1 Timing Information

9.1.1 Timing Value for TS83102G0BMGS

The timing values are defined in the “Electrical Operating Characteristics” on page 4.

The timing values are given at the package inputs/outputs, taking into account the package’s transmission line, bond wire, pad and ESD protections capacitance, as well as specified termination loads. The evaluation board propagation delays in 50Ω controlled impedance traces are not taken into account. You should apply proper derating values corresponding to termination topology.

9.1.2 Propagation Time Considerations

The TOD and TDR timing values are given from the package pin to pin and do not include the additional propagation times between the device pins and input/output termination loads. For the evaluation board, the propagation time delay is 6.1 ps/mm (155 ps/inch) corresponding to a 3.4 dielectric constant (at 10 GHz) of the RO4003 used for the board.

If a different dielectric layer is used (for instance Teflon), you should use appropriate propagation time values.

TD1 and TD2 do not depend on propagation times because they are differential data (see “Definition of Terms” on page 33).

TD1 and TD2 are also the most straightforward data to measure, because they are differential: TD can be measured directly on the termination loads, with matching oscilloscope probes.

9.1.3 TOD-TDR Variation Over Temperature

Values for TOD and TDR track each other over the temperature (there is a 1% variation for TOD and TDR per 100°C temperature variation). Therefore the TOD and TDR variation over temperature is negligible. Moreover, the internal (on-chip) skews between each TOD and TDR data effect can be considered negligible. Consequently, the minimum values for TOD and TDR are never more than 100 ps apart. The same is true for their maximum values.

However, the external TOD and TDR values can be dictated by the total digital data skews between each TOD and TDR. These digital skews can include the MCM board, bonding wires and output line length differences, as well as output termination impedance mismatches.

The external (on-board) skew effect has not been taken into account for the specification of TOD and TDR minimum and maximum values.

9.1.4 Principle of Operation

The analog input is sampled on the rising edge of the external clock’s input (CLK/CLKB) after TA (aperture delay). The digitized data is available after 4 clock periods’ latency (pipeline delay [TPD]) on the clock’s rising edge, after a typical propagation delay TOD. The Data Ready differential output signal frequency (DR/DRB) is half the external clock’s frequency. It switches at the same rate as the digital outputs. The Data Ready output signal (DR/DRB) switches on the external clock’s falling edge after a propagation delay TDR.

If TOD equals TDR, the rising edge (True-False) of the differential Data Ready signal is placed in the middle of the Output Data Valid window. This gives maximum setup and hold times for external data acquisition.

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A Master Asynchronous Reset input command DRRB (ECL compatible single-ended input) is available for initializing the differential Data Ready output signal (DR/DRB). This feature is mandatory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Without Data Ready signal initialization, it is impossible to store the output digital data in a defined order.

When used with e2v's TS81102G0 1:4/8 8/10 bit DMUX, it is not necessary to initialize Data Ready, as this device can start on either clock edge.

9.2 Principle of Data Ready Signal Control by DRRB Input Command

9.2.1 Data Ready Output Signal Reset

The Data Ready signal is reset on the DRRB input command's falling edge, on the ECL logical low level (–1.8V). DRRB may also be tied to V_{EE} = –5V for the Data Ready output signal master reset. As long as DRRB remains at a logical low level, (or tied to V_{EE} = –5V), the Data Ready output remains at a logical zero and is independent of the external free-running encoding clock.

The Data Ready output signal (DR/DRB) is reset to a logical zero after TRDR.

TRDR is measured between the –1.3V point of the DRRB input command's falling edge and the zero crossing point of the differential Data Ready output signal (DR/DRB).The Data Ready Reset command may be a pulse of 1 ns minimum time width.

9.2.2 Data Ready Output Signal Restart

The Data Ready output signal restarts on the DRRB command's rising edge, on the ECL logical high level (–0.8V).

DRRB may also be grounded, or may float, for normal free-running of the Data Ready output signal. The Data Ready signal's restart sequence depends on the logical level of the external encoding clock, at a DRRB rising edge instant:

- The DRRB's rising edge occurs when the external encoding clock input (CLK/CLKB) is LOW : the Data Ready output's first rising edge occurs after half a clock period on the clock's falling edge, and a TDR delay time of 410 ps, as defined above.
- The DRRB's rising edge occurs when the external encoding clock input (CLK/CLKB) is HIGH : the Data Ready output's first rising edge occurs after one clock period on the clock's falling edge, and a TDR delay time of 410 ps.

Consequently, as the analog input is sampled on the clock's rising edge, the first digitized data corresponding to the first acquisition (N), after a Data Ready signal restart (rising edge), is always strobed by the third rising edge of the Data Ready signal.

The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR/DRB) [zero crossing point].

Note: For normal initialization of the Data Ready output signal, the external encoding clock signal frequency and level must be controlled. The minimum encoding clock sampling rate for the ADC is 150 Msps, due to the internal Sample and Hold drop rate. Consequently the clock cannot be stopped.

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9.2.3 Timing Diagram

Figure 9-1. TS83102G0BMGS Timing Diagram (2 Gsps Clock Rate) - Data Ready Reset Clock Held at LOW Level

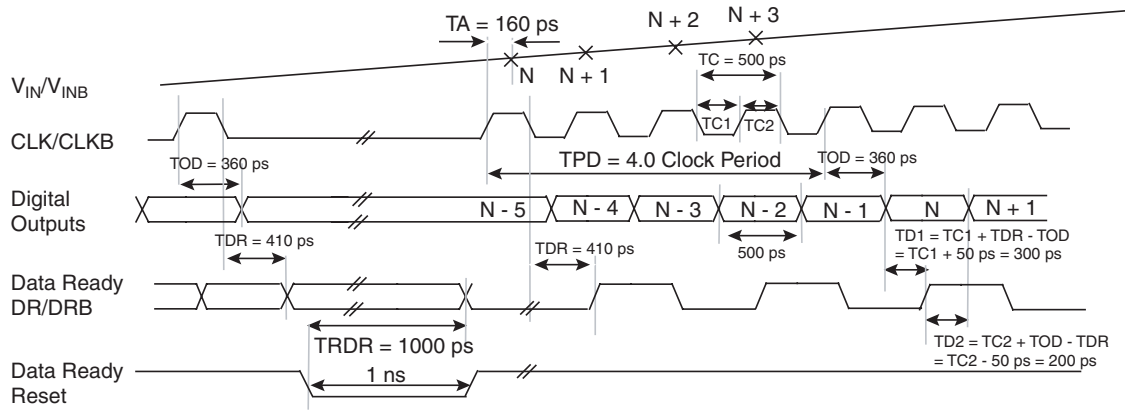
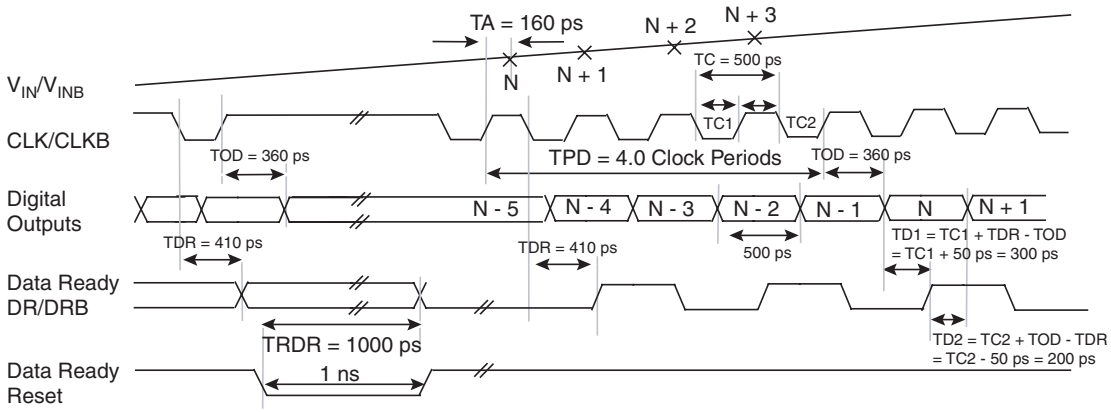


Figure 9-2. TS83102G0BMGS Timing Diagram (2 Gsps Clock Rate) - Data Ready Reset Clock Held at HIGH Level



9.3 Analog Inputs (VIN/VINB)

9.3.1 Static Issues: Differential vs. Single-ended (Full-scale Inputs)

The ADC's front-end Track and Hold differential preamplifier has been designed to be entered either in differential or single-ended mode, up to the maximum operating speed of 2.2 Gsps, without affecting dynamic performances (it does not require a single to differential balun).

In a single-ended input configuration, the in-phase full-scale input amplitude is 0.5V peak-to-peak, centered on 0V (or –2 dBm into 50Ω).

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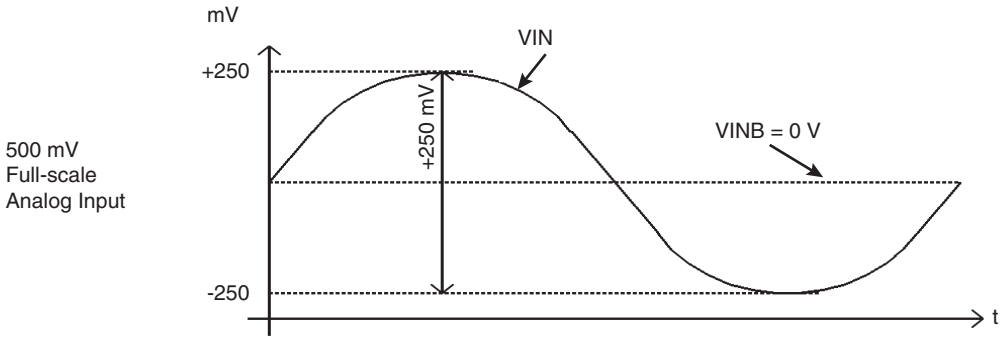
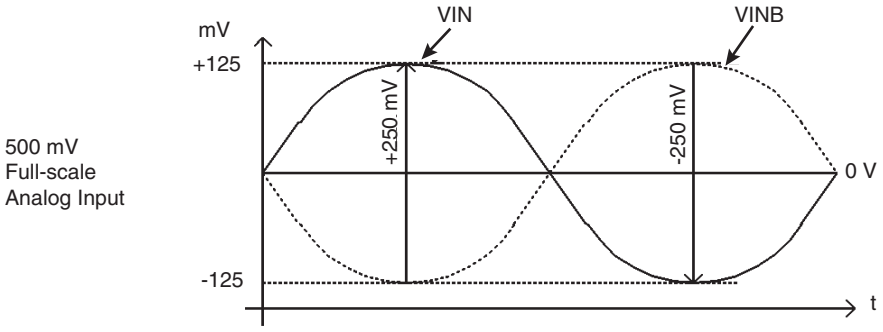
Figure 9-3. Typical Single-ended Analog Input Configuration (Full-scale)



The analog full-scale input range is 0.5V peak-to-peak (Vpp), or –2 dBm into the 50Ω (100Ω differential) termination resistor.

In the differential mode input configuration, this means 0.25V on each input, or ±125 mV around 0V. The input common mode is ground.

Figure 9-4. Differential Inputs Voltage Span (Full-scale)



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9.3.2 Dynamic Issues: Input Impedance and VSWR

The TS83102G0BMGS analog input features a 100Ω (±2%) differential input impedance (2 x 50Ω // 0.3 pF). Each analog input (VIN,VINB) is terminated by 50Ω single-ended (100Ω differential) resistors (±2% matching) soldered into the package cavity.

The transmission lines of the ADC package's analog inputs feature a 50Ω controlled impedance. Each single-ended die input pad capacitance (taking into account the ESD protection) is 0.3 pF. This leads to a global input VSWR (including ball, package and bonding) of less than 1.2 from DC up to 2.5 GHz.

9.4 Clock Inputs (CLK/CLKB)

The TS83102G0BMGS clock inputs are designed for either single-ended or differential operation. The device's clock inputs are on-chip 100Ω (2 x 50Ω) differentially terminated. The termination mid point is AC coupled to ground through a 40 pF on-chip capacitor. Therefore, either ground or different common modes can be used (ECL, LVDS).

Note: As long as V_{IH} remains below the 1 V peak, the ADC clock can be DC coupled. If V_{IH} is higher than the 1V peak, it is necessary to AC couple the signal via 100 pF capacitors, for example, and to bias CLK and CLKB:
- CLK biased to ground via a 10 kΩ resistor
- CLKB biased to ground via a 10 kΩ resistor and to V_{EE} via a 100 kΩ resistor.

However, logic ECL or LVDS square wave clock generators are not recommended because of poor jitter performances. Furthermore, the propagation times of the biasing tees used to offset the common mode voltage to ECL or LVDS levels may not match. A very low-phase noise (low jitter) sinewave input signal should be used for enhanced SNR performance, when digitizing high frequency analog inputs. Typically, when using a sinewave oscillator featuring a –135 dBc/Hz phase noise, at 20 KHz from the carrier, a global jitter value (including the ADC and the generator) of less than 200 fs RMS has been measured. If the clock signal frequency is at fixed rates, it is recommended to narrow-band filter the signal to improve jitter performance.

Note: The clock input buffer's 100Ω termination load is on-chip and mid-point AC coupled (40 pF) to the chip's ground plane, whereas the analog input buffer's 100Ω termination is soldered inside the package cavity and mid-point DC coupled to the package ground plane.Therefore, driving the analog input in single-ended mode does not perturb the chip's ground plane (since the termination mid-point is connected to the package ground plane). However, driving the clock input in single-ended mode does perturb the chip's ground plane (since the termination mid-point is AC coupled to the chip's ground plane). Therefore, it is required to drive the clock input in differential mode for minimum chip ground plane perturbation (a 4 dBm maximum operation is recommended). The typical clock input power is 0 dBm. The minimum operating clock input power is -4 dBm (equivalent to a 250 mV minimum swing amplitude), to avoid SNR performance degradations linked to the clock signal's slew rate.

A single to differential balun with sqrt (2) ratio may be used (featuring a 50Ω input impedance with 100Ω differential termination).

For instance:

4 dBm is equivalent to 1 Vpp into 50Ω and 1.4 Vpp into 100Ω termination (secondary).
0 dBm is equivalent to 0.632 Vpp into 50Ω and 0.632 x sqrt (2) = 0.894 Vpp into 100Ω termination (secondary), ± 0.226V at each clock input.

The recommended clock input's common mode is ground.

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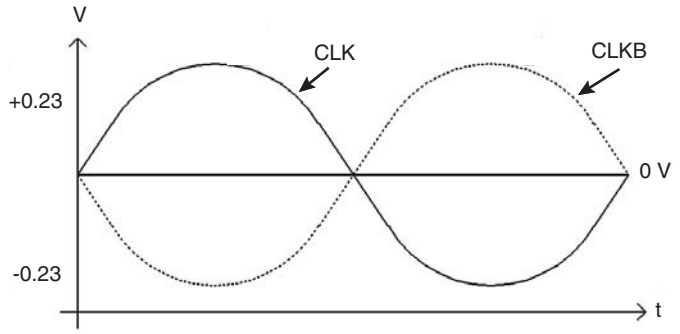
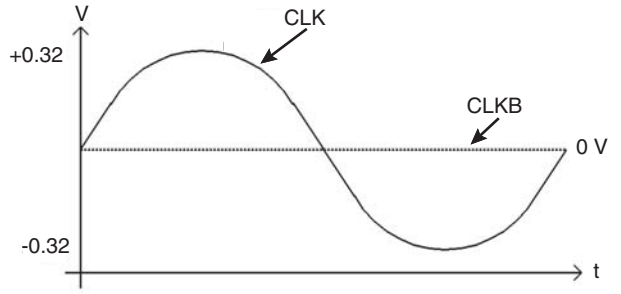
9.4.1 Differential Clock Inputs Voltage Levels (0 dBm Typical)

Figure 9-5. Differential Clock Inputs - Ground Common Mode (Recommended)



9.4.2 Equivalent Single-ended Clock Input Voltage Levels (0 dBm Typical)

Figure 9-6. Single-ended Clock Inputs - Ground Common Mode



9.5 Noise Immunity Information

The circuit's noise immunity performance begins at the design level. Efforts have been made on the design to make the device as insensitive as possible to chip environment perturbations, which may result from the circuit itself or be induced by external circuitry (cascode stage's isolation, internal damping resistors, clamps, internal on-chip decoupling capacitors.)

Furthermore, the fully differential operation from the analog input up to the digital output provides enhanced noise immunity by common mode noise rejection. The common mode noise voltage induced on the differential analog and clock inputs is cancelled out by these balanced differential amplifiers.

Moreover, proper active signal shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs. The analog and clock inputs of the TS83102G0BMGS device have been surrounded by ground pins, which must be directly connected to the external ground plane.

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9.6 Digital Outputs: Termination and Logic Compatibility

Each single-ended output of the TS83102G0BMGS's differential output buffers are internally 50Ω terminated, and feature a 100Ω differential output impedance. The 50Ω resistors are connected to the VPLUSD digital power supply. The TS83102G0BMGS output buffers are designed to drive 50Ω controlled impedance lines properly terminated by a 50Ω resistor. A 10.5 mA bias current flowing alternately into one of the 50Ω resistors when switching, ensures a 0.25V
single-ended voltage drop across the resistor (0.5V differential).

Each single-ended output transmission line length must be kept identical (< 3 mm). Mismatches in the differential line lengths may cause variations in the output differential common mode.

It is recommended to bypass the midpoint of the differential 100Ω termination with a 47 pF capacitor, so as to avoid common mode perturbations in case of a slight mismatch in the differential output line lengths.

See the recommended termination scenarios in Figures 9-7 and. and Figure 9-8 on page 42.

Note: Since the output buffers feature a 100Ω differential output impedance, it is possible to directly drive high the input impedance storing registers without terminating the 50Ω transmission lines. Timewise, this means that the incident wave reflects at the 50Ω transmission line output and travels back to the 50Ω data output buffer. Since the buffer output impedance is 50Ω, no
back reflection occurs and the output swing is doubled.

9.6.0.1 VPLUSD Digital Power Supply Settings

- For differential ECL digital output levels: V_{PLUSD} should be supplied with –0.8V (or connected to ground via a 5Ω resistor to ensure the –0.8 voltage drop).
- For the LVDS digital output logic compatibility: V_{PLUSD} should be tied to 1.45V (±75 mV).

If used with the TS81102G0 DMUX, V_{PLUSD} can be set to ground.

9.6.1 ECL Differential Output Termination Configurations

Figure 9-7. 50Ω Terminated Differential Outputs (Recommended)

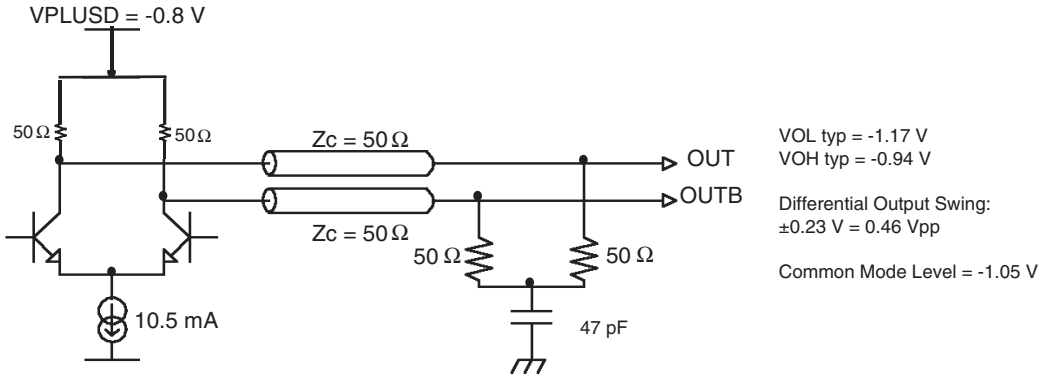

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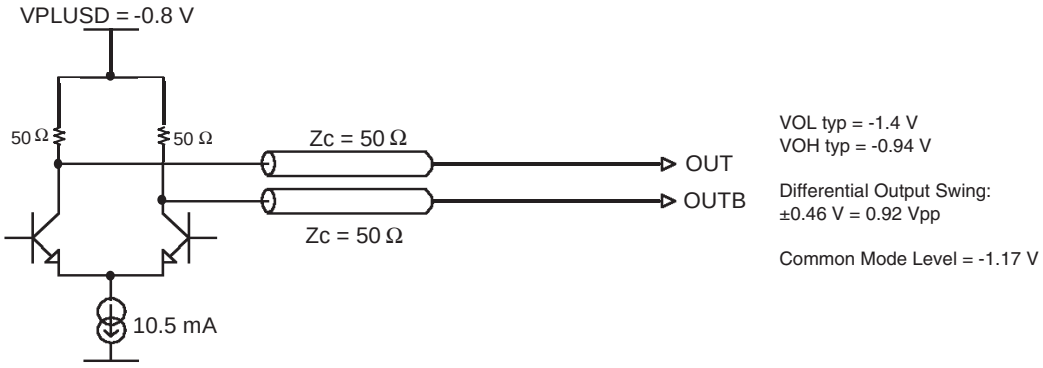
Figure 9-8. Unterminated Differential Outputs (Optional)



9.6.2 LVDS Differential Output Loading Configurations

Figure 9-9. 50Ω Terminated Differential Outputs (Recommended)

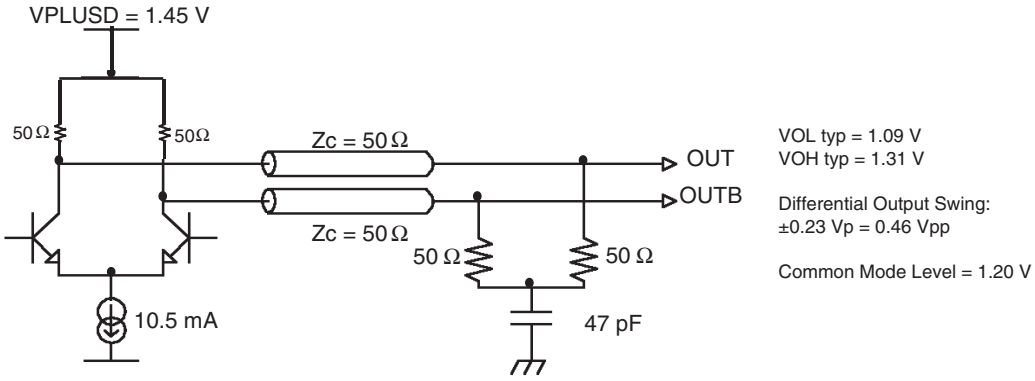
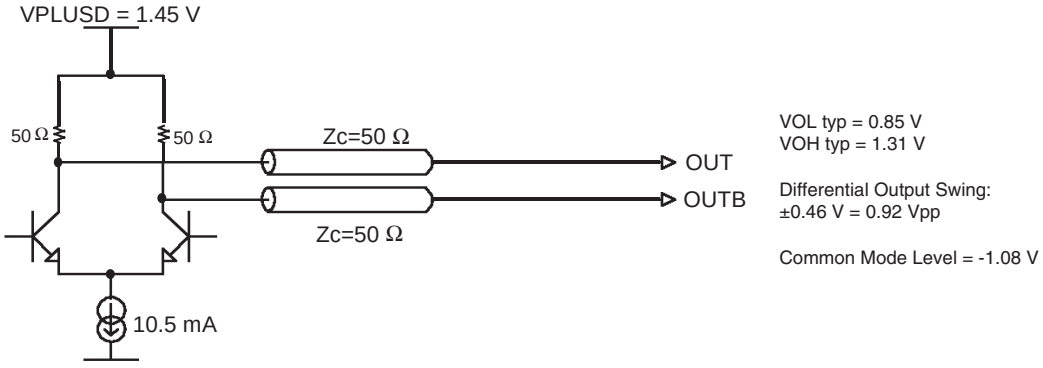


Figure 9-10. Unterminated Differential Outputs (Optional)



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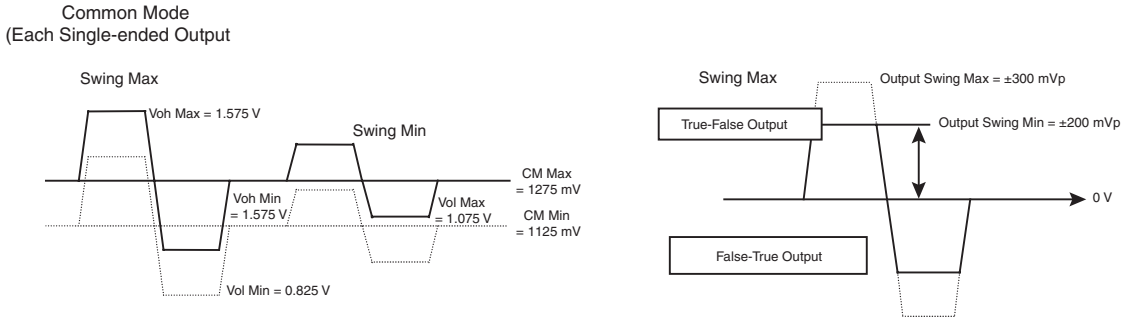
9.6.3 LVDS Logic Compatibility

Figure 9-11. LVDS Format (Refer to the IEEE Standards 1596.3 - 1994): 1125 mV < Common Mode <1275 mV and 250 mV < Output Swing < 400 mV



9.7 Main Functions of the ADC

9.7.1 Out-of-range Bit (OR/ORB)

The out-of-range bit reaches a logical high state when the input exceeds the positive full-scale or falls below the negative full-scale. When the analog input exceeds the positive full-scale, the digital outputs remain at a logical high state with OR/ORB at a logical one. When the analog input falls below the negative full-scale, the digital outputs remain at a logical low state, with OR/ORB at a logical one again.

9.7.2 Bit Error Rate (BER)

The TS83102G0BMGS's internal regeneration latches indecisions (for inputs very close to the latches' threshold). This may produce errors in the logic encoding circuitry, leading to large amplitude output errors.

This is because the latches regenerate the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time D(t): Av = exp (D (t)/t), with t being the positive regeneration time constant feedback.

The TS83102G0BMGS has been designed to reduce the probability of such errors occuring to 10-12 (measured for the converter at 2 Gsps). A standard technique for reducing the amplitude of such errors down to ±1 LSB consists in setting the digital output data to gray code format. However, the TS83102G0BMGS has been designed to feature a Bit Error Rate of 10-12 with a binary output format.

9.7.3 Gray or Binary Output Data Format Selection

To reduce the amplitude of such errors when they occur, it is possible to choose between the binary or gray output data format by storing gray output codes.

Digital data format selection:

- BINARY output format if B/GB is floating or GND
- GRAY output format if B/GB is connected to V_{EE}

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9.7.4 Pattern Generator Function

The pattern generator function (enabled by connecting pin A9 PGEB to V_{EE} = –5V) allows you to rapidly check the ADC's operation thanks to a checker board pattern delivered internally to the ADC. Each of the ADC's output bits should toggle from 0 to 1
successively, giving sequences such as 0101010101 and 1010101010 every 2 cycles.

The out of range bit also toggles when the pattern generator is active. Even bits as well as the out of range bit are low on low to high transition of the data ready signal.

9.7.5 DECB/DIODE: Junction Temperature Monitoring and Output Decimation Enable

The DECB/DIODE pin is provided to enable the decimation function and monitor the die junction temperature.

When connected to V_{EE} = –5V, the ADC runs in "decimation by 32" mode (1 out of 32 data is output from the ADC, thus reducing the data rate by 32).

When the DECB/DIODE pin is left floating, then the ADC is said to be in a "normal" mode of operation (the output data is not decimated) and can be used for die junction temperature monitoring only.

If you do not intend to use the die junction temperature monitoring function, the DECB/DIODE pin (A10) has to be left either floating or connected to ground.

The decimation function can be used to debug the ADC at initial stages. This function enables you to reduce the ADC output rate by 32, thus reducing the time of the ADC's debug phase at the maximum speed rate, and is compatible with industrial testing environments.

When this function is active, the ADC outputs only 1 out of 32 bits of data, resulting in a data rate 32 times slower than the clock rate.

Note: The ADC decimation test mode is different from the pattern generator function, which is used to check the ADC's outputs.

9.7.6 External Configuration Description

Because of the use of one internal diode-mounted transistor (used for junction temperature monitoring), you have to implement external head-to-tail protection diodes so as to avoid potential reverse current flows, which can damage the internal diode component.

Two external configurations are possible:

- Configuration 1: allows both junction temperature monitoring and output data decimation
- Configuration 2: allows junction temperature monitoring only

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9.7.6.1 Configuration 1

This external configuration allows you to apply the requested levels to activate output data decimation (V_{EE} = –5V) and at the same time monitor the junction temperature diode (this explains why 7 protection diodes are needed in the other direction, as shown in Figure 9-12).

Figure 9-12. Recommended Diode Pin Implementation Allowing for Both Die Junction Temperature Monitoring Function and Decimation Mode

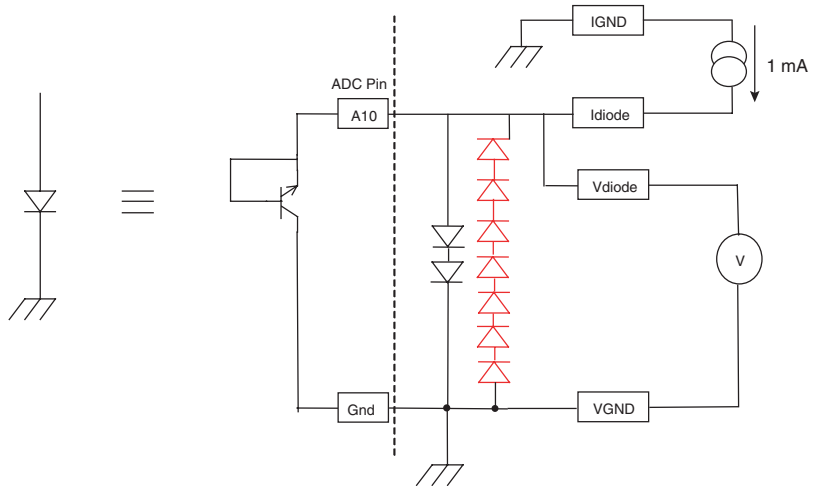
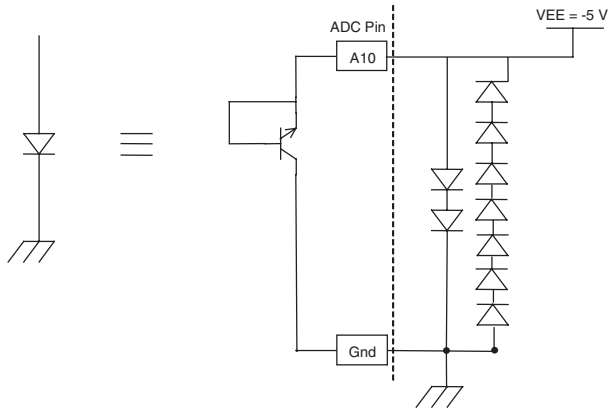


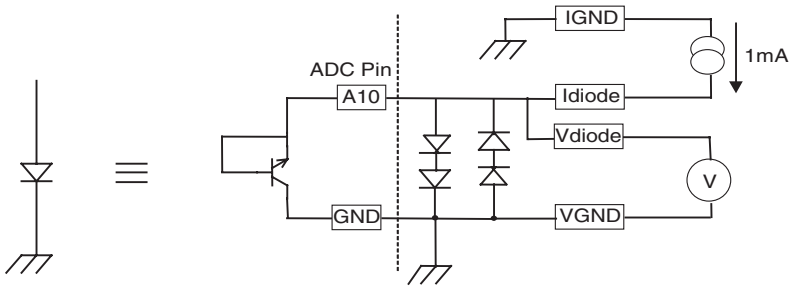
Figure 9-13. Diode Pin Implementation for Decimation Activation



9.7.6.2 Configuration 2:

Note: In the preliminary specification, e2v recommends the use of 2 x 3 head-to-tail protection diodes. The final updated configuration is described in Figure 9-14.

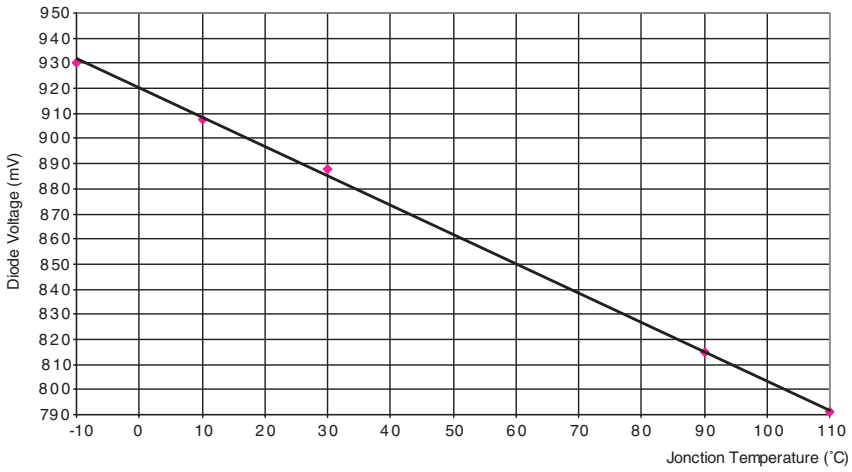
Figure 9-14. Diode Pin Implementation of Die Junction Temperature Monitoring Function Only



9.7.7 Junction Temperature Diode Transfer Function

The forward voltage drop (V_{DIODE}), across the diode component, versus the junction temperature (including the chip's parasitic resistance) is given in the following graph (I_{DIODE} = 1 mA).

Figure 9-15. Junction Temperature vs. Diode Voltage for I = 1 mA



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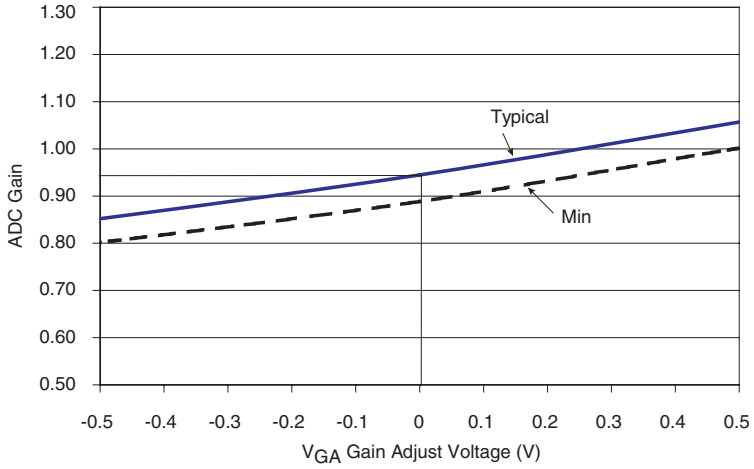
9.7.8 ADC Gain Control

The ADC gain is adjustable by using pin R9 of the CI-CGA package. The gain adjust transfer function is shown Figure 9-16.

Figure 9-16. Gain Adjust Transfer Function



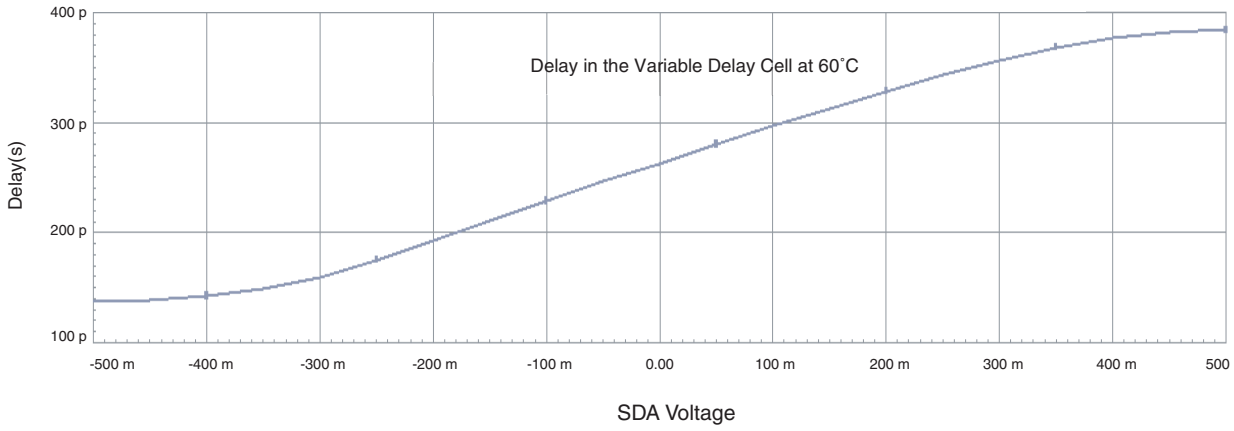
9.7.9 Sampling Delay Adjust

The sampling delay adjust (SDA pin) enables you to fine-tune the sampling ADC aperture delay TAD around its nominal value (160 ps). This functionality is enabled with the SDAEN signal, which is active when tied to V_{EE} and inactive when tied to GND.

This feature is particularly interesting for interleaving ADCs to increase the sampling rate.

The variation of the delay around its nominal value as a function of the SDA voltage is shown in Figure 9-17 (simulation result).

Figure 9-17. Typical Tuning Range (±120 ps for Applied Control Voltage Varying Between –0.5V and 0.5V on the SDA Pin)



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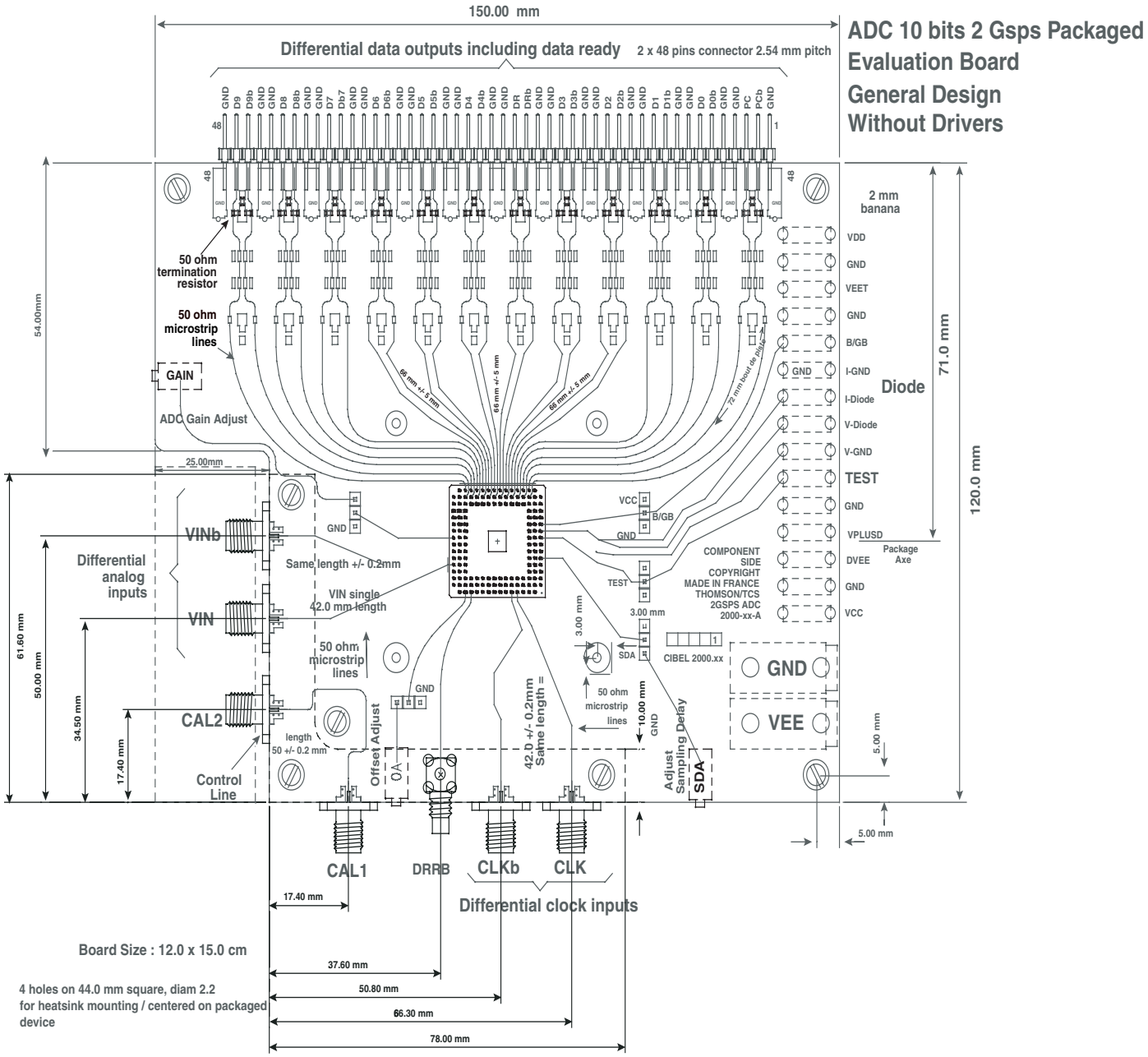
10. TSEV83102G0BGL Evaluation Board (Only CBGA Package)

Figure 10-1. Schematic Board View



Note: For more details, refer to the TSEV83102G0BGL Evaluation Board document

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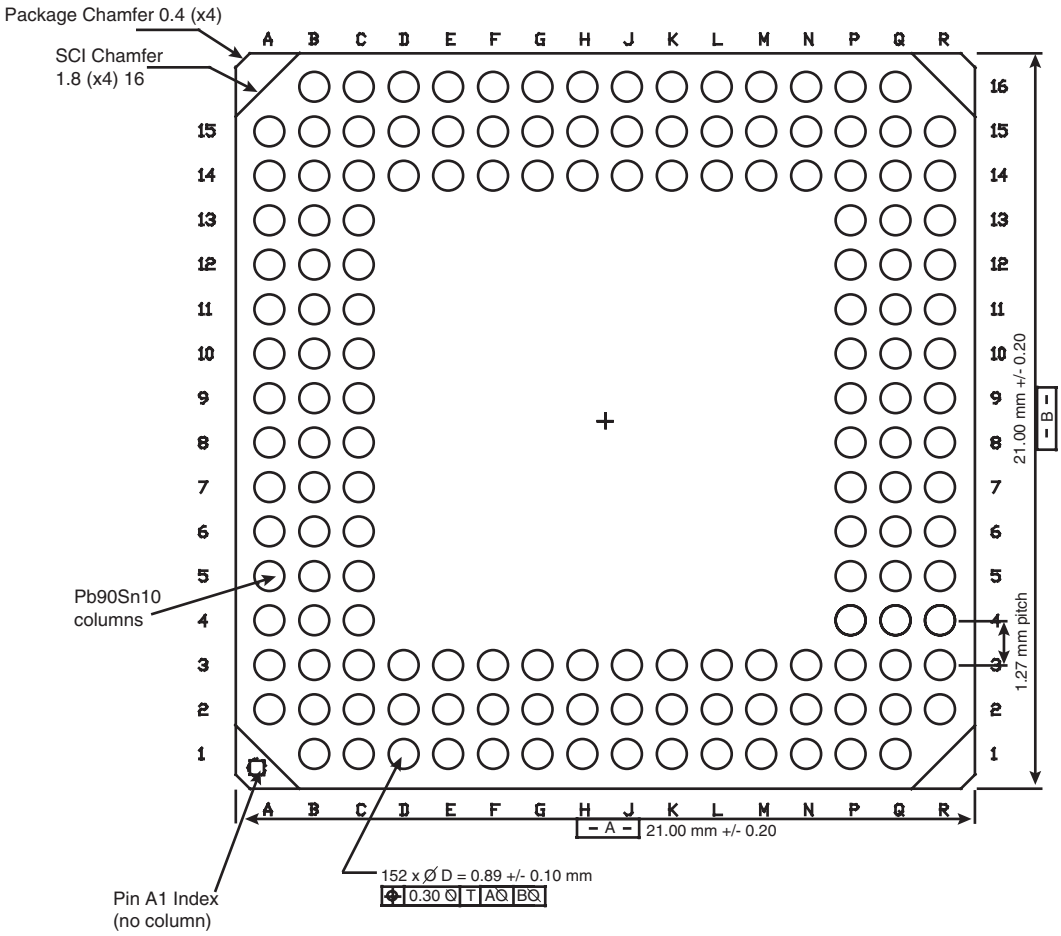
11. Package Description

11.1 Hermetic CI-CGA 152 Outline Dimensions

Figure 11-1. Mechanical Description Bottom View



Note: CuW Heat Spreader on Opposite Side of Package

- Ceramic body size: 21 x 21 mm
- Column pitch: 1.27 mm
- Cofired : Al2O3

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Figure 11-2. Package Top View

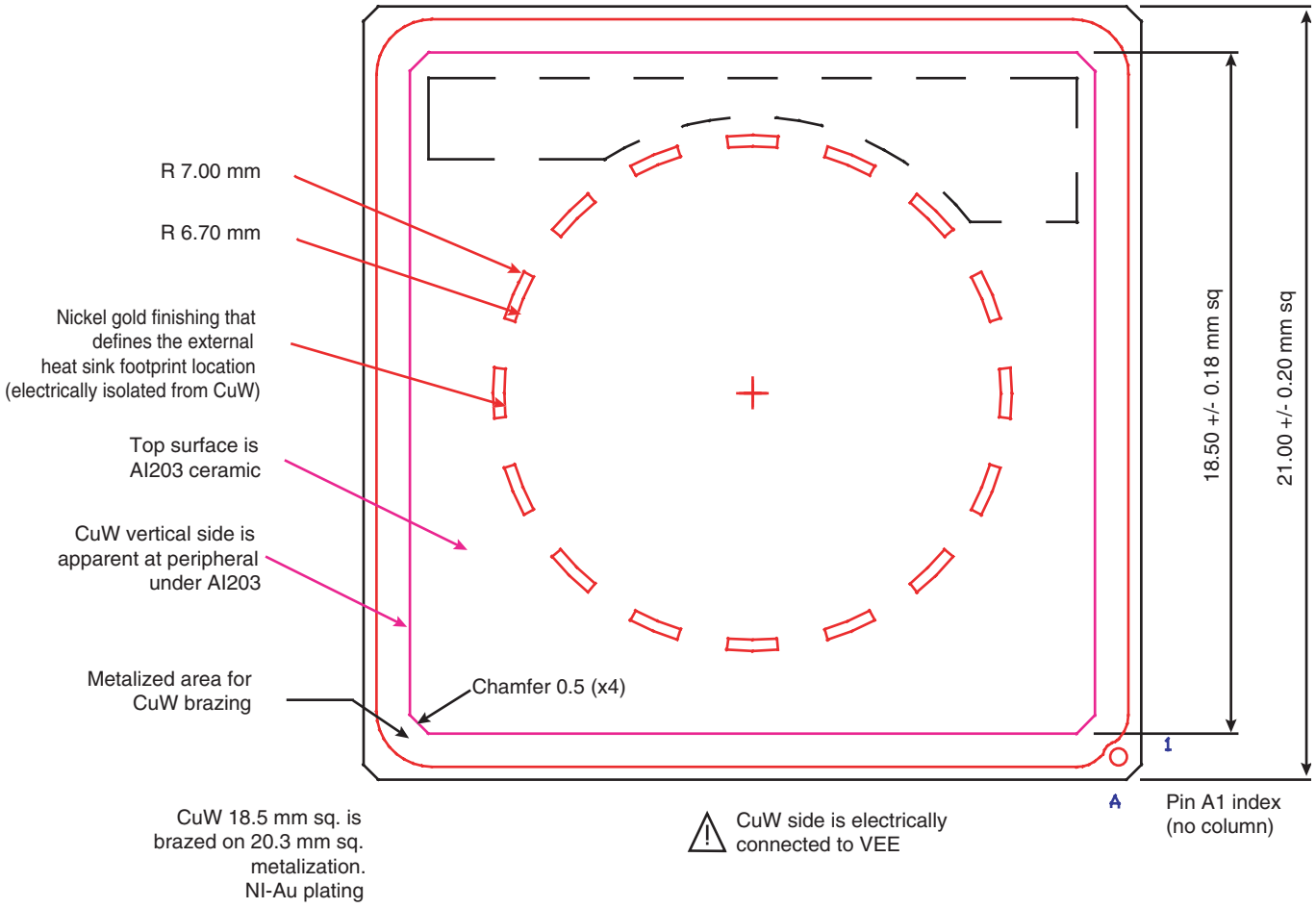

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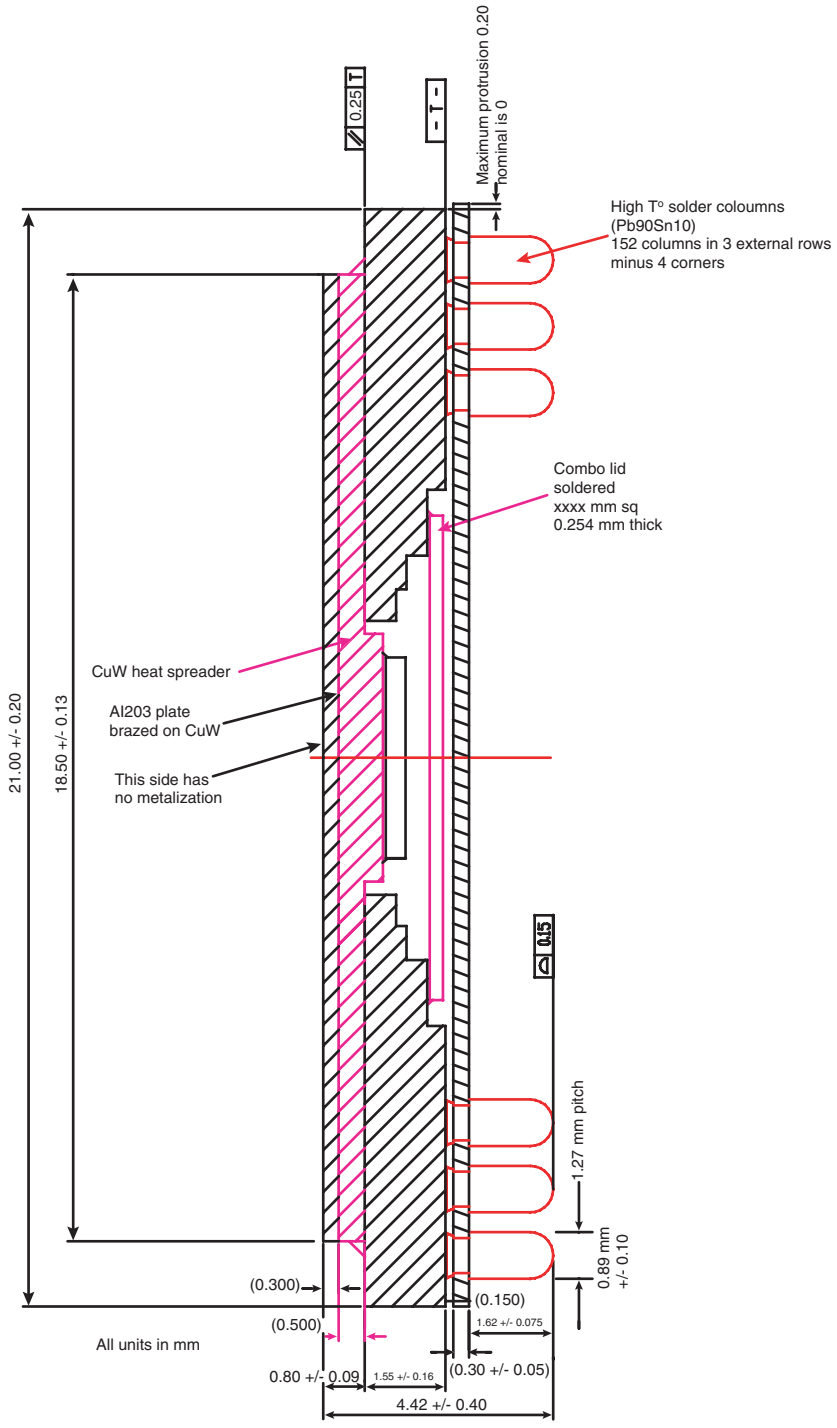
Figure 11-3. Cross Section



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12. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
TS83102G0BMGS	CI-CGA 152	–40°C < T_c; T_J < 125°C	Standard product	Please contact e2v's sales office
TSEV83102G0BGL	CBGA 152	Ambient	Prototype	Evaluation Board (delivered with a heat sink)

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