PC8280/PC8270
Integrated Communication Processors

Datasheet

Features

- **PC603e Microprocessor (Embedded PowerPC® Core) at 166-450 MHz**
- **603e Core with 16K Inst and 16K Data Caches**
- **64-bit 60x Bus, 32-bit Local/PCI Bus**
- **128K ROM, 32K IRAM, 32K DPRAM**
- **Three FCCs Supporting ATM, 10/100 Ethernet or HDLC**
- **256 HDLC Channels, 8 TDMs**
- **4 SCCs, 2 SMCs, SPI, I2C**
- **Memory Controller Built from SDRAM, UPM, GPCM Machines**
- **New Features - USB, RMII, UTOPIA Improvements**
- **Performance**
  - **400 MHz CPU, 250 MHz CPM, 83 MHz Bus**
  - **Less than 2W at Full Performance, 1.5V**
- **Technology**
  - **3.3V I/O, 1.5V Core**
  - **480 TBGA, 37.5 × 37.5 mm, 1.27 mm Ball Pitch**

Description

This document contains detailed information about power considerations, DC/AC electrical characteristics, and AC timing specifications for 130 nm members of the PowerQUICC II™ family of integrated communications processors: the PC8280 and the PC8270 (collectively called 'the PC8280' throughout this document).

Screening/Quality/Packaging

This product is manufactured in full compliance with:

- **Upscreening Based Upon e2v Standards**
- **Military Temperature Range (T_{case} = -55°C, T_J = +125°C)**
- **480-ball Tape Ball Grid Array Package (TBGA 37.5 × 37.5 mm)**

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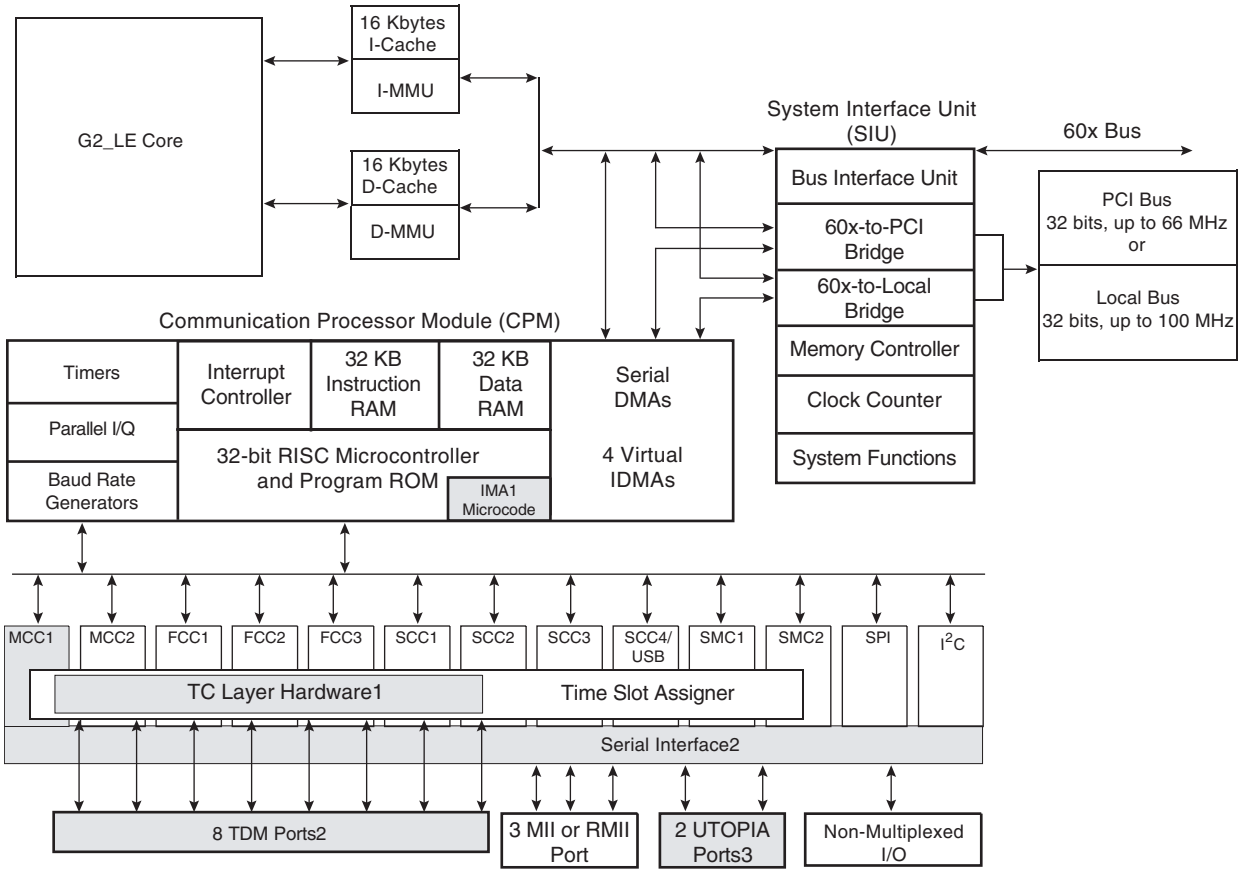
1. Overview

Table 1-1 shows the functionality supported by the PC8280.

Table 1-1. PC8280 PowerQUICC II Functionality

Functionality	Package	PC8270	PC8280
		480 TBGA	480 TBGA
Serial communications controllers (SCCs)		4	4
QUICC multi-channel controller (QMC)		–	–
Fast communication controllers (FCCs)		3	3
I-Cache (Kbyte)		16	16
D-Cache (Kbyte)		16	16
Ethernet (10/100)		3	3
UTOPIA II Ports		0	2
Multi-channel controllers (MCCs)		1	2
PCI bridge		Yes	Yes
Transmission convergence (TC) layer		–	Yes
Inverse multiplexing for ATM (IMA)		–	Yes
Universal serial bus (USB) 2 full/low rate		1	1
Security engine (SEC)		–	–

Figure 1-1. PC8280 Block Diagram



Notes: 1. PC8280 only (not on PC8270).
2. PC8280 has 2 serial interface (SI) blocks and 8 TDM ports. PC8270 has only 1 SI block and 4 TDM ports (TDM2[A–D]).
3. PC8280 only (not on PC8270).

1.1 Features

The major features of the PC8280 are as follows:

- Dual-issue integer (G2_LE) core

  A core version of the EC603e microprocessor

  System core microprocessor supporting frequencies of 166–450 MHz

  Separate 16-Kbyte data and instruction caches:

  – Four-way set associative
  – Physically addressed
  – LRU replacement algorithm

  Architecture-compliant memory management unit (MMU)

  Common on-chip processor (COP) test interface

  High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)

  Supports bus snooping for data cache coherency

Floating-point unit (FPU)

- Separate power supply for internal logic and for I/O
- Separate PLLs for G2_LE core and for the CPM

  G2_LE core and CPM can run at different frequencies for power/performance optimization

  Internal core/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1 ratios

  Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios

- 64-bit data and 32-bit address 60x bus

  Bus supports multiple master designs

  Supports single- and four-beat burst transfers

  64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

  Supports data parity or ECC and address parity

- 32-bit data and 18-bit address local bus

  Single-master bus, supports external slaves

  Eight-beat burst transfers

  32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

- 60x-to-PCI bridge

  Programmable host bridge and agent

  32-bit data bus, 66.67/83.3/100 MHz, 3.3V

  Synchronous and asynchronous 60x and PCI clock modes

  All internal address space available to external PCI host

  DMA for memory block transfers

  PCI-to-60x address remapping

- PCI bridge

  PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz

  On-chip arbitration

  Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming

  PCI host bridge or peripheral capabilities

  Includes 4 DMA channels for the following transfers:

  – PCI-to-60x to 60x-to-PCI
  – 60x-to-PCI to PCI-to-60x
  – PCI-to-60x to PCI-to-60x
  – 60x-to-PCI to 60x-to-PCI–

  Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the PC8280) required by the PCI standard as well as message and doorbell registers

  Supports the I^2O standard

Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)

Support for 66.67/83.33/100 MHz, 3.3V specification

60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port

Uses the local bus signals, removing need for additional pins

- System Interface Unit (SIU)

  Clock synthesizer

  Reset controller

  Real-time clock (RTC) register

  Periodic interrupt timer

  Hardware bus monitor and software watchdog timer

  IEEE® 1149.1 JTAG test access port

- 12-bank memory controller

  Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user- definable peripherals

  Byte write enables and selectable parity generation

  32-bit address decodes with programmable bank size

  Three user-programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine

  Byte selects for 64-bus width (60x) and byte selects for 32-bus width (local)

  Dedicated interface logic for SDRAM

- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications Processor Module (CPM)

  Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols

  Interfaces to G2_LE core through an on-chip 32-Kbyte dual-port data RAM, an on-chip 32-Kbyte dual-port instruction RAM and DMA controller

  Serial DMA channels for receive and transmit on all serial channels

  Parallel I/O registers with open-drain and interrupt capability

  Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers

  Three fast communications controllers supporting the following protocols:

  – 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)
  – ATM: Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64 K external connections (no ATM support for the PC8270)
  – Transparent

- HDLC: Up to T3 rates (clear channel)
- FCC2 can also be connected to the TC layer

Two multichannel controllers (MCCs) (one MCC on the PC8270)

- Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
- Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC

Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:

- Ethernet/IEEE 802.3 CDMA/CS
- HDLC/SDLC and HDLC bus
- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Binary synchronous (BISYNC) communications
- Transparent

Universal serial bus (USB) controller

- Supports USB 2.0 full/low rate compatible
- USB host mode
- Supports control, bulk, interrupt, and isochronous data transfers
- CRC16 generation and checking
- NRZI encoding/decoding with bit stuffing
- Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
- Flexible data buffers with multiple buffers per frame
- Supports local loopback mode for diagnostics (12 Mbps only)
- Supports USB slave mode
- Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
- CRC16 generation and checking
- CRC5 checking
- NRZI encoding/decoding with bit stuffing
- 12- or 1.5-Mbps data rate
- Flexible data buffers with multiple buffers per frame
- Automatic retransmission upon transmit error

Two serial management controllers (SMCs), identical to those of the MPC860

- Provide management for BRI devices as general circuit interface (GCI) controllers in timedivision-multiplexed (TDM) channels
- Transparent
- UART (low-speed operation)

One serial peripheral interface identical to the MPC860 SPI

One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)

– Microwire compatible

– Multiple-master, single-master, and slave modes

Up to eight TDM interfaces (four on the PC8270)

– Supports two groups of four TDM channels for a total of eight TDMs

– 2,048 bytes of SI RAM

– Bit or byte resolution

– Independent transmit and receive routing, frame synchronization

– Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale™ interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces

Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels

Four independent 16-bit timers that can be interconnected as two 32-bit timers

- Inverse multiplexing for ATM capabilities (IMA). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer

2. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7447A in compliance with e2v standard screening.

2.1 Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

2.2 Operating Conditions

Table 2-1 shows the maximum electrical ratings.

Table 2-1. Absolute Maximum Ratings(1)

Rating	Symbol	Value	Unit
Core supply voltage(2)	V_{DD}	-0.3 to +2.25	V
PLL supply voltage(2)	VCCSYN	-0.3 to +2.25	V
I/O supply voltage(3)	VDDH	-0.3 to +4	V
Input voltage(4)	V_{IN}	GND(-0.3) to +3.6	V
Storage temperature range	T_{STG}	-65 to +150	°C

Notes: 1. Absolute maximum ratings are stress ratings only; functional operation (see Table 2-2 on page 8) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2. **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4V during power-on reset for no more than 100 ms.
3. **Caution:** VDDH can exceed VDD/VCCSYN by 3.3V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5V during normal operation.
4. **Caution:** V_{IN} must not exceed VDDH by more than 2.5V at any time, including during power-on reset.

Table 2-2 lists recommended operational voltage conditions.

Table 2-2. Recommended Operaging Conditions(1)

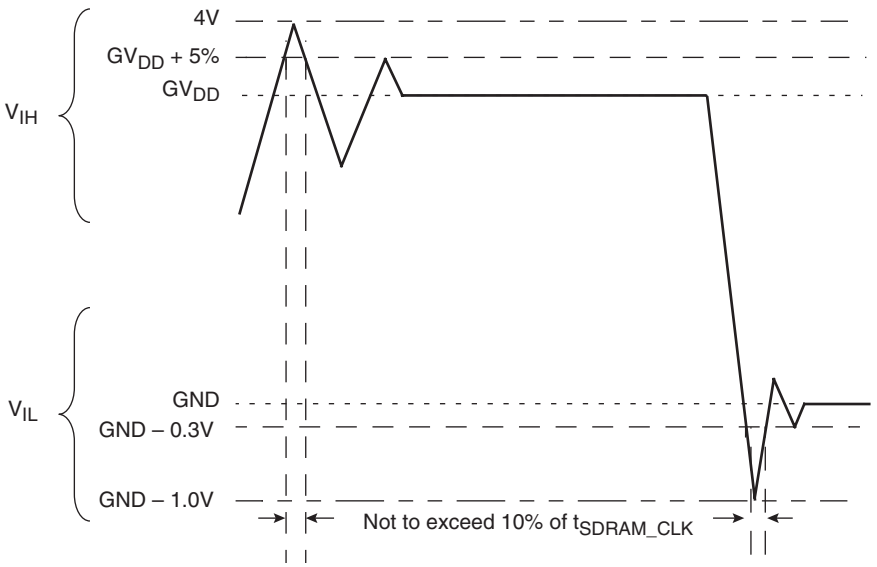
Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.45 – 1.60	V
PLL supply voltage	VCCSYN	1.45 – 1.60	V
I/O supply voltage	VDDH	3.135 – 3.4	V
Input voltage	V_{IN}	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T_J	125	°C
Ambient temperature	T_{case}	-55	°C

Notes: 1. Caution: These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an a propriate logic voltage level (either GND or V_{CC}).

Figure 2-1 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the PC8280. Note that in PCI mode the I/O interface is different.

Figure 2-1. Overshoot/Undershoot Voltage



3. DC Electrical Characteristics

Table 3-1 shows DC electrical characteristics.

Table 3-1. DC Electrical Characteristics[1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage: all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2]	V_{IH}	2	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKin input high voltage	V_{IHC}	2.4	3.465	V
CLKin input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH[3]	I_{IN}	–	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[3]	I_{OZ}	–	10	µA
Signal low input current, V_{IL} = 0.8V[4]	I_L	–	1	µA
Signal high input current, V_{IH} = 2V	I_H	–	1	µA
Output high voltage, I_{OH} = -2 mA except UTOPIA mode, and open drain pins In UTOPIA mode (UTOPIA pins only): I_{OH} = -8 mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	–	
In UTOPIA mode (UTOPIA pins only): I_{OL}= 8 mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	–	0.5	

Table 3-1. DC Electrical Characteristics[1] (Continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 6 mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/EXT_DBG3/IRQ5/CINT DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5/CINT CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF	V_{OL}	–	0.4	

Table 3-1. DC Electrical Characteristics[1] (Continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3 mA $\overline{CS}$[0-9] $\overline{CS}$(10)/$\overline{BCTL1}$ $\overline{CS}$(11)/AP(0) BADDR[27–28] ALE $\overline{BCTL0}$ $\overline{PWE}$[0–7]/$\overline{PSDDQM}$[0–7]/$\overline{PBS}$[0–7] PSDA10/PGPL0 $\overline{PSDWE}$/PGPL1 $\overline{POE}$/$\overline{PSDRAS}$/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 $\overline{LWE}$[0–3]$\overline{LSDDQM}$[0–3]/$\overline{LBS}$[0–3]/PCI_CFG[0–3] LSDA10/LGPL0/PCI_MODCKH0 LSDWE/LGPL1/PCI_MODCKH1 $\overline{LOE}$/$\overline{LSDRAS}$/LGPL2/PCI_MODCKH2 LSDCAS/LGPL3/PCI_MODCKH3 LGTA/LUPMWAIT/LGPL4/$\overline{LPBS}$ LSDAMUX/LGPL5/PCI_MODCK $\overline{LWR}$ MODCK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2]	V_{OL}	–	0.4	V
I_{OL} = 3.2 mA L_A14/PAR L_A15/$\overline{FRAME}$/$\overline{SMI}$ L_A16/$\overline{TRDY}$ L_A17/$\overline{IRDY}$/CKSTP_OUT L_A18/$\overline{STOP}$ L_A19/$\overline{DEVSEL}$ L_A20/IDSEL L_A21/$\overline{PERR}$ L_A22/$\overline{SERR}$ L_A23/$\overline{REQ0}$ L_A24/$\overline{REQ1}$/$\overline{HSEJSW}$ L_A25/$\overline{GNT0}$ L_A26/$\overline{GNT1}$/$\overline{HSLED}$ L_A27/$\overline{GNT2}$/$\overline{HSENUM}$ L_A28/$\overline{RST}$/$\overline{CORE\_SRESET}$ L_A29/$\overline{INTA}$ L_A30/$\overline{REQ2}$ L_A31 LCL_D[0-31]/AD[0-31] LCL_DP[0-3]/C/$\overline{BE}$[0-3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO QREQ	V_{OL}	–	0.4	V

Notes:
1. The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.
2. TCK, $\overline{TRST}$ and $\overline{PORESET}$ have min V_{IH} = 2.5V.
3. The leakage current is measured for nominal VDDH,VCCSYN, and VDD.
4. V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.

4. Thermal Characteristics

Table 4-1 describes thermal characteristics for both the packages. For the discussions Section 4.1 and Section 4.5, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

Table 4-1. Thermal Characteristics

Characteristic	Symbol	Value	Unit	Air Flow
		480 TBGA		
Junction to ambient, single-layer board[1]	$R_{\theta JA}$	16	°C/W	Natural convection
		11		1 m/s
Junction to ambient, four-layer board	$R_{\theta JA}$	12	°C/W	Natural convection
		9		1 m/s
Junction to board[2]	$R_{\theta JB}$	6	°C/W	–
Junction to case[3]	$R_{\theta JC}$	2	°C/W	–
Junction-to-package top[4]	Ψ_{JT}	2	°C/W	–

Notes:
1. Assumes no thermal vias.
2. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$T_J = T_{amb} + (R_{\theta JA} \times P_D)$

where:

T_{amb} = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_{amb}$) are possible.

4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$T_J = T_B + (R_{\theta JB} \times P_D)$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature (°C)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\psi_{JT} \times P_D)$

where:

ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using by-pass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1 µF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47 µF for VDD and 2 capacitors of 47 µF for VDDH are also recommnded. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the PC8280 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

5. Power Dissipation

Table 5-1 on page 15 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value.

Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, refer to section "Clock Configuration Modes" on page 25.

Table 5-1. Estimated Power Dissipation for Various Configuration[1]

Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	P_{INT}(W)[2][3] Vddl 1.5 Volts	
					Nominal	Maximum
66.67	2.5	166	3.5	233	0.95	1
66.67	2.5	166	4	266	1	1.05
66.67	3	200	4	266	1.05	1.1
66.67	3.5	233	4.5	300	1.05	1.15
83.33	3	250	4	333	1.25	1.35
83.33	3	250	4.5	375	1.3	1.4
83.33	3.5	292	5	417	1.45	1.55
100	3	300	4	400	1.5	1.6
100	3	300	4.5	450	1.55	1.65

Notes: 1. Test temperature = 105°C

2. $P_{INT} = I_{DD} \times V_{DD}$ Watts

3. Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.45W (nominal), 0.5W (maximum)
83.3 MHz = 0.5W (nominal), 0.6W (maximum)
100 MHz = 0.6 W (nominal), 0.7W (maximum)

6. AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10 pF load for MIN delay. Typical output buffer impedances are shown in Table 6-1.

Table 6-1. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27[2]
Local bus	45
Memory controller	45 or 27[2]
Parallel I/O	45
PCI	27

Notes: 1. These are typical values at 65°C. Impedance may vary by ±25% with process and temperature.

2. On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45Ω On all other revisions, impedance value is selected through the SIUMCR[20,21]. Refer to the PC8280 PowerQUICC II Family Reference Manual.

6.1 CPM AC Characteristics

Table 6-2 lists CPM output characteristics.

Table 6-2. AC Characteristics for CPM Outputs[1]

Spec Number			Value (ns)					
			Maximum Delay			Minimum Delay		
Max	Min	Characteristic	66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp36a	sp37a	FCC outputs, internal clock (NMSI)	6	5.5	5.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs, external clock (NMSI)	8	8	8	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs, internal clock (NMSI)	10	10	10	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs, external clock (NMSI)	8	8	8	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	0.5	0.5	0.5

Note: 1. Output specifications are measured from the 50% level of the rising edge of CLKin to the 50% level of the signal. Timings are measured at the pin.

Table 6-3 lists CPM input characteristics.

Note: Rise/Fall Time on CPM Input Pins.
It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{CC}; fall time refers to transitions from 90% to 10% of V_{CC}.

Table 6-3. AC Characteristics for CPM Inputs[1]

Spec Number			Value (ns)					
			Setup			Hold		
Setup	Hold	Characteristic	66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs, internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	inputs, external clock (NMSI)	2.5	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2Cclock inputs, internal (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2Cclock inputs, external (NMSI)	4	4	4	2	2	2
sp20	sp21	TDM inputs/SI	5	5	5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	0.5	0.5	0.5

Note: 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKin. Timings are measured at the pin.

Note: Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 6-1 shows the FCC internal clock.

Figure 6-1. FCC Internal Clock Diagram

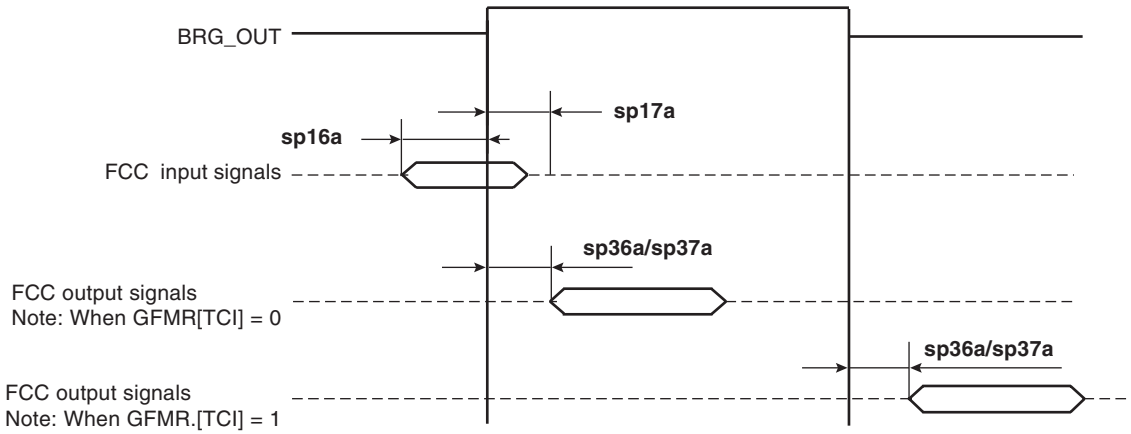


Figure 6-2 shows the FCC external clock.

Figure 6-2. FCC External Clock Diagram

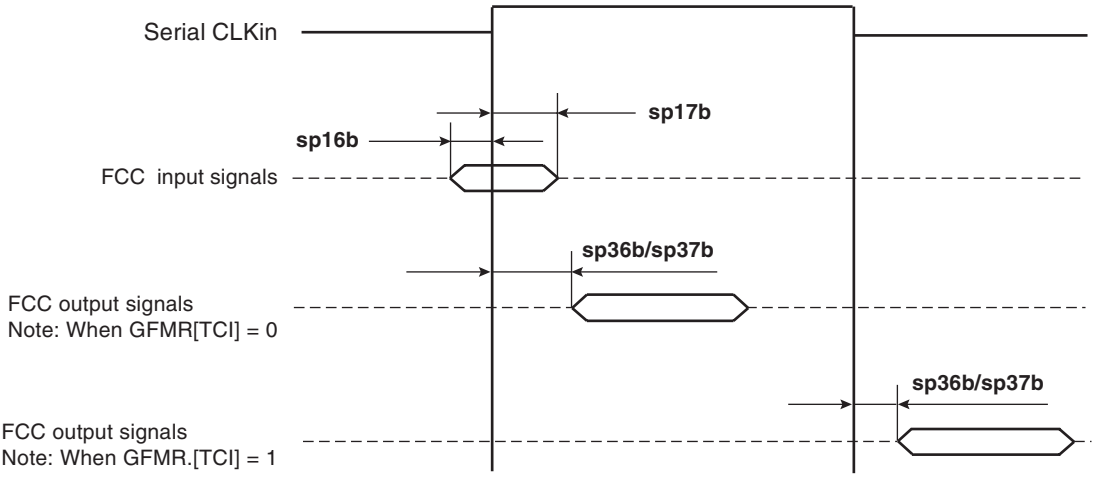
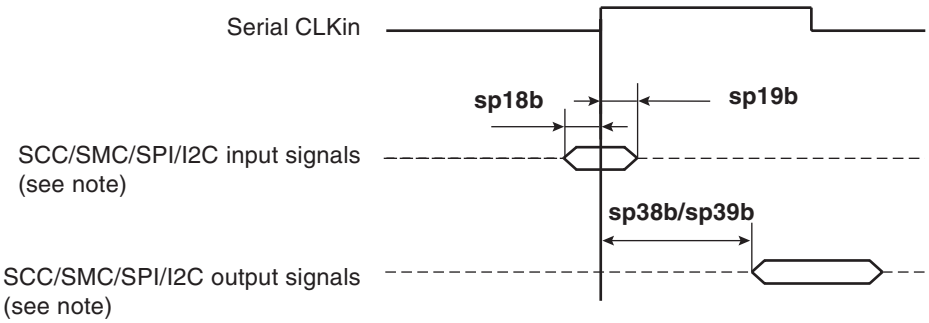


Figure 6-3 shows the SCC/SMC/SPI/I^{2}C external clock.

Figure 6-3. SCC/SMC/SPI/I^{2}C External Clock Diagram

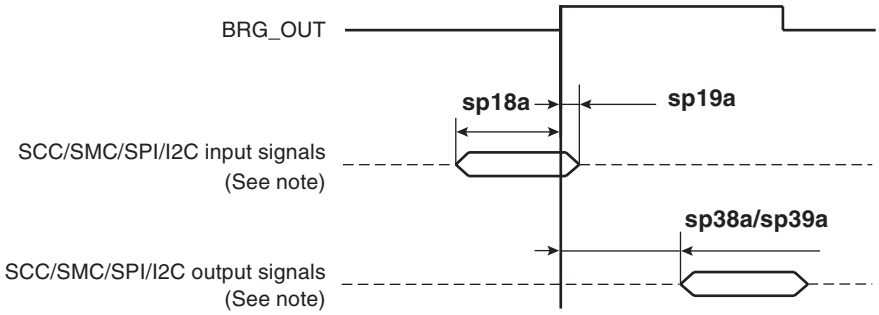


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6-4 shows the SCC/SMC/SPI/I^{2}C internal clock.

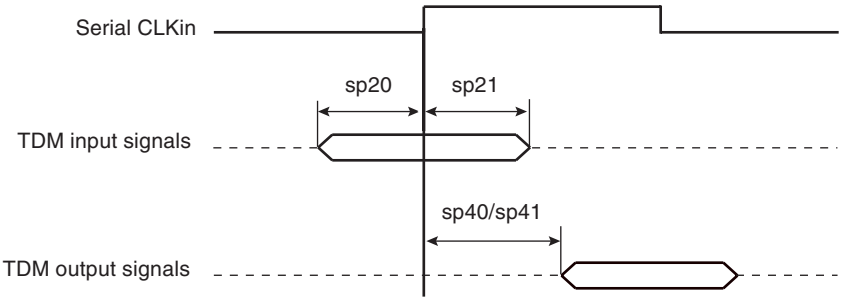
Figure 6-4. SCC/SMC/SPI/I^{2}C Internal Clock Diagram



Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6-5. TDM Signal Diagram

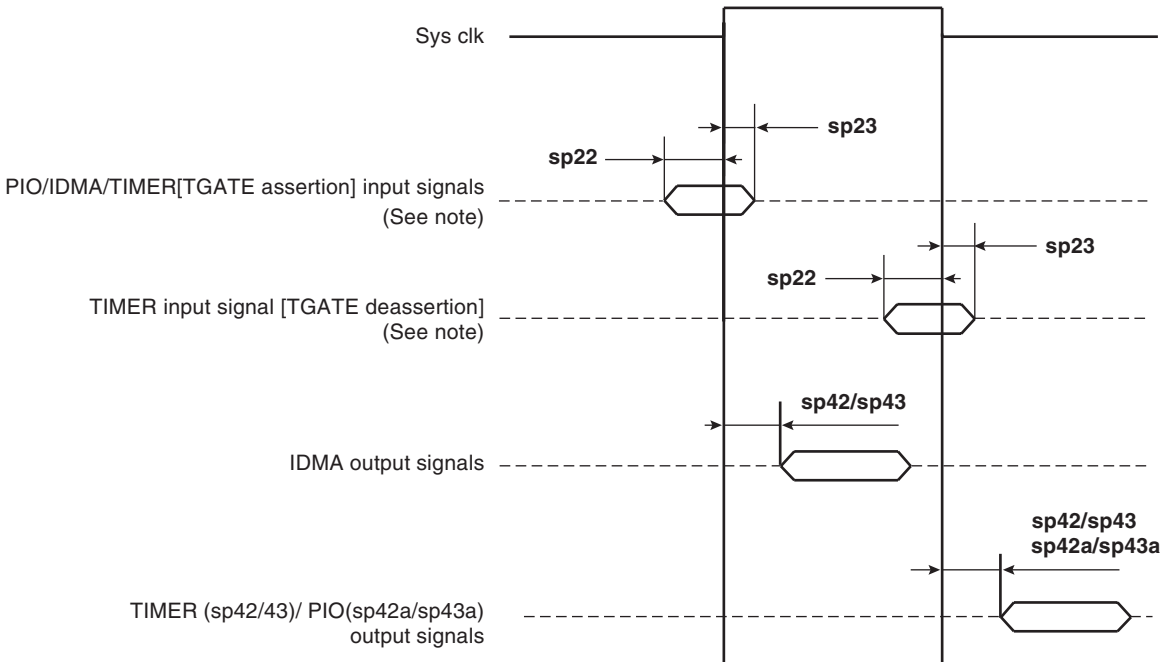


Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6-6 shows PIO and timer signals.

Figure 6-6. PIO and Timer Signal Diagram



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

6.2 SIU AC Characteristics

1. **CLKin Jitter and Duty Cycle**
   The CLKIN input to the PC8280 should not exceed ±150 psec of jitter (peak-to-peak). This represents total input jitter: the combination of short term (cycle-to-cycle) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60. The rise/file time of CLKIN should adhere to the typical SDRAM device AC clock requirement of 1 V/ns to meet SDRAM AC specs.
2. **Spread Spectrum Clocking**
   Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.
3. **PCI AC Timing**
   The PC8280 meets the timing requirements of PCI Specification Revision 2.2. Refer to Section 7.2 ”PCI Host Mode” on page 28 and Section 7.3 ”PCI Agent Mode” on page 35 and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

Table 6-4 lists SIU input characteristics.

Table 6-4. AC Characteristics for SIU Inputs[1]

Spec Number			Value (ns)					
			Setup			Hold		
Setup	Hold	Characteristic	66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11	sp10	$\overline{AACK}/\overline{TA}/\overline{TS}/\overline{DBG}/\overline{BG}/\overline{BR}/\overline{ARTRY}/\overline{TEA}$	6	5	3.5	0.5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	7	5	3.5	0.5	0.5	0.5
sp13a	sp10	Pipeline mode – Data bus in PARITY mode[2] ECC mode	5	4	2.5	0.5	0.5	0.5
sp14	sp10	DP pins	7	5	3.5	0.5	0.5	0.5
sp14a	sp10	Pipeline mode – DP pins[2]	–	4	2.5	–	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	0.5	0.5	0.5

Notes: 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKin. Timings are measured at the pin.
2. Not supported at 66 MHz

Table 6-5 lists SIU output characteristics.

Table 6-5. AC Characteristics for SIU Outputs[1]

Spec Number			Value (ns)					
			Maximum Delay			Minimum Delay		
Max	Min	Characteristic	66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	5.5	1	1	1
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	1	1	1
sp33a	sp30	Data bus[2]	6.5	6.5	5.5	0.7	0.7	0.7
sp33b	sp30	DP	6	5.5	5.5	1	1	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	1	1	1
sp35a	sp30	AP	7	7	7	1	1	1

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKin to the 50% level of the signal. Timings are measured at the pin.
2. To achieve 1 ns of hold time at 66, 83, or 100 MHz, a minimum loading of 20 pF is required.

Note: Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing.

Figure 6-7 shows the interaction of several bus signals.

Figure 6-7. Bus Signals

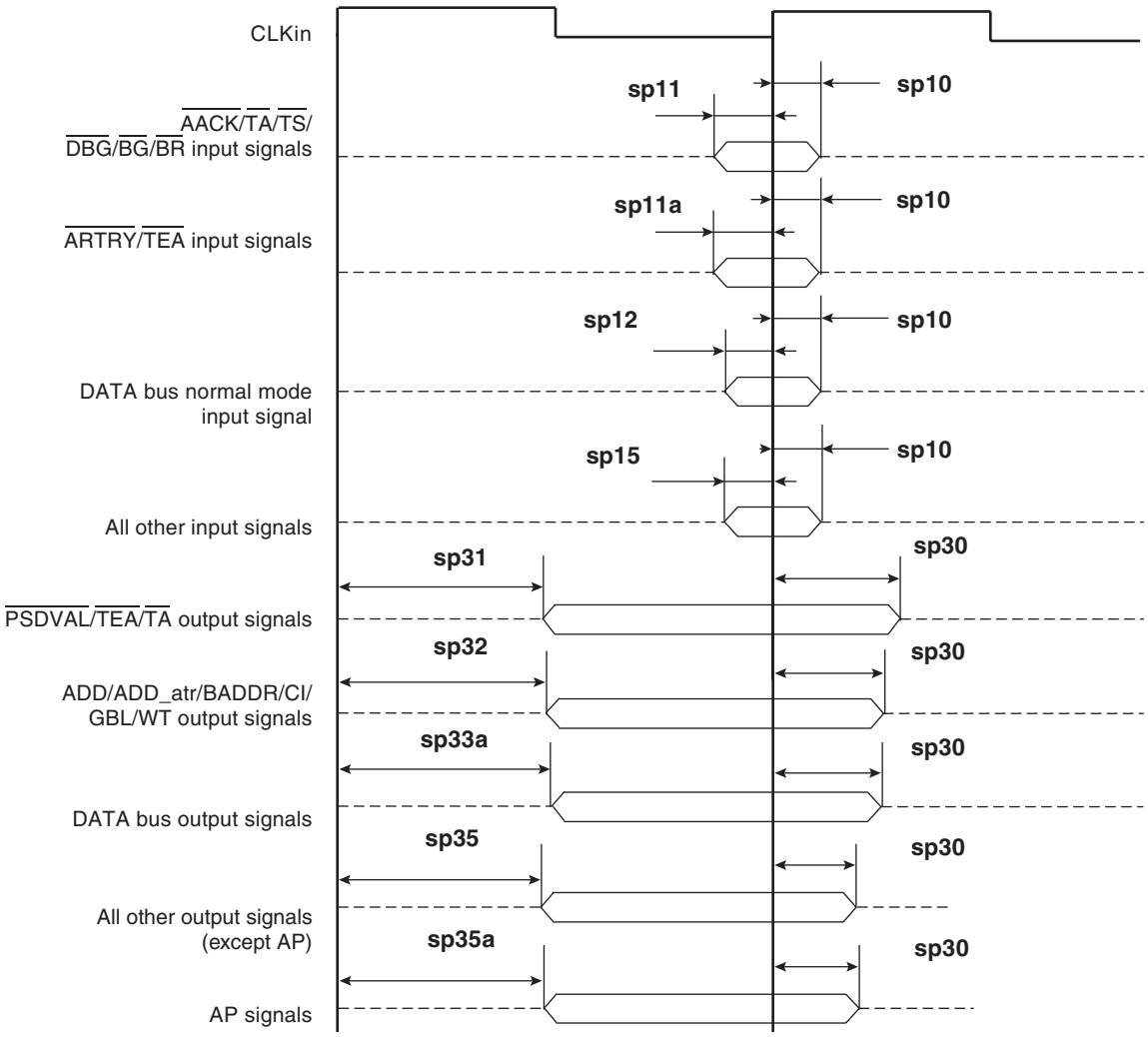


Figure 6-8 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

Figure 6-8. Parity Mode Diagram

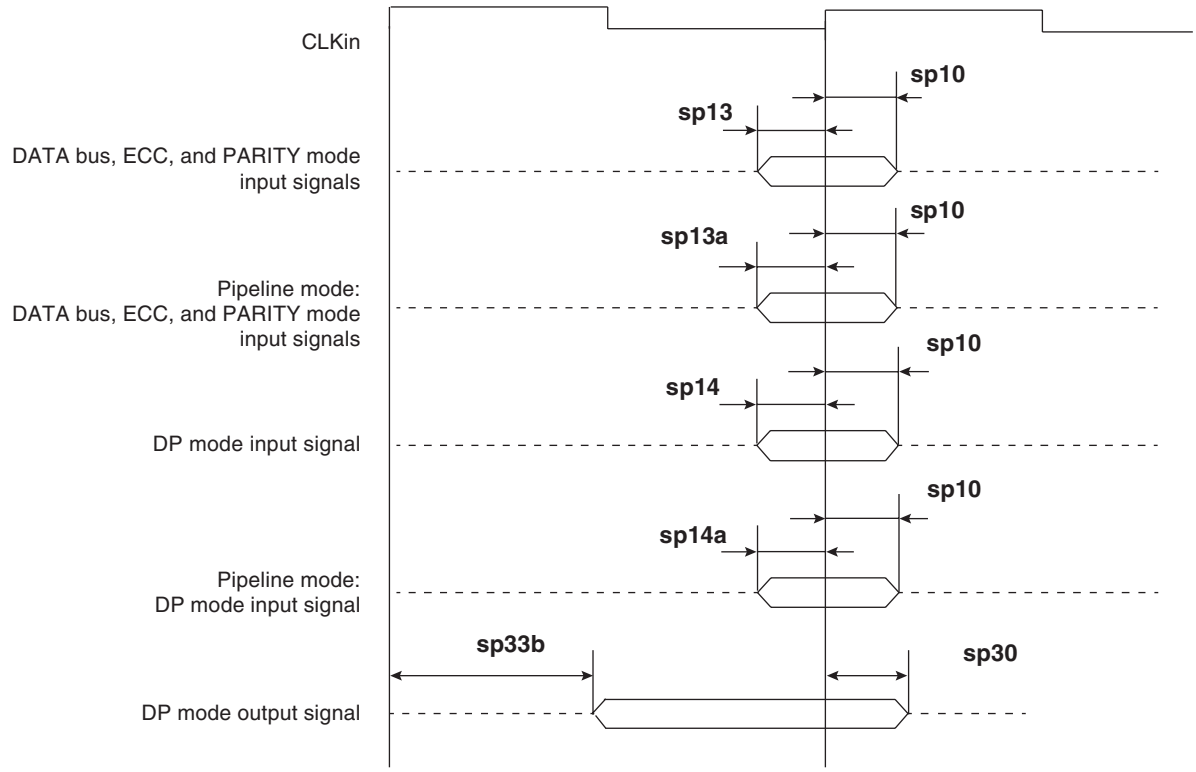
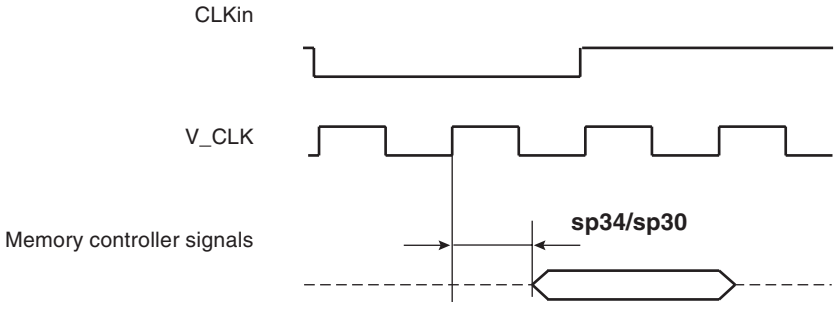


Figure 6-9 shows signal behavior in MEMC mode.

Figure 6-9. MEMC Mode Diagram



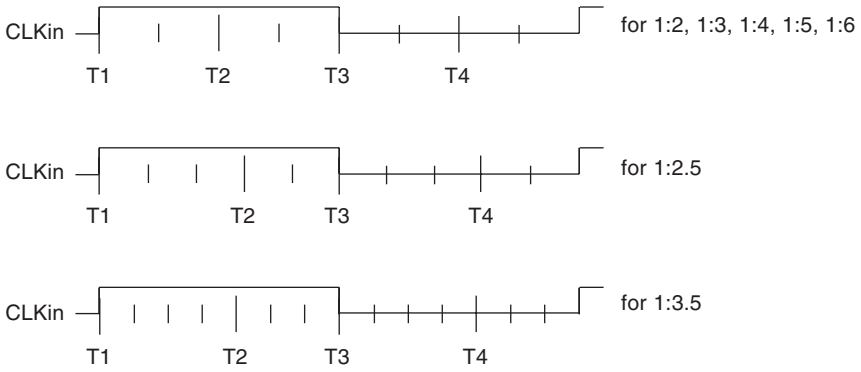
Note: Generally, all PC8280 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 6-6 on page 24.

Table 6-6. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 6-10 is a representation of the information in Table 6-6 on page 24.

Figure 6-10. Internal Tick Spacing for Memory Controller Signals



Note: The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

6.3 JTAG Timings

Table 6-7 lists the JTAG timings.

Table 6-7. JTAG Timings[1]

Symbol	Parameter	Min	Max	Unit
f_{JTG}	JTAG external clock frequency of operation	0	33.3	MHz
t_{JTG}	JTAG external clock cycle time	30	–	ns
t_{JTKHKL}	JTAG external clock pulse width measured at 1.4V	15	–	ns
t_{JTGR} and t_{JTGF}[6]	JTAG external clock rise and fall times	0	5	ns
t_{TRST}[3][6]	TRST assert time	25	–	ns
	Input setup times:			
t_{JTDVKH}[4][7]	Boundary-scan data	4	–	ns
t_{JTIVKH}[4][7]	TMS, TDI	4	–	ns
	Input hold times:			
t_{JTDXKH}[4][7]	Boundary-scan data	10	–	ns
t_{JTIXKH}[4][7]	TMS, TDI	10	–	ns

Table 6-7. JTAG Timings[1] (Continued)

Symbol	Parameter	Min	Max	Unit
	Output hold times:			
t_{JTKLDV}[5][7]	Boundary-scan data	–	10	ns
t_{JTKLOV}[5][7]	TDO	–	10	ns
	Output hold times:			
t_{JTKLDX}[5][7]	Boundary-scan data	1	–	ns
t_{JTKLOX}[5][7]	TDO	1	–	ns
	JTAG external clock to output hig impedance			
t_{JTKLDZ}[5][6]	Boundary-scan data	1	10	ns
t_{JTKLOZ}[5][6]	TDO	1	10	

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.
7. Guaranteed by design and device characterization.

7. Clock Configuration Modes

The PC8280 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins, PCI_MODE, PCI_CFG[0], PCI_MODCK, as shown in Table 7-1.

Table 7-1. PC8280 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK			
1			Local bus		Table 7-2 on page 26
0	0	0	PCI host	50-66	Table 7-3 on page 29
0	0	1		25-50	Table 7-4 on page 32
0	1	0	PCI agent	50-66	Table 7-5 on page 36
0	1	1		25-50	Table 7-6 on page 39

Note: 1. Determines PCI clock frequency range. Refer to Section 7.2 and Section 7.3.

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset: three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected PC8280 clock operation mode as described in the following sections.

7.1 Local Bus Mode

Table 7-2 lists clock configurations for the PC8280 in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Note: Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

Table 7-2. Clock Configurations for Local Bus Mode[1]

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High
Default Modes (MODCK_H = 0000)								
0000_000	37.5	133.3	3	112.5	400	4	150	533.3
0000_001	33.3	133.3	3	100	400	5	166.7	666.7
0000_010	37.5	100	4	150	400	4	150	400
0000_011	30	100	4	120	400	5	150	500
0000_100	60	167	2	120	334	2.5	150	417.5
0000_101	50	167	2	100	334	3	150	501
0000_110	60	160	2.5	150	400.	2.5	150	400
0000_111	50	160	2.5	125	400.	3	150	480
Full Configuration Modes								
0001_000	50	167	2	100	334	4	200	668
0001_001	50	167	2	100	334	5	250	835
0001_010	50	145.8	2	100	291.7	6	300	875
0001_011	Reserved							
0001_100	Reserved							
0001_101	37.5	133.3	3	112.5	400	4	150	533.3
0001_110	33.3	133.3	3	100	400	5	166.7	666.7
1000_111	33.3	133.3	3	100	400	5.5	183.3	733.3
0001_111	33.3	133.3	3	100	400	6	200	800
0010_000	Reserved							
0010_001	Reserved							
0010_010	37.5	100	4	150	400	4	150	400
0010_011	30	100	4	120	400	5	150	500
0010_100	25	100	4	100	400	6	150	600
0010_101	25	100	4	100	400	7	175	700
0010_110	25	100	4	100	400	8	200	800
0010_111	Reserved							
0011_000	30	80	5	150	400	5	150	400

Table 7-2. Clock Configurations for Local Bus Mode[1] (Continued)

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High
0011_001	25	80	5	125	400	6	150	480
0011_010	25	80	5	125	400	7	175	560
0011_011	25	80	5	125	400	8	200	640
0011_100	Reserved							
0011_101	Reserved							
0011_110	25	66.7	6	150	400	6	150	400
0011_111	25	66.7	6	150	400	7	175	466.7
0100_000	25	66.7	6	150	400	8	200	533.3
0101_101	75	167	2	150	334	2	166.7	334
0101_110	60	167	2	120	334	2.5	166.7	417.5
0101_111	50	167	2	100	334	3	200	501
0110_000	50	167	2	100	334	3.5	250	584.5
0110_001	50	167	2	100	334	4	250	668
0110_010	50	167	2	100	334	4.5	250	751.5
0110_011	Reserved							
0110_100	60	160	2.5	150	400	2.5	150	400
0110_101	50	160	2.5	125	400	3	150	480
0110_110	42.9	160	2.5	107.1	400	3.5	150	560
0110_111	40	160	2.5	100	400	4	160	640
0111_000	40	160	2.5	100	400	4.5	180	720
0111_001	Reserved							
0111_010	Reserved							
0111_011	50	133.3	3	150	400	3	150	400
0111_100	42.9	133.3	3	128.6	400	3.5	150	466.7
0111_101	37.5	133.3	3	112.5	400	4	150	533.3
0111_110	33.3	133.3	3	100	400	4.5	150	600
0111_111	Reserved							
1000_000	Reserved							
1000_001	Reserved							
1000_010	42.9	114.3	3.5	150	400	3.5	150	400
1000_011	37.5	114.3	3.5	131.3	400	4	150	457.1

Table 7-2. Clock Configurations for Local Bus Mode[1] (Continued)

Mode[2]	Bus Clock[3] (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High
1000_100	33.3	114.3	3.5	116.7	400	4.5	150	514.3
1000_101	30	114.3	3.5	105	400	5	150	571.4
1000_110	28.6	114.3	3.5	100	400	5.5	150	628.6
1100_000	Reserved							
1100_001	Reserved							
1100_010	Reserved							
1101_000	Reserved							

Notes:
1. The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor ≤3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor ≥ 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for RevA or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.
2. MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
3. 60x and local bus frequency. Identical to CLKin.
4. CPM multiplication factor = CPM clock/bus clock.
5. CPU multiplication factor = Core PLL multiplication factor.

7.2 PCI Host Mode

Table 7-3 on page 29 and Table 7-4 on page 32 show clock configurations for PCI host mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. In addition, note the following:

Notes:
1. PCI_MODCK
   In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.
2. Tval (Output Hold)
   The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

Table 7-3. Clock Configurations for PCI Host Mode (PCI_MODCK = 0)[1][2]

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H = 0000)											
0000_000	60	66.7	2	120	133.3	2.5	150	166.7	2	60	66.7
0000_001	50	66.7	2	100	133.3	3	150	200	2	50	66.7
0000_010	60	80	2.5	150	200	3	180	240	3	50	66.7
0000_011	60	80	2.5	150	200	3.5	210	280	3	50	66.7
0000_100	60	80	2.5	150	200	4	240	320	3	50	66.7
0000_101	50	66.7	3	150	200	3	150	200	3	50	66.7
0000_110	50	66.7	3.5	150	200	3.5	175	233.3	3	50	66.7
0000_111	50	66.7	3	150	200	4	200	266.6	3	50	66.7
Full Configuration Modes											
0001_000	50	66.7	3	150	200	5	250	333.3	3	50	66.7
0001_001	50	66.7	3	150	200	6	300	400	3	50	66.7
0001_010	50	66.7	3	150	200	7	350	466.6	3	50	66.7
0001_011	50	66.7	3	150	200	8	400	533.3	3	50	66.7
0010_000	50	66.7	4	200	266.6	5	250	333.3	4	50	66.7
0010_001	50	66.7	4	200	266.6	6	300	400	4	50	66.7
0010_010	50	66.7	4	200	266.6	7	350	466.6	4	50	66.7
0010_011	50	66.7	4	200	266.6	8	400	533.3	4	50	66.7
0010_100	75	100	4	300	400	5	375	500	6	50	66.7
0010_101	75	100	4	300	400	5.5	412.5	549.9	6	50	66.7
0010_110	75	100	4	300	400	6	450	599.9	6	50	66.7
0011_000	50	66.7	5	250	333.3	5	250	333.3	5	50	66.7
0011_001	50	66.7	5	250	333.3	6	300	400	5	50	66.7
0011_010	50	66.7	5	250	333.3	7	350	466.6	5	50	66.7
0011_011	50	66.7	5	250	333.3	8	400	533.3	5	50	66.7
0100_000	Reserved										
0100_001	50	66.7	6	300	400	6	300	400	6	50	66.7
0100_010	50	66.7	6	300	400	7	350	466.6	6	50	66.7
0100_011	50	66.7	6	300	400	8	400	533.3	6	50	66.7
0101_000	60	66.7	2	120	133.3	2.5	150	166.7	2	60	66.7
0101_001	50	66.7	2	100	133.3	3	150	200	2	50	66.7

Table 7-3. Clock Configurations for PCI Host Mode (PCI_MODCK = 0)[1][2] (Continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0101_010	50	66.7	2	100	133.3	3.5	175	233.3	2	50	66.7
0101_011	50	66.7	2	100	133.3	4	200	266.6	2	50	66.7
0101_100	50	66.7	2	100	133.3	4.5	225	300	2	50	66.7
0110_000	60	80	2.5	150	200	2.5	150	200	3	50	66.7
0110_001	60	80	2.5	150	200	3	180	240	3	50	66.7
0110_010	60	80	2.5	150	200	3.5	210	280	3	50	66.7
0110_011	60	80	2.5	150	200	4	240	320	3	50	66.7
0110_100	60	80	2.5	150	200	4.5	270	360	3	50	66.7
0110_101	60	80	2.5	150	200	5	300	400	3	50	66.7
0110_110	60	80	2.5	150	200	6	360	480	3	50	66.7
0111_000	Reserved										
0111_001	50	66.7	3	150	200	3	150	200	3	50	66.7
0111_010	50	66.7	3	150	200	3.5	175	233.3	3	50	66.7
0111_011	50	66.7	3	150	200	4	200	266.6	3	50	66.7
0111_100	50	66.7	3	150	200	4.5	225	300	3	50	66.7
1000_000	Reserved										
1000_001	66.7	88.9	3	200	266.6	3	200	266.6	4	50	66.7
1000_010	66.7	88.9	3	200	266.6	3.5	233.3	311.1	4	50	66.7
1000_011	66.7	88.9	3	200	266.6	4	266.7	355.5	4	50	66.7
1000_100	66.7	88.9	3	200	266.6	4.5	300	400	4	50	66.7
1000_101	66.7	88.9	3	200	266.6	6	400	533.3	4	50	66.7
1000_110	66.7	88.9	3	200	266.6	6.5	433.3	577.7	4	50	66.7
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	76.2	3.5	200	266.6	3.5	200	266.6	4	50	66.7
1001_011	57.1	76.2	3.5	200	266.6	4	228.6	304.7	4	50	66.7
1001_100	57.1	76.2	3.5	200	266.6	4.5	257.1	342.8	4	50	66.7
1001_101	85.7	114.3	3.5	300	400	5	428.6	571.4	6	50	66.7
1001_110	85.7	114.3	3.5	300	400	5.5	471.4	628.5	6	50	66.7
1001_111	85.7	114.3	3.5	300	400	6	514.3	685.6	6	50	66.7

Table 7-3. Clock Configurations for PCI Host Mode (PCI_MODCK = 0)[1][2] (Continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1010_000	75	100	2	150	200	2	150	200	3	50	66.7
1010_001	75	100	2	150	200	2.5	187.5	250	3	50	66.7
1010_010	75	100	2	150	200	3	225	300	3	50	66.7
1010_011	75	100	2	150	200	3.5	262.5	350	3	50	66.7
1010_100	75	100	2	150	200	4	300	400	3	50	66.7
1011_000	Reserved										
1011_001	80	106.7	2.5	200	266.6	2.5	200	266.6	4	50	66.7
1011_010	80	106.7	2.5	200	266.6	3	240	320	4	50	66.7
1011_011	80	106.7	2.5	200	266.6	3.5	280	373.3	4	50	66.7
1011_100	80	106.7	2.5	200	266.6	4	320	426.6	4	50	66.7
1011_101	80	106.7	2.5	200	266.6	4.5	360	480	4	50	66.7
1101_000	100	133.3	2.5	250	333.3	3	300	400	5	50	66.7
1101_001	100	133.3	2.5	250	333.3	3.5	350	466.6	5	50	66.7
1101_010	100	133.3	2.5	250	333.3	4	400	533.3	5	50	66.7
1101_011	100	133.3	2.5	250	333.3	4.5	450	599.9	5	50	66.7
1101_100	100	133.3	2.5	250	333.3	5	500	666.6	5	50	66.7
1101_101	125	166.7	2	250	333.3	3	375	500	5	50	66.7
1101_110	125	166.7	2	250	333.3	4	500	666.6	5	50	66.7
1110_000	100	133.3	3	300	400	3.5	350	466.6	6	50	66.7
1110_001	100	133.3	3	300	400	4	400	533.3	6	50	66.7
1110_010	100	133.3	3	300	400	4.5	450	599.9	6	50	66.7
1110_011	100	133.3	3	300	400	5	500	666.6	6	50	66.7
1110_100	100	133.3	3	300	400	5.5	550	733.3	6	50	66.7
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

Notes: 1. The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode.

For modes with a CPU multiplication factor ≤ 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor ≥ 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for RevA or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2. As Table 7-1 on page 25 shows, PCI_MODCK determines the PCI clock frequency range. Refer to Table 7-4 on page 32 for lower configurations.
3. MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
4. 60x and local bus frequency. Identical to CLKin.
5. CPM multiplication factor = CPM clock/bus clock.
6. CPU multiplication factor = Core PLL multiplication factor.

Table 7-4. Clock Configurations for PCI Host Mode (PCI_MODCK = 1)[1][2]

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H = 0000)											
0000_000	60	100	2	120	200	2.5	150	250	4	30	50
0000_001	50	100	2	100	200	3	150	300	4	25	50
0000_010	60	120	2.5	150	300	3	180	360	6	25	50
0000_011	60	120	2.5	150	300	3.5	210	420	6	25	50
0000_100	60	120	2.5	150	300	4	240	480	6	25	50
0000_101	50	100	3	150	300	3	150	300	6	25	50
0000_110	50	100	3	150	300	3.5	175	350	6	25	50
0000_111	50	100	3	150	300	4	200	400	6	25	50
Full Configuration Modes											
0001_000	50	100	3	150	300	5	250	500	6	25	50
0001_001	50	100	3	150	300	6	300	600	6	25	50
0001_010	50	100	3	150	300	7	350	700	6	25	50
0001_011	50	100	3	150	300	8	400	800	6	25	50
0010_000	50	100	4	200	400	5	250	500	8	25	50
0010_001	50	100	4	200	400	6	300	600	8	25	50
0010_010	50	100	4	200	400	7	350	700	8	25	50
0010_011	50	100	4	200	400	8	400	800	8	25	50
0010_100	37.5	75	4	150	300	5	187.5	375	6	25	50
0010_101	37.5	75	4	150	300	5.5	206.3	412.5	6	25	50
0010_110	37.5	75	4	150	300	6	225	450	6	25	50
0011_000	30	50	5	150	250	5	150	250	5	30	50
0011_001	25	50	5	125	250	6	150	300	5	25	50
0011_010	25	50	5	125	250	7	175	350	5	25	50

Table 7-4. Clock Configurations for PCI Host Mode (PCI_MODCK = 1)[1][2] (Continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0011_011	25	50	5	125	250	8	200	400	5	25	50
0100_000	Reserved										
0100_001	25	50	6	150	300	6	150	300	6	25	50
0100_010	25	50	6	150	300	7	175	350	6	25	50
0100_011	25	50	6	150	300	8	200	400	6	25	50
0101_000	60	100	2	120	200	2.5	150	250	4	30	50
0101_001	50	100	2	100	200	3	150	300	4	25	50
0101_010	50	100	2	100	200	3.5	175	350	4	25	50
0101_011	50	100	2	100	200	4	200	400	4	25	50
0101_100	50	100	2	100	200	4.5	225	450	4	25	50
0110_000	60	120	2.5	150	300	2.5	150	300	6	25	50
0110_001	60	120	2.5	150	300	3	180	360	6	25	50
0110_010	60	120	2.5	150	300	3.5	210	420	6	25	50
0110_011	60	120	2.5	150	300	4	240	480	6	25	50
0110_100	60	120	2.5	150	300	4.5	270	540	6	25	50
0110_101	60	120	2.5	150	300	5	300	600	6	25	50
0110_110	60	120	2.5	150	300	6	360	720	6	25	50
0111_000	Reserved										
0111_001	50	100	3	150	300	3	150	300	6	25	50
0111_010	50	100	3	150	300	3.5	175	350	6	25	50
0111_011	50	100	3	150	300	4	200	400	6	25	50
0111_100	50	100	3	150	300	4.5	225	450	6	25	50
1000_000	Reserved										
1000_001	66.7	133.3	3	200	400	3	200	400	8	25	50
1000_010	66.7	133.3	3	200	400	3.5	233.3	466.7	8	25	50
1000_011	66.7	133.3	3	200	400	4	266.7	533.3	8	25	50
1000_100	66.7	133.3	3	200	400	4.5	300	600	8	25	50
1000_101	66.7	133.3	3	200	400	6	400	800	8	25	50
1000_110	66.7	133.3	3	200	400	6.5	433.3	866.7	8	25	50

Table 7-4. Clock Configurations for PCI Host Mode (PCI_MODCK = 1)[1][2] (Continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	114.3	3.5	200	400	3.5	200	400	8	25	50
1001_011	57.1	114.3	3.5	200	400	4	228.6	457.1	8	25	50
1001_100	57.1	114.3	3.5	200	400	4.5	257.1	514.3	8	25	50
1001_101	42.9	85.7	3.5	150	300	5	214.3	428.6	6	25	50
1001_110	42.9	85.7	3.5	150	300	5.5	235.7	471.4	6	25	50
1010_000	75	150	2	150	300	2	150	300	6	25	50
1010_001	75	150	2	150	300	2.5	187.5	375	6	25	50
1010_010	75	150	2	150	300	3	225	450	6	25	50
1010_011	75	150	2	150	300	3.5	262.5	525	6	25	50
1010_100	75	150	2	150	300	4	300	600	6	25	50
1011_000	Reserved										
1011_001	80	160	2.5	200	400	2.5	200	400	8	25	50
1011_010	80	160	2.5	200	400	3	240	480	8	25	50
1011_011	80	160	2.5	200	400	3.5	280	560	8	25	50
1011_100	80	160	2.5	200	400	4	320	640	8	25	50
1011_101	80	160	2.5	200	400	4.5	360	720	8	25	50
1101_000	50	100	2.5	125	250	3	150	300	5	25	50
1101_001	50	100	2.5	125	250	3.5	175	350	5	25	50
1101_010	50	100	2.5	125	250	4	200	400	5	25	50
1101_011	50	100	2.5	125	250	4.5	225	450	5	25	50
1101_100	50	100	2.5	125	250	5	250	500	5	25	50
1101_101	62.5	125	2	125	250	3	187.5	375	5	25	50
1101_110	62.5	125	2	125	250	4	250	500	5	25	50
1110_000	50	100	3	150	300	3.5	175	350	6	25	50
1110_001	50	100	3	150	300	4	200	400	6	25	50
						.		.			.
1110_011	50	100	3	150	300	5	250	500	6	25	50

Table 7-4. Clock Configurations for PCI Host Mode (PCI_MODCK = 1)[1][2] (Continued)

Mode[3]	Bus Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPM Multiplication Factor[6]	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1110_100	50	100	3	150	300	5.5	275	550	6	25	50
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

Notes:
1. The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor ≤3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor ≥ 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for RevA or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.
2. As Table 7-1 on page 25 shows, PCI_MODCK determines the PCI clock frequency range. Refer to Table 7-3 on page 29 for higher configurations.
3. MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
4. 60x and local bus frequency. Identical to CLKin.
5. CPM multiplication factor = CPM clock/bus clock.
6. CPU multiplication factor = Core PLL multiplication factor.

7.3 PCI Agent Mode

Table 7-5 and Table 7-6 on page 39 show configurations for PCI agent mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. In addition, note the following:

Notes:
1. PCI_MODCK
   In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.
2. Tval (Output Hold)
   The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

Table 7-5. Clock Configurations for PCI Agent Mode (PCI_MODCK = 0)[1][2]

Mode[3]	PCI Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H = 0000)											
0000_000	60	66.7	2	120	133.3	2.5	150	166.7	2	60	66.7
0000_001	50	66.7	2	100	133.3	3	150	200	2	50	66.7
0000_010	50	66.7	3	150	200	3	150	200	3	50	66.7
0000_011	50	66.7	3	150	200	4	200	266.6	3	50	66.7
0000_100	50	66.7	3	150	200	3	180	240	2.5	60	80
0000_101	50	66.7	3	150	200	3.5	210	280	2.5	60	80
0000_110	50	66.7	4	200	266.6	3.5	233.3	311.1	3	66.7	88.9
0000_111	50	66.7	4	200	266.6	3	240	320	2.5	80	106.7
Full Configuration Modes											
0001_001	60	66.7	2	120	133.3	5	150	166.7	4	30	33.3
0001_010	50	66.7	2	100	133.3	6	150	200	4	25	33.3
0001_011	50	66.7	2	100	133.3	7	175	233.3	4	25	33.3
0001_100	50	66.7	2	100	133.3	8	200	266.6	4	25	33.3
0010_001	50	66.7	3	150	200	3	180	240	2.5	60	80
0010_010	50	66.7	3	150	200	3.5	210	280	2.5	60	80
0010_011	50	66.7	3	150	200	4	240	320	2.5	60	80
0010_100	50	66.7	3	150	200	4.5	270	360	2.5	60	80
0011_000	Reserved										
0011_001	Reserved										
0011_010	Reserved										
0011_011	Reserved										
0011_100	Reserved										
0100_000	Reserved										
0100_001	50	66.7	2	150	200	3	150	200	3	50	66.7
0100_010	50	66.7	3	150	200	3.5	175	200	3	50	66.7
0100_011	50	66.7	3	150	200	4	200	266.6	3	50	66.7
0100_100	50	66.7	3	150	200	4.5	225	300	3	50	66.7
0101_000	50	66.7	5	250	333.3	2.5	250	333.3	2.5	100	133.3
0101_001	50	66.7	5	250	333.3	3	300	400	2.5	100	133.3
0101_010	50	66.7	5	250	333.3	3.5	350	466.6	2.5	100	133.3

Table 7-5. Clock Configurations for PCI Agent Mode (PCI_MODCK = 0)[1][2] (Continued)

Mode[3]	PCI Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0101_011	50	66.7	5	250	333.3	4	400	533.3	2.5	100	133.3
0101_100	50	66.7	5	250	333.3	4.5	450	599.9	2.5	100	133.3
0101_101	50	66.7	5	250	333.3	5	500	666.6	2.5	100	133.3
0101_110	50	66.7	5	250	333.3	5.5	550	733.3	2.5	100	133.3
0110_000	Reserved										
0110_001	50	66.7	4	200	266.6	3	200	266.6	3	66.7	88.9
0110_010	50	66.7	4	200	266.6	3.5	233.3	311.1	3	66.7	88.9
0110_011	50	66.7	4	200	266.6	4	266.7	355.5	3	66.7	88.9
0110_100	50	66.7	4	200	266.6	4.5	300	400	3	66.7	88.9
0111_000	50	66.7	3	150	200	2	150	200	2	75	100
0111_001	50	66.7	3	150	200	2.5	187.5	250	2	75	100
0111_010	50	66.7	3	150	200	3	225	300	2	75	100
0111_011	50	66.7	3	150	200	3.5	262.5	350	2	75	100
1000_000	Reserved										
1000_001	50	66.7	3	150	200	2.5	150	166.7	2.5	60	80
1000_010	50	66.7	3	150	200	3	180	240	2.5	60	80
1000_011	50	66.7	3	150	200	3.5	210	280	2.5	60	80
1000_100	50	66.7	3	150	200	4	240	320	2.5	60	80
1000_101	50	66.7	3	150	200	4.5	270	360	2.5	60	80
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50	66.7	4	200	266.6	4	200	266.6	4	50	66.7
1001_100	50	66.7	4	200	266.6	4.5	225	300	4	50	66.7
1010_000	Reserved										
1010_001	50	66.7	4	200	266.6	3	200	266.6	3	66.7	88.9
1010_010	50	66.7	4	200	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50	66.7	4	200	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50	66.7	4	200	266.6	4.5	300	400	3	66.7	88.9
1011_000	Reserved										

Table 7-5. Clock Configurations for PCI Agent Mode (PCI_MODCK = 0)[1][2] (Continued)

Mode[3]	PCI Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_001	50	66.7	4	200	266.6	2.5	200	266.6	2.5	80	106.7
1011_010	50	66.7	4	200	266.6	3	240	320	2.5	80	106.7
1011_011	50	66.7	4	200	266.6	3.5	280	373.3	2.5	80	106.7
1011_100	50	66.7	4	200	266.6	4	320	426.6	2.5	80	106.7
1100_101	50	66.7	6	300	400	4	400	533.3	3	100	133.3
1100_110	50	66.7	6	300	400	4.5	450	599.9	3	100	133.3
1100_111	50	66.7	6	300	400	5	500	666.6	3	100	133.3
1101_000	50	66.7	6	300	400	5.5	550	733.3	3	100	133.3
1101_001	50	66.7	6	300	400	3.5	420	559.9	2.5	120	160
1101_010	50	66.7	6	300	400	4	480	639.9	2.5	120	160
1101_011	50	66.7	6	300	400	4.5	540	719.9	2.5	120	160
1101_100	50	66.7	6	300	400	5	600	799.9	2.5	120	160
1110_000	50	66.7	5	250	333.3	2.5	312.5	416.6	2	125	166.7
1110_001	50	66.7	5	250	333.3	3	375	500	2	125	166.7
1110_010	50	66.7	5	250	333.3	3.5	437.5	583.3	2	125	166.7
1110_011	50	66.7	5	250	333.3	4	500	666.6	2	125	166.7
1110_100	50	66.7	5	250	333.3	4	333.3	444.4	3	83.3	111.1
1110_101	50	66.7	5	250	333.3	4.5	375	500	3	83.3	111.1
1110_110	50	66.7	5	250	333.3	5	416.7	555.5	3	83.3	111.1
1110_111	50	66.7	5	250	333.3	5.5	458.3	611.1	3	83.3	111.1
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

Notes:
1. The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor ≤3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor ≥ 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for RevA or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.
2. As shown in Table 7-1 on page 25, PCI_MODCK determines the PCI clock frequency range. Refer to Table 7-6 for lower configurations.

3. MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
4. CPM multiplication factor = CPM clock/PCI clock.
5. CPU multiplication factor = Core PLL multiplication factor.

Table 7-6. Clock Configurations for PCI Agent Mode (PCI_MODCK = 1)[1][2]

Mode[3]	PCI Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H = 0000)											
0000_000	30	50	4	120	200	2.5	150	250	2	60	100
0000_001	25	50	4	100	200	3	150	300	2	50	100
0000_010	25	50	6	150	300	3	150	300	3	50	100
0000_011	25	50	6	150	300	4	200	400	3	50	100
0000_100	25	50	6	150	300	3	180	360	2.5	60	120
0000_101	25	50	6	150	300	3.5	210	420	2.5	60	120
0000_110	25	50	8	200	400	3.5	233.3	466.7	3	66.7	133.3
0000_111	25	50	8	200	400	3	240	480	2.5	80	160
Full Configuration Modes											
0001_001	30	50	4	120	200	5	150	250	4	30	50
0001_010	25	50	4	100	200	6	150	300	4	25	50
0001_011	25	50	4	100	200	7	175	350	4	25	50
0001_100	25	50	4	100	200	8	200	400	4	25	50
0010_001	25	50	6	150	300	3	180	360	2.5	60	120
0010_010	25	50	6	150	300	3.5	210	420	2.5	60	120
0010_011	25	50	6	150	300	4	240	480	2.5	60	120
0010_100	25	50	6	150	300	4.5	270	540	2.5	60	120
0011_000	Reserved										
0011_001	37.5	50	4	150	200	3	150	200	3	50	66.7
0011_010	32.1	50	4	128.6	200	3.5	150	233.3	3	42.9	66.7
0011_011	28.1	50	4	112.5	200	4	150	266.7	3	37.5	66.7
0011_100	25	50	4	100	200	4.5	150	300	3	33.3	66.7
0100_000	Reserved										
0100_001	25	50	6	150	300	3	150	300	3	50	100
0100_010	25	50	6	150	300	3.5	175	350	3	50	100
0100_011	25	50	6	150	300	4	200	400	3	50	100
0100_100	25	50	6	150	300	4.5	225	450	3	50	100

Table 7-6. Clock Configurations for PCI Agent Mode (PCI_MODCK = 1)[1][2] (Continued)

Mode[3]	PCI Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0101_000	30	50	5	150	250	2.5	150	250	2.5	60	100
0101_001	25	50	5	125	250	3	150	300	2.5	50	100
0101_010	25	50	5	125	250	3.5	175	350	2.5	50	100
0101_011	25	50	5	125	250	4	200	400	2.5	50	100
0101_100	25	50	5	125	250	4.5	225	450	2.5	50	100
0101_101	25	50	5	125	250	5	250	500	2.5	50	100
0101_110	25	50	5	125	250	5.5	275	550	2.5	50	100
0110_000	Reserved										
0110_001	25	50	8	200	400	3	200	400	3	66.7	133.3
0110_010	25	50	8	200	400	3.5	233.3	466.7	3	66.7	133.3
0110_011	25	50	8	200	400	4	266.7	533.3	3	66.7	133.3
0110_100	25	50	8	200	400	4.5	300	600	3	66.7	133.3
0111_000	25	50	6	150	300	2	150	300	2	75	150
0111_001	25	50	6	150	300	2.5	187.5	375	2	75	150
0111_010	25	50	6	150	300	3	225	450	2	75	150
0111_011	25	50	6	150	300	3.5	262.5	525	2	75	150
1000_000	Reserved										
1000_001	25	50	6	150	300	2.5	150	300	2.5	60	120
1000_010	25	50	6	150	300	3	180	360	2.5	60	120
1000_011	25	50	6	150	300	3.5	210	420	2.5	60	120
1000_100	25	50	6	150	300	4	240	480	2.5	60	120
1000_101	25	50	6	150	300	4.5	270	540	2.5	60	120
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	25	50	8	200	400	4	200	400	4	50	100
1001_100	25	50	8	200	400	4.5	225	450	4	50	100
1010_000	Reserved										
1010_001	25	50	8	200	400	3	200	400	3	66.7	133.3
1010_010	25	50	8	200	400	3.5	233.3	466.7	3	66.7	133.3

Table 7-6. Clock Configurations for PCI Agent Mode (PCI_MODCK = 1)[1][2] (Continued)

Mode[3]	PCI Clock[4] (MHz)		CPM Multiplication Factor[5]	CPM Clock (MHz)		CPU Multiplication Factor	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1010_011	25	50	8	200	400	4	266.7	533.3	3	66.7	133.3
1010_100	25	50	8	200	400	4.5	300	600	3	66.7	133.3
1011_000	Reserved										
1011_001	25	50	8	200	400	2.5	200	400	2.5	80	160
1011_010	25	50	8	200	400	3	240	480	2.5	80	160
1011_011	25	50	8	200	400	3.5	280	560	2.5	80	160
1011_100	25	50	8	200	400	4	320	640	2.5	80	160
1100_101	25	50	6	150	300	4	200	400	3	50	100
1100_110	25	50	6	150	300	4.5	225	450	3	50	100
1100_111	25	50	6	150	300	5	250	500	3	50	100
1101_000	25	50	6	150	300	5.5	275	550	3	50	100
1101_001	25	50	6	150	300	3.5	210	420	2.5	60	120
1101_010	25	50	6	150	300	4	240	480	2.5	60	120
1101_011	25	50	6	150	300	4.5	270	540	2.5	60	120
1101_100	25	50	6	150	300	5	300	600	2.5	60	120
1110_000	25	50	5	125	250	2.5	156.3	312.5	2	62.5	125
1110_001	25	50	5	125	250	3	187.5	375	2	62.5	125
1110_010	25	50	5	125	250	3.5	218.8	437.5	2	62.5	125
1110_011	25	50	5	125	250	4	250	500	2	62.5	125
1110_100	25	50	5	125	250	4	166.7	333.3	3	41.7	83.3
1110_101	25	50	5	125	250	4.5	187.5	375	3	41.7	83.3
1110_110	25	50	5	125	250	5	208.3	416.7	3	41.7	83.3
1110_111	25	50	5	125	250	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

Notes: 1. The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not violate the frequency rating of the user’s device. The minimum CPM frequency is 120 MHz. Minimum CPU frequency is determined by the clock mode.

For modes with a CPU multiplication factor ≤ 3, the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. For modes with a CPU multiplication factor ≥ 3.5: for Rev0.1 the minimum CPU frequency is 250 MHz; for RevA or later the minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices.

2. As shown in Table 7-1 on page 25, PCI_MODCK determines the PCI clock range. Refer to Table 7-5 on page 36 for higher range configurations.
3. MODCK_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
4. CPM multiplication factor = CPM clock/PCI clock.
5. CPU multiplication factor = Core PLL multiplication factor.

8. Pinout

This section provides the pin assignments and pinout lists for PowerQUICC II TBGA package.

The following figures and table represent the standard 480 TBGA package.

Figure 8-1 on page 43 shows the pinout of the package as viewed from the top surface.

Figure 8-1. Pinout of the 480 TBGA Package (View from Top)

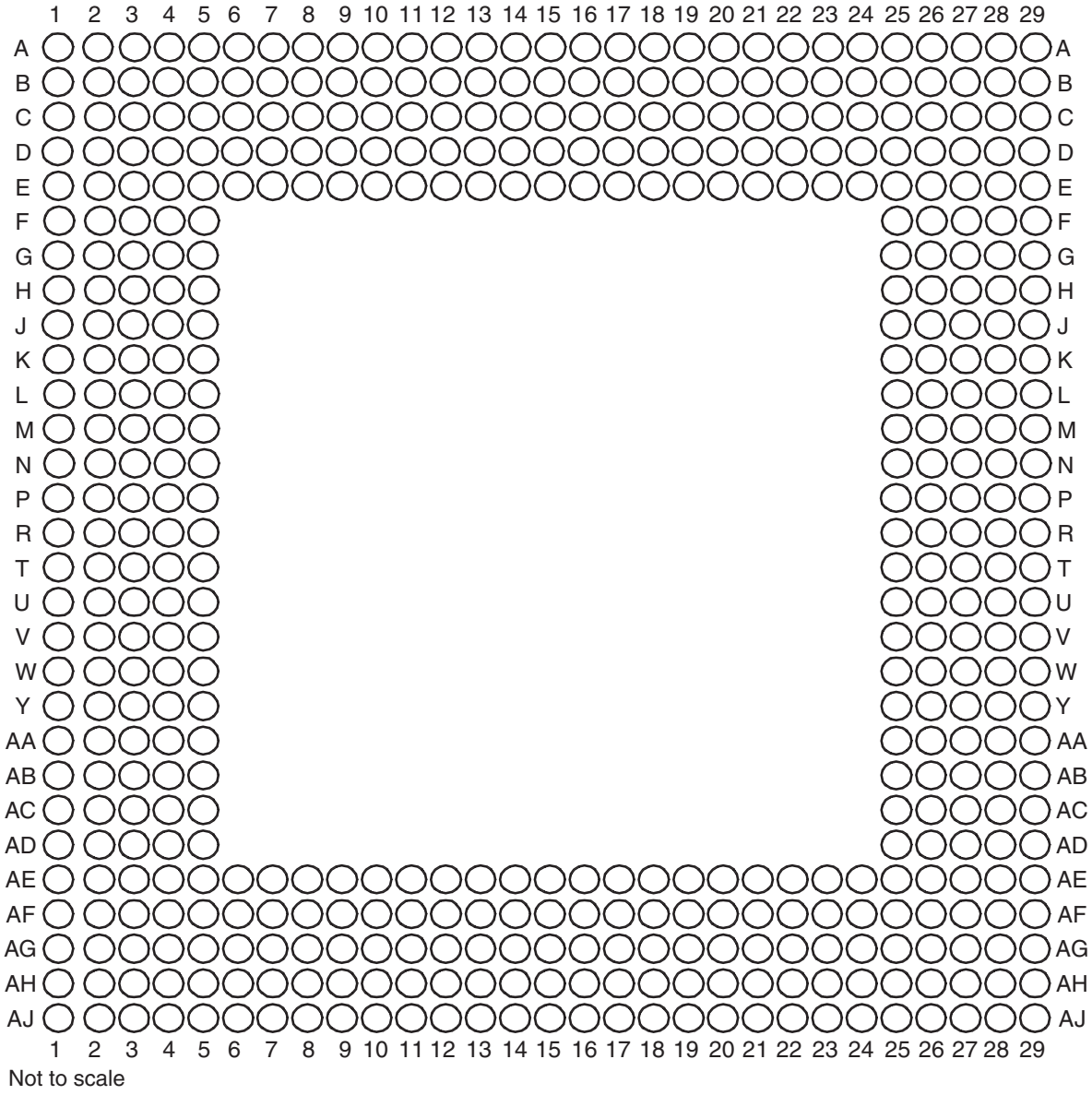


Figure 8-2 shows the side profile of the TBGA package to indicate the direction of the top surface view.

Figure 8-2. Side View of the TBGA Package

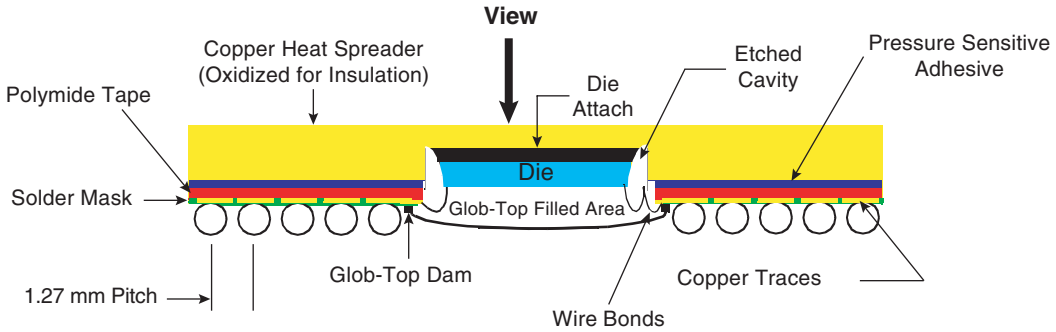


Table 8-1 shows the pinout list of the PC8280 and MPC8270. Table 8-2 on page 56 defines conventions and acronyms used in Table 8-2 on page 56.

Table 8-1. PC8280 and PC8270 Pinout List

Pin Name		Ball
PC8280/PC8270	PC8280 only	
$\overline{BR}$		W5
$\overline{BG}$		F4
$\overline{ABB}/\overline{IRQ2}$		E2
TS		E3
A0		G1
A1		H5
A2		H2
A3		H1
A4		J5
A5		J4
A6		J3
A7		J2
A8		J1
A9		K4
A10		K3
A11		K2
A12		K1
A13		L5
A14		L4
A15		L3
A16		L2
A17		L1
A18		M5
A19		N5
A20		N4
A21		N3
A22		N2
A23		N1
A24		P4
A25		P3
A26		P2
A27		P1
A28		R1
A29		R3
A30		R5

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	PC8280 only	
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
$\overline{\text{TBST}}$		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
$\overline{\text{AACK}}$		F3
$\overline{\text{ARTRY}}$		E1
$\overline{\text{DBG}}$		V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4
D16		D19
D17		D17
D18		D15
D19		C13
D20		B11
D21		A8

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	PC8280 only	
D22		A5
D23		C5
D24		C19
D25		C17
D26		C15
D27		D13
D28		C11
D29		B8
D30		A4
D31		E6
D32		E18
D33		B17
D34		A15
D35		A12
D36		D11
D37		C8
D38		E7
D39		A3
D40		D18
D41		A17
D42		A14
D43		B12
D44		A10
D45		D8
D46		B6
D47		C4
D48		C18
D49		E16
D50		B14
D51		C12
D52		B10
D53		A7
D54		C6
D55		D5
D56		B18
D57		B16
D58		E14

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	
D59		D12
D60		C10
D61		E8
D62		D6
D63		C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$		B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$		A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$		E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$		D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$		C21
$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$		B21
$\overline{\text{IRQ6}}$/DP6/CSE0		A21
$\overline{\text{IRQ7}}$/DP7/CSE1		E20
$\overline{\text{PSDVAL}}$		V3
$\overline{\text{TA}}$		C22
$\overline{\text{TEA}}$		V5
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$		W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$		U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$		U3
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$		Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$		U4
$\overline{\text{CPU\_DBG}}$		R2
$\overline{\text{CPU\_BR}}$		Y3
$\overline{\text{CS0}}$		F25
$\overline{\text{CS1}}$		C29
$\overline{\text{CS2}}$		E27
$\overline{\text{CS3}}$		E28
$\overline{\text{CS4}}$		F26
$\overline{\text{CS5}}$		F27
$\overline{\text{CS6}}$		F28
$\overline{\text{CS7}}$		G25
$\overline{\text{CS8}}$		D29
$\overline{\text{CS9}}$		E29
$\overline{\text{CS10}}$/$\overline{\text{BCTL1}}$		F29
$\overline{\text{CS11}}$/AP0		G28
BADDR27		T5
BADDR28		U1

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	PC8280 only	
ALE		T2
$\overline{\text{BCTL0}}$		A27
$\overline{\text{PWE0}}$/PSDDQM0/$\overline{\text{PBS0}}$		C25
$\overline{\text{PWE1}}$/PSDDQM1/$\overline{\text{PBS1}}$		E24
$\overline{\text{PWE2}}$/PSDDQM2/$\overline{\text{PBS2}}$		D24
$\overline{\text{PWE3}}$/PSDDQM3/$\overline{\text{PBS3}}$		C24
$\overline{\text{PWE4}}$/PSDDQM4/$\overline{\text{PBS4}}$		B26
$\overline{\text{PWE5}}$/PSDDQM5/$\overline{\text{PBS5}}$		A26
$\overline{\text{PWE6}}$/PSDDQM6/$\overline{\text{PBS6}}$		B25
$\overline{\text{PWE7}}$/PSDDQM7/$\overline{\text{PBS7}}$		A25
PSDA10/PGPL0		E23
$\overline{\text{PSDWE}}$/PGPL1		B24
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2		A24
$\overline{\text{PSDCAS}}$/PGPL3		B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$		A23
PSDAMUX/PGPL5		D22
$\overline{\text{LWE0}}$/$\overline{\text{LSDDQM0}}$/$\overline{\text{LBS0}}$/PCI_CFG0		H28
$\overline{\text{LWE1}}$/$\overline{\text{LSDDQM1}}$/$\overline{\text{LBS1}}$/PCI_CFG1		H27
$\overline{\text{LWE2}}$/$\overline{\text{LSDDQM2}}$/$\overline{\text{LBS2}}$/PCI_CFG2		H26
$\overline{\text{LWE3}}$/$\overline{\text{LSDDQM3}}$/$\overline{\text{LBS3}}$/PCI_CFG3		G29
LSDA10/LGPL0/PCI_MODCKH0		D27
$\overline{\text{LSDWE}}$/LGPL1/PCI_MODCKH1		C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2/PCI_MODCKH2		E26
$\overline{\text{LSDCAS}}$/LGPL3/PCI_MODCKH3		D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
$\overline{\text{LWR}}$		D28
L_A14/PAR		N27
L_A15/$\overline{\text{FRAME}}$/$\overline{\text{SMI}}$		T29
L_A16/$\overline{\text{TRDY}}$		R27
L_A17/$\overline{\text{IRDY}}$/$\overline{\text{CKSTP\_OUT}}$		R26
L_A18/$\overline{\text{STOP}}$		R29
L_A19/$\overline{\text{DEVSEL}}$		R28
L_A20/IDSEL		W29
L_A21/$\overline{\text{PERR}}$		P28
L_A22/$\overline{\text{SERR}}$		N26
L_A23/$\overline{\text{REQ0}}$		AA27

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	PC8280 only	
L_A24/$\overline{\text{REQ1}}$/HSEJSW		P29
L_A25/$\overline{\text{GNT0}}$		AA26
L_A26/$\overline{\text{GNT1}}$/HSLED		N25
L_A27/$\overline{\text{GNT2}}$/$\overline{\text{HSENUM}}$		AA25
L_A28/$\overline{\text{RST}}$/$\overline{\text{CORE\_SRESET}}$		AB29
L_A29/$\overline{\text{INTA}}$		AB28
L_A30/$\overline{\text{REQ2}}$		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27
LCL_D9/AD9		L26
LCL_D10/AD10		L25
LCL_D11/AD11		M29
LCL_D12/AD12		M28
LCL_D13/AD13		M27
LCL_D14/AD14		M26
LCL_D15/AD15		N29
LCL_D16/AD16		T25
LCL_D17/AD17		U27
LCL_D18/AD18		U26
LCL_D19/AD19		U25
LCL_D20/AD20		V29
LCL_D21/AD21		V28
LCL_D22/AD22		V27
LCL_D23/AD23		V26
LCL_D24/AD24		W27
LCL_D25/AD25		W26
LCL_D26/AD26		W25
LCL_D27/AD27		Y29
LCL_D28/AD28		Y28

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	
LCL_D29/AD29		Y25
LCL_D30/AD30		AA29
LCL_D31/AD31		AA28
LCL_DP0/C0/$\overline{BE0}$		L28
LCL_DP1/C1/$\overline{BE1}$		N28
LCL_DP2/C2/$\overline{BE2}$		T28
LCL_DP3/C3/$\overline{BE3}$		W28
$\overline{IRQ0}$/NMI_OUT		T1
$\overline{IRQ7}$/$\overline{INT\_OUT}$/$\overline{APE}$		D1
$\overline{TRST}$[1]		AH3
TCK		AG5
TMS		AJ3
TDI		AE6
TDO		AF5
TRIS		AB4
$\overline{PORESET}$[1]		AG6
$\overline{HRESET}$		AH5
$\overline{SRESET}$		AF6
$\overline{QREQ}$		AA3
$\overline{RSTCONF}$		AJ4
MODCK1/AP1/TC0/BNKSEL0		W2
MODCK2/AP2/TC1/BNKSEL1		W3
MODCK3/AP3/TC2/BNKSEL2		W4
CLKin1		AH4
PA0/$\overline{RESTART1}$/DREQ3	FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{REJECT1}$/$\overline{DONE3}$	FCC2_UTM_TXADDR1	AC25[2]
PA2/CLK20/$\overline{DACK3}$	FCC2_UTM_TXADDR0	AE28[2]
PA3/CLK19/$\overline{DACK4}$/L1RXD1A2	FCC2_UTM_RXADDR0	AG29[2]
PA4/$\overline{REJECT2}$/$\overline{DONE4}$	FCC2_UTM_RXADDR1	AG28[2]
PA5/$\overline{RESTART2}$/DREQ4	FCC2_UTM_RXADDR2/ FCC1_UT_RXPRTY	AG26[2]
PA6/FCC2_RXADDR3	L1RSYNCA1	AE24[2]
PA7/SMSYN2/FCC2_TXADDR3	L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/FCC2_TXADDR4	L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2	L1TXD0A1	AH23[2]
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	AE22[2]

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	**Ball**
PA11/MSNUM4	FCC1_UT8_RXD1/ FCC1_UT16_RXD9	AH22(2)
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	AJ21(2)
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	AH20(2)
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	AG19(2)
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT8_RXD5/ FCC1_UT16_RXD13	AF18(2)
PA16/FCC1_MII_HDLC_RXD1/ FCCI_RMII_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	AF17(2)
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCCI_RMII_RXD0	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	AE16(2)
PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT8_TXD7/ FCC1_UT16_TXD15	AJ16(2)
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/ FCC1_UT16_TXD14	AG15(2)
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/ FCC1_UT16_TXD13	AJ13(2)
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/ FCC1_UT16_TXD12	AE13(2)
PA22	FCC1_UT8_TXD3/ FCC1_UT16_TXD11	AF12(2)
PA23	FCC1_UT8_TXD2/ FCC1_UT16_TXD10	AG11(2)
PA24/MSNUM1	FCC1_UT8_TXD1/ FCC1_UT16_TXD9	AH9(2)
PA25/MSNUM0	FCC1_UT8_TXD0/ FCC1_UT16_TXD8	AJ8(2)
PA26/FCC1_RMII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	AH7(2)
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRS_DV	FCC1_UT_RXSOC	AF7(2)
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	$\overline{\text{FCC1\_UTM\_RXENB}}$/ $\overline{\text{FCC1\_UTS\_RXENB}}$	AD5(2)
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	AF1(2)
PA30/FCC1_MII_CRS/ $\overline{\text{FCC1\_RTS}}$	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	AD3(2)
PA31/FCC1_MII_COL	$\overline{\text{FCC1\_UTM\_TXENB}}$/ $\overline{\text{FCC1\_UTS\_TXENB}}$	AB5(2)
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	FCC2_UT8_RXD0	AD28(2)

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	**Ball**
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD26[2]
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AD25[2]
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26[2]
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/FCC3_RXD/TXD3	FCC2_UT8_TXD3/L1RSYNCD1	AH27[2]
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2/ L1TSYNCD1/L1GNTD1	AG24[2]
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24[2]
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/TXD2	L1CLKOB1/L1RSYNCC1	AG22[2]
PB13/FCC3_MII_COL/L1TXD1A2	$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1	AH21[2]
PB14/FCC3_MII_RMII_TX_EN/RXD3	L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19[2]
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18[2]
PB17/FCC3_MII_RX_DV/ CLK17/FCC3_RMII_CRS_DV	L1RQA1	AJ17[2]
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14[2]
PB19FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13[2]
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12[2]
PB21/FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/ L1TSYNCD2/L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11[2]
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16[2]
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15[2]
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9[2]
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7[2]
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6[2]
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1		AE3[2]

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	**Ball**
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2(2)
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5(2)
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4(2)
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2		AB26(2)
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$/$\overline{\text{SPISEL}}$		AD29(2)
PC2/$\overline{\text{FCC3_CD}}$/$\overline{\text{DONE2}}$	FCC2_UT8_TXD3	AE29(2)
PC3/$\overline{\text{FCC3_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$/$\overline{\text{USB_RP}}$	FCC2_UT8_TXD2	AE27(2)
PC4/SI2_L1ST4/FCC2_CD	$\overline{\text{FCC2_UTM_RXENB}}$/ $\overline{\text{FCC2_UTS_RXENB}}$	AF27(2)
PC5/SI2_L1ST3/$\overline{\text{FCC2_CTS}}$	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AF24(2)
PC6/$\overline{\text{FCC1_CD}}$	L1CLKOC1/FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26(2)
PC7/$\overline{\text{FCC1_CTS}}$	$\overline{\text{L1RQC1}}$/FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25(2)
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/ $\overline{\text{CTS3}}$/USBRN	FCC1_UT16_TXD0	AF22(2)
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	AE21(2)
PC10/$\overline{\text{CD3}}$/RENA3	FCC1_UT16_TXD2/SI1_L1ST4/ FCC2_UT8_RXD3	AF20(2)
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	L1CLKOD1/FCC2_UT8_RXD2	AE19(2)
PC12/$\overline{\text{CD2}}$/RENA2	SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	AE18(2)
PC13/$\overline{\text{CTS2}}$/CLSN2	$\overline{\text{L1RQD1}}$/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	AH18(2)
PC14/$\overline{\text{CD1}}$/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	AH17(2)
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	AG16(2)
PC16/CLK16/TIN4		AF15(2)
PC17/CLK15/TIN3/BRGO8		AJ15(2)
PC18/CLK14/$\overline{\text{TGATE2}}$		AH14(2)
PC19/CLK13/BRGO7/SPICLK		AG13(2)
PC20/CLK12/$\overline{\text{TGATE1}}$/USB_OE		AH12(2)
PC21/CLK11/BRGO6		AJ11(2)
PC22/CLK10/$\overline{\text{DONE1}}$/FCC1_UT_TXPRTY		AG10(2)
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$		AE10(2)

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	
PC24/CLK8/$\overline{\text{TOUT4}}$	FCC2_UT8_TXD3	AF9[2]
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	AE8[2]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK		AJ6[2]
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		AG2[2]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2/FCC2_RXADDR4		AF3[2]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1		AF2[2]
PC30/CLK2/$\overline{\text{TOUT1}}$	FCC2_UT8_TXD3	AE1[2]
PC31/CLK1/BRGO1		AD1[2]
PD4/BRGO8/$\overline{\text{FCC3\_RTS}}$/SMRXD2	L1TSYNCD1/L1GNTD1	AC28[2]
PD5/$\overline{\text{DONE1}}$	FCC1_UT16_TXD3	AD27[2]
PD6/$\overline{\text{DACK1}}$	FCC1_UT16_TXD4	AF29[2]
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AF28[2]
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AG25[2]
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	AH26[2]
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$	FCC2_UT8_RXD0/ L1TSYNCB1/L1GNTB1	AJ23[2]
PD12	SI1_L1ST2/L1RXDB1	AG23[2]
PD13	SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	AE20[2]
PD15/$\overline{\text{L1RQC2}}$/I2CSDA	FCC1_UT16_RXD1	AJ20[2]
PD16/SPIMISO	FCC1_UT_TXPRTY/ L1TSYNCC1/L1GNTC1	AG18[2]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	AG17[2]
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	AF16[2]
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	AJ14[2]

Table 8-1. PC8280 and PC8270 Pinout List (Continued)

Pin Name		Ball
PC8280/PC8270	**PC8280 only**	**Ball**
PD21/TXD4/L1RXD0A2/ L1RXDA2/USB_TN	FCC1_UT16_RXD3	AH13[2]
PD22/RXD4L1TXD0A2/ L1TXDA2/USB_RXD	FCC1_UT16_TXD5	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3	FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3	FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3	FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2	FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2	FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2	FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	AG1[2]
PD30/TXD1	$\overline{\text{FCC2\_UTM\_TXENB}}$/ $\overline{\text{FCC2\_UTS\_TXENB}}$	AD4[2]
PD31/RXD1		AD2[2]
VCCSYN		AB3
VCCSYN1		B9
CLKin2		AE11
SPARE4[3]		U5
$\overline{\text{PCI\_MODE}}$[4]		AF25
SPARE6[3]		V4
Noconnect[5]		AA1, AG4
I/Opower		AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core power		U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground		AA5, AB1[6], AB2[7], AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

Notes:
1. Should be tied to VDDH via a 2 kΩ external pull-up resistor.
2. The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.
3. Must be pulled down or left floating.

4. If PCI is not desired, must be pulled up or left floating.
5. Sphere is not connected to die.
6. GNDSYN (AB1): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the PC8280. New designs must connect AB1 to GND and follow the suggestions in Section 4.6 ”Layout Practices” on page 14. Old designs in which the PC8280 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.
7. XFC (AB2) pin: This pin is used in MPC826x(A) devices; it is not used in PC8280 because there is no need for external capacitor to operate the PLL. New designs should connect AB2 (XFC) pin to GND. Old designs in which the PC8280 is used as a drop-in replacement can leave the pin connected to the current capacitor.

Symbols used in Table 8-2 are described in Table 9-1 on page 56.

Table 8-2. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low
UTM	Indicates that a signal is part of the UTOPIA master interface
UTS	Indicates that a signal is part of the UTOPIA slave interface
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface
MII	Indicates that a signal is part of the media independent interface
RMII	Indicates that a signal is part of the reduced media independent interface

9. Package Description

The following sections provide the package parameters and mechanical dimensions.

9.1 Package Parameters

Package parameters are provided in Table 9-1.

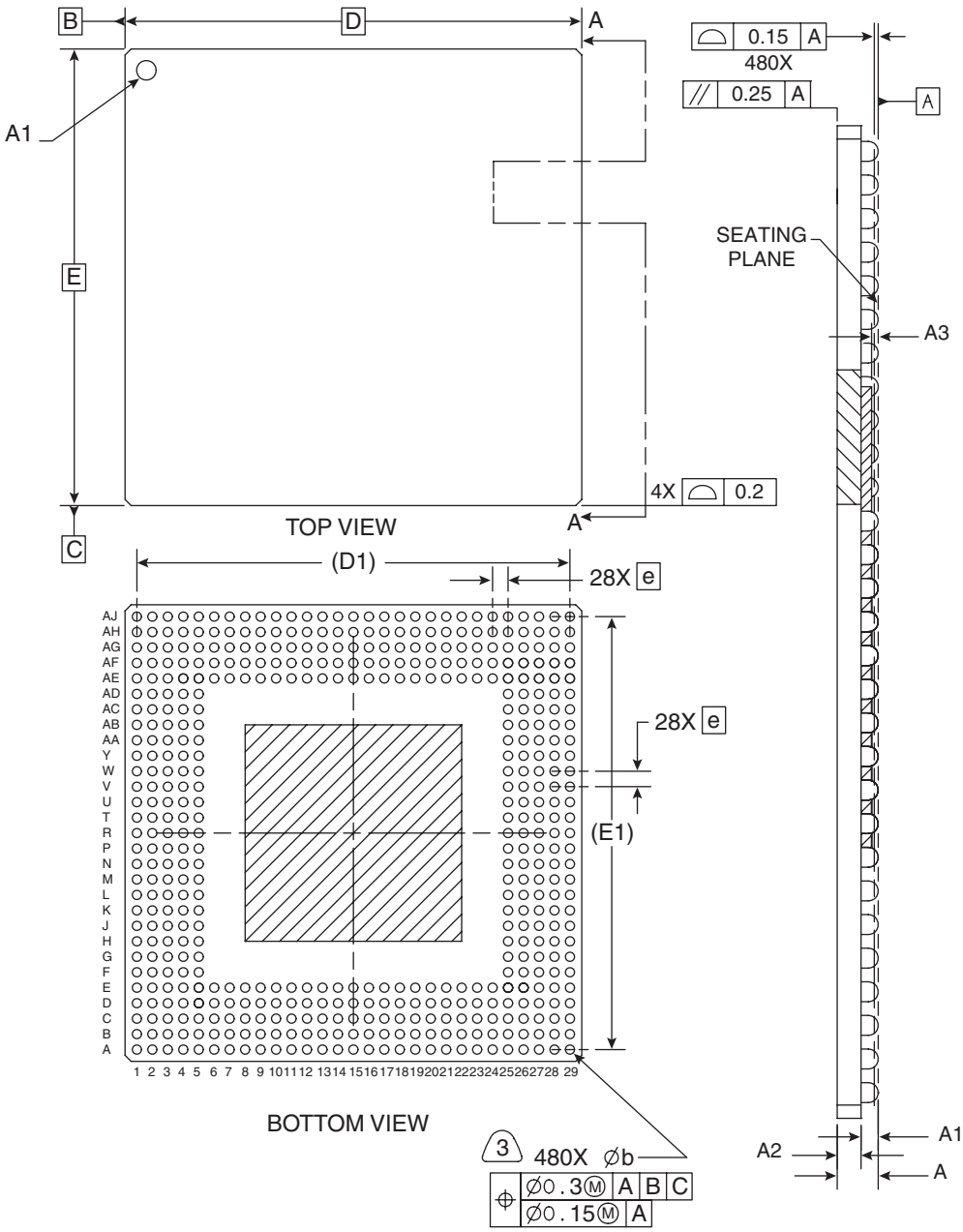
Table 9-1. Package Parameters

Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
TP	PC8280 PC8270	37.5 x 37.5	TBGA	480	1.27	1.55

9.2 Mechanical Dimensions

Figure 9-1 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

Figure 9-1. Mechanical Dimensions and Bottom Surface Nomenclature – 480 TBGA



Notes:
1. Dimensions and tolerancing per ASME Y14.5M-1994
2. Dimensions in millimeters
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

10. Ordering Information

Figure 10-1 provides an example of the e2v part numbering nomenclature for the PC8280. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

Figure 10-1. Ordering Information

xx 8280 y xx U nnn x

Product Code(1)	Part Identifier	Temperature Range(1)	Package(1)	Screening Level	CPU/CPM/Bus Speed(1)			Revision Level(1)
					CPU	CPM	BUS	
PC(X)(2)	8280	M: T_{case} = -55˚C T_J = +125˚C E: T_{case} = -45˚C T_J = +115˚C	TP = 480 TBGA	Upscreening	Q = 333 T = 400	L = 250	D = 83	A

xx 8270 y xx U nnn x

Product Code(1)	Part Identifier	Temperature Range(1)	Package(1)	Screening Level	CPU/CPM/Bus Speed(1)			Revision Level(1)
					CPU	CPM	BUS	
PC(X)(2)	8270	M: T_{case} = -55˚C T_J = +125˚C	TP = 480 TBGA	Upscreening	Q = 333 T = 400	L = 250	D = 83	A

Notes:
1. For availability of the different versions, contact your local e2v sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

11. Definitions

11.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

12. Document Revision History

Table 12-1 provides a revision history for this hardware specification.

Table 12-1. Document Revision History

Revision	Date	Substantive Change(s)
F	12/09	Preliminary specification changed to final. Modified Figure 10-1 “Ordering Information on page 58.
E	04/08	Table 8-1, “PC8280 and PC8270 Pinout List,” on page 44 update
D	02/07	Name change from Atmel to e2v Section 6. ”AC Electrical Characteristics” on page 15: removed deratings statement and clarified AC timing descriptions
C	05/06	Table 6-4, “AC Characteristics for SIU Inputs(1),” on page 20: Added text to clarify that Data Bus Parity is not supported at 66 MHz Table 6-4, “AC Characteristics for SIU Inputs(1),” on page 20: Added text to clarify that Data Bus ECC is supported at 66 MHz Table 6-4, “AC Characteristics for SIU Inputs(1),” on page 20: Added note to DP pins to show it is not supported at 66 MHz Table 6-5, “AC Characteristics for SIU Outputs(1),” on page 21: Added note to support 1 ns hold time
B	03/06	- Added the PC8270 characteristics - In Section 6.2 ”SIU AC Characteristics” on page 20, modified the note on CLKIN Jitter and duty cycle - Added Section 6.3 ”JTAG Timings” on page 24 - Modified Figure 9-1 on page 57 to display all text
A	11/05	Initial revision

Table of Contents

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