EV12AS200AZP
ANALOG TO DIGITAL CONVERTER
12-bit 1.5 GSps

Datasheet

Main features

- Single Core ADC Architecture with 12-bit Resolution Integrating a Selectable 1:1 and 1:2 DEMUX
- 1.5 GSps Guaranteed Conversion Rate
- 500 mVpp Analog Input Voltage (Differential Full Scale and AC Coupled)
- Very Low Latency (< 5 Clock Cycles)
- Noise Floor of –150 dBm/Hz (13-bit ENOB in 10 MHz Bandwidth)
- Analog and Clock Input Impedance: 100Ω Differential
- Power Dissipation: 3.0W (1:1 Mode) ; 3.1W (1:2 Mode)
- Differential Input Clock (AC Coupled)
- LVDS Differential Output Data and Data Ready on the 2 Output Ports
- Write only 3WSI-like Digital Interface (Gain, Offset, Sampling Delay adjust, DMUX Ratio Selection, test Modes)
- ADC Gain, Offset, Sampling Delay Adjustment for Interleaving Control
- Dynamic Test Mode (Alignment Sequence)
- Power Supplies: V_{CCA5} = 5.0V, V_{CCA3} = 3.3V, V_{CCO} = 2.5V or 3.3V
- Package: FpBGA196 15 x15 mm^2 196 balls

Performances

- 2.3 GHz Full Power Input Bandwidth (–3 dB)
- Single Tone Performance:
  SFDR = –66 dBFS; ENOB = 9.0-Bit; SNR = 57 dBFS at Fin = 997 MHz @ –1 dBFS, Fs = 1.5 GSps
  SFDR = –65 dBFS; ENOB = 8.8-Bit; SNR = 56 dBFS at Fin = 1600 MHz @ –1 dBFS, Fs = 1.5 GSps
  SFDR = –70 dBFS; ENOB = 9.3-Bit; SNR = 59 dBFS at Fin = 997 MHz @ –12 dBFS, Fs = 1.5 GSps
  SFDR = –70 dBFS; ENOB = 9.3-Bit; SNR = 58.5 dBFS at Fin = 1600 MHz @ –12 dBFS, Fs = 1.5 GSps
- Broadband Performance:
  NPR = 48 dB at –14 dBFS Optimum Loading Factor in 1st Nyquist

Applications

- Satellite Communications Systems
- Telecom Test Instrumentation
- Wireless Communications Systems
- Direct RF Down-conversion
- Automatic Test Equipment
- Direct L-Band RF Down Conversion
- Radar Systems
- High Resolution Oscilloscopes

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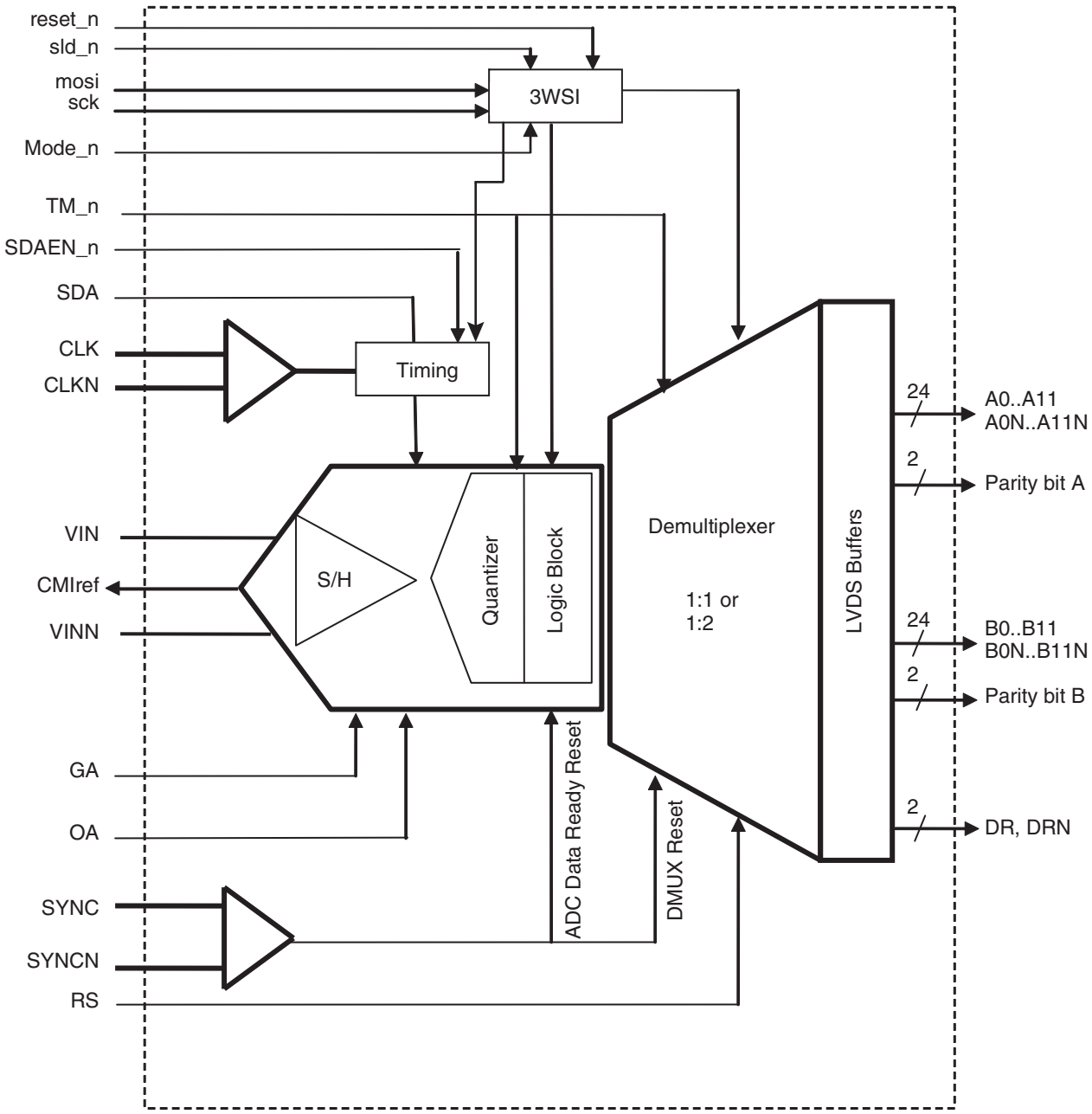
1. General Description

1.1 Block Diagram

Figure 1-1. ADC with Integrated DEMUX Block Diagram



1.2 Description

The EV12AS200A is a 12-bit 1.5 GSps ADC (Analog to Digital Converter) based on a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100Ω differential output buffers. It integrates a three Wire Serial Interface (3WSI) circuit (write only), which can be activated or desactivated (via Mode signal). Main functions accessed via the 3WSI can be accessed by hardware also (OA, GA, SDA, SDAEN_n, TM_n, RS pins).

The EV12AS200A works in fully differential mode from analog inputs through digital outputs.
It operates in the first Nyquist zone up to L-Band.

DEMUX Ratio (1:1 or 1:2) can be selected with the pin RS or via the 3WSI when activated.
DEMUX outputs are synchronous on each port.

A differential Data Ready output is available to indicate when the outputs are valid. The Data Ready (DR, DRN) is common to the 2 ports.

In order to ease the synchronization of multiple ADCs, the TRIGGER function could be used.

A power up reset ensures that the first digitized data corresponds to the first acquisition. An external differential LVDS Reset (SYNC, SYNCN) can also be used. The RES function accessible by 3WSI allows changing the active edge of the RESET signal.

The gain control pin GA and offset control OA are provided to adjust the ADC gain and offset transfer function. These functions can also be accessed via the 3WSI.

A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requiring the interleaving of multiple ADCs for example.

The junction temperature of the device could be monitored through a diode.

For debug and testability, the following functions are provided:

- A static test mode, used to test either V_{OL} or V_{OH} at the ADC outputs (all bits at "0" level or "1" level respectively) - these modes are accessed only via the 3WSI when activated;
- A dynamic built-In Test (alignment pattern with period of 16), accessed by hardware (TM_n signal) or via 3WSI when activated.

The circuit could be supplied either with 3 different power supplies voltages (V_{CC5} = 5.0V, V_{CC3} = 3.3V and V_{CCO} = 2.5V) to optimize the power consumption, or 2 different power supplies (V_{CCA5} = 5.0V, V_{CC3} = V_{CCO} = 3.3V) to use only 2 rails.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum ratings

Parameter	Symbol	Comments	Value	Unit
V_{CC5} supply voltage	V_{CC5}		GND to 6V	V
V_{CC3} supply voltage	V_{CC3}		GND to 4V	V
V_{CCO} supply voltage	V_{CCO}		GND to 4V	V
Analog input voltages	V_{IN} or V_{INN}		2V to 4V	V
Maximum difference between V_{IN} and V_{INN}	$\lvert V_{IN} - V_{INN} \rvert$		4Vpp<=> +13 dBm in 100Ω	Vpp
Maximum difference between V_{CLK} and V_{CLKN} (AC coupled)	$\lvert V_{CLK} - V_{CLKN} \rvert$		3.8Vpp<=> +12.5 dBm in 100Ω	Vpp
SYNC input voltage (AC coupled)	$\lvert V_{SYNC} - V_{SYNCN} \rvert$		3.8Vpp<=> +12.5 dBm in 100Ω	Vpp
Analog input settings	V_A	OA, GA, SDA	–0.3 to V_{CC3} + 0.3	V
Control inputs	V_D	SDAEN_n, TM_n, DEC_n, RS, reset_n, mosi, sld_n, sck, mode_n	–0.3 to V_{CC3} + 0.3	V
Junction Temperature	$T_{Junction}$		170	°C
ESD Immunity HBM Model			Class 1A	
Moisture sensitivity level			MSL3	

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
2. Maximum ratings enable active inputs with ADC powered off.
3. Maximum ratings enable floating inputs with ADC powered on.

2.2 Recommended Conditions of Use

Table 2-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Power supplies[1][2]	V_{CC5}		5.0	V
	V_{CC3}		3.3	V
	V_{CC0}		2.5	V
Differential analog input voltage (Full Scale)	$V_{IN} - V_{INN}$	100Ω differential	500	mVpp
Clock input power level (Ground common mode)	P_{CLK} P_{CLKN}	100Ω differential input	7	dBm
Operating Temperature Range	T_{case} $T_{junction}$	Commercial “C” grade Industrial “V” grade	Tc > 0 < Tj < 90 Tc > –40 < Tj < 110	°C
Storage Temperature	Tstg		–65 to 150	°C

Note: 1. No specific power supplies sequencing is required; however to benefit from the internal reset at power up, V_{CC3} should be applied before V_{CC5}

2. V_{CCO} could be merged to V_{CC3} to use the device using only 2 power supplies.

2.3 Electrical Characteristics

Unless otherwise stated, values here below are typical values for typical conditions of operation (Troom, typical power supply).

Table 2-3. Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
ADC RESOLUTION			12		bit	
POWER REQUIREMENTS						
Power Supply voltage						
- Analogue	VCC5	4.75	5.0	5.25	V	1
- Analogue Core and Digital	VCC3	3.15	3.3	3.45	V	1
- Output buffers (2.5V configuration)	VCCO	2.4	2.5	2.6	V	1
- Output buffers (3V configuration)	VCCO	3.15	3.3	3.45	V	1
Power Supply current in 1:1 DEMUX						
- Analogue	I_VCC5		170	190	mA	1
- Analogue Core and Digital	I_VCC3		535	600	mA	1
- Output buffers	I_VCCO		50	70	mA	1
Power Supply current in 1:2 DEMUX Ratio						
- Analogue	I_VCC5		170	190	mA	1
- Analogue Core and Digital	I_VCC3		540	600	mA	1
- Output buffers	I_VCCO		90	110	mA	1
Power dissipation DMUX1:1						
- 1:1 Ratio with standard LVDS output swing, 750 Msps output rate **(Vcco = 2.5V)**	P_D		2.75	3.0		1
- 1:1 Ratio with standard LVDS output swing, 750 Msps output rate **(Vcco = 3.3V)**	P_D		2.9	3.15		4
Power dissipation DMUX1:2					W	
- 1:2 Ratio with standard LVDS output swing, 1500 Msps output rate (Vcco = 2.5V)	P_D		2.85	3.10		1
- 1:2 Ratio with standard LVDS output swing, 1500 Msps output rate (Vcco = 3.3V)	P_D		3.0	3.25		1

Table 2-3. Electrical characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
LVDS Data and Data Ready Outputs						
Logic compatibility			LVDS differential			
Output Common Mode [1]	V_{OCM}	1.125	1.25	1.375	V	1
Differential output [1]	V_{ODIFF}	250	350	450	mVpp	1
Output level “High” [2]	V_{OH}	1.25	–	–	V	1
Output level “Low” [2]	V_{OL}	–	–	1.25	V	1
Output current level [2]	I_O	–	–	100	µA	
Output data format			Binary			
ANALOG INPUT						
Input type			AC coupled			
Analogue input Common mode (for DC coupled input) [5]			3.0			
Full scale input voltage range (differential mode) [6]	V_{IN} V_{INN}	–125 –125		+125 +125	mVp mVp	
Full scale analog input power level	P_{IN}		–5		dBm	
Analog input capacitance (die only)	C_{IN}		0.3		pF	
Input leakage current (V_{IN} = V_{INN} = 0V)	I_{IN}		50		µA	
Analog Input resistance (Differential)	R_{IN}	90	100	110	Ω	
CLOCK INPUT (CLK, CLKN)						
Input type			DC or AC coupled			
Clock Input Common Mode (for DC coupled clock)	V_{ICM}		2.65		V	
Clock Input power level (low phase noise sinewave input) 100Ω differential	P_{CLK}	0	4	10	dBm	
Clock input swing (differential voltage) on each clock input	V_{CLK} V_{CLKN}	±447	±708	2800	mVp	
Clock input capacitance (die only)	C_{CLK}		0.3		pF	
Clock Input resistance (Differential)	R_{CLK}		100		Ω	
SYNC, SYNCN						
Logic compatibility			LVDS			
Input Common Mode	V_{ICM}	1.125	1.25	1.375	V	
Differential input	V_{IDIFF}	250	350	450	mVp	
Input level “High”	V_{IH}			1.8	V	
Input level “Low”	V_{IL}	0.7			V	

Table 2-3. Electrical characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
DIGITAL INPUTS (RS, DEC_n, SDAEN_n, TM_n)						
Logic low Resistor to ground Voltage level Input current	 R_{IL} V_{IL} I_{IL}	 0	 	 10 0.5 450	 Ω V µA	
Logic high Resistor to ground Voltage level Input current	 R_{IH} V_{IH} I_{IH}	 10 2.0 	 	 100 150	 KΩ V µA	
OFFSET, GAIN , SAMPLING DELAY & CLOCK ADJUST SETTINGS (OA, GA, SDA)						
Min voltage for minimum Gain, Offset or SDA	Analog_min	$2*V_{cc3}/3 - 0.5$			V	
Max voltage for maximum Gain, Offset or SDA	Analog_max			$2*V_{cc3}/3 + 0.5$	V	
Input current for min setting	I_{min}			200	µA	
Input current for nominal setting	I_{nom}			50	µA	
Input current for max setting	I_{max}			200	µA	
3WSI (sclk, sld_n, mosi, reset_n, mode_n) INPUTS						
Logic compatibility		3.3V CMOS				
Low Level input voltage	V_{IL}	0		1	V	
High Level input voltage	V_{IH}	2.3		V_{cc3}	V	
Low Level input current	I_{IL}		100		µA	
High Level input current	I_{IH}		100		µA	
DC ACCURACY						
Differential Non Linearity (for information only)	$\lvert DNL \rvert$			2	LSB	1
Peak positive Integral Non Linearity (for information only)(7)	INL+		5		LSB	1
Peak negative Integral Non Linearity(7)	INL-		–5		LSB	1
Gain central value (3)	ADC_{GAIN}	0.8	1.0	1.2		1
Gain error drift versus temperature (over 15°C)				0.15	dB	4
Initial ADC offset (4)	ADC_{OFFSET}	1948	2048	2148	LSB	1

Notes:
1. Assuming 100Ω termination ASIC load
2. V_{OH} min and V_{OL} max can never be 1.25V at the same time when V_{ODIFF}min.
3. The ADC Gain center value can be tuned to 1.0 using Gain adjust function. Estimated at Fs = 1 GHz, Fin = 400 MHz
4. The ADC offset can be tuned to mid code 2048 using Offset adjust function.
5. For DC coupling application, the common mode value to apply is available as reference on the CMIREF pin.
6. Minimum input level validated is –12 dBFS.
7. INL is measured at –1dBFS

2.4 Dynamic Performance

Unless otherwise stated, values here below are typical values (typical conditions of operations) assuming an external clock jitter of 75 fs rms (corresponds to e2v testbench value). ADC internal clock jitter is 75 fs rms.

Table 2-4. Dynamic Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
AC Analog Inputs						
Full power Input Bandwidth (Fclk = 1.5 GSps)	FPBW		2.3		GHz	
Gain Flatness (from 10 to 170 MHz) (Fclk = 1.5 GSps)				0.5	dB	
Gain Flatness (from 170 to 1500 MHz) (Fclk = 1.5 GSps)				1	dB	
Gain Flatness (from 1500 to 1800 MHz) (Fclk = 1.5 GSps)				1.5	dB	
–1 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1 GSps Fin = 997 MHz			54.5			1
FS = 1.5 GSps Fin = 740 MHz	SINAD		54.5		dBFS	4
FS = 1.5 GSps Fin = 997 MHz			56			1
FS = 1.5 GSps Fin = 1600 MHz			54.5			1
Effective Number of Bits						
FS = 1 GSps Fin = 997 MHz			8.8			1
FS = 1.5 GSps Fin = 740 MHz	ENOB		8.8		Bit FS	4
FS = 1.5 GSps Fin = 997 MHz		8.4	9.0			1
FS = 1.5 GSps Fin = 1600 MHz		8.2	8.8			1
Signal to Noise Ratio						
FS = 1 GSps Fin = 997 MHz			57.0			1
FS = 1.5 GSps Fin = 740 MHz	SNR		56.5		dBFS	4
FS = 1.5 GSps Fin = 997 MHz		55.5	57.0			1
FS = 1.5 GSps Fin = 1600 MHz		54.5	56.0			1
Total Harmonic Distortion (25 harmonics)						
FS = 1 GSps Fin = 997 MHz			60			1
FS = 1.5 GSps Fin = 740 MHz	THD		60		dBFS	4
FS = 1.5 GSps Fin = 997 MHz			61			1
FS = 1.5 GSps Fin = 1600 MHz			60			1
Spurious Free Dynamic Range						
FS = 1 GSps Fin = 997 MHz			62			1
FS = 1.5 GSps Fin = 740 MHz	SFDR		63		dBFS	4
FS = 1.5 GSps Fin = 997 MHz		54	66			1
FS = 1.5 GSps Fin = 1600 MHz		53	65			1

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
–3 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1 GSps Fin = 997 MHz	SINAD		55.5		dBFS	4
FS = 1.5 GSps Fin = 997 MHz			56			4
FS = 1.5 GSps Fin = 1600 MHz			54.5			1
Effective Number of Bits						
FS = 1 GSps Fin = 997 MHz	ENOB		8.9		Bit FS	4
FS = 1.5 GSps Fin = 997 MHz			9.0			4
FS = 1.5 GSps Fin = 1600 MHz		8.2	8.8			1
Signal to Noise Ratio						
FFS = 1 GSps Fin = 997 MHz	SNR		57.5		dBFS	4
FS = 1.5 GSps Fin = 997 MHz			57.5			4
FS = 1.5 GSps Fin = 1600 MHz		55.5	57			1
Total Harmonic Distortion (25 harmonics)						
FS = 1 GSps Fin = 997 MHz	THD		59		dBFS	4
FS = 1.5 GSps Fin = 997 MHz			61			4
FS = 1.5 GSps Fin = 1600 MHz			58			1
Spurious Free Dynamic Range						
FS = 1 GSps Fin = 997 MHz	SFDR		62		dBFS	4
FS = 1.5 GSps Fin = 997 MHz			66			4
FS = 1.5 GSps Fin = 1600 MHz		50	62			1
–8 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1 GSps Fin = 997 MHz			57.0			1
FS = 1.5 GSps Fin = 740 MHz	SINAD		56.5		dBFS	4
FS = 1.5 GSps Fin = 1000 MHz			57.0			1
FS = 1.5 GSps Fin = 1600 MHz			57.0			1
Effective Number of Bits						
FS = 1 GSps Fin = 997 MHz			9.2			1
FS = 1.5 GSps Fin = 740 MHz	ENOB		9.1		Bit FS	4
FS = 1.5 GSps Fin = 1000 MHz			9.2			1
FS = 1.5 GSps Fin = 1600 MHz		8.6	9.2			1
Signal to Noise Ratio						
FS = 1 GSps Fin = 997 MHz			59			1
FS = 1.5 GSps Fin = 740 MHz	SNR		59		dBFS	4
FS = 1.5 GSps Fin = 1000 MHz			58.5			1
FS = 1.5 GSps Fin = 1600 MHz		56.5	58.0			1
Total Harmonic Distortion (25 harmonics)						
FS = 1 GSps Fin = 997 MHz			62			1
FS = 1.5 GSps Fin = 740 MHz	THD		61.5		dBFS	4
FS = 1.5 GSps Fin = 1000 MHz			62			1
FS = 1.5 GSps Fin = 1600 MHz			62			1

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Spurious Free Dynamic Range						
FS = 1 GSps Fin = 997 MHz	SFDR		69		dBFS	1
FS = 1.5 GSps Fin = 740 MHz			65			4
FS = 1.5 GSps Fin = 1000 MHz			67			1
FS = 1.5 GSps Fin = 1600 MHz		55	68			1
–12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 75 fs rms max						
Signal to Noise And Distortion Ratio						
FS = 1 GSps Fin = 997 MHz	SINAD		57.7		dBFS	1
FS = 1.5 GSps Fin = 997 MHz			57.7			1
FS = 1.5 GSps Fin = 1600 MHz			57.7			1
Effective Number of Bits						
FS = 1 GSps Fin = 997 MHz	ENOB		9.3		Bit FS	1
FS = 1.5 GSps Fin = 997 MHz			9.3			1
FS = 1.5 GSps Fin = 1600 MHz			9.3			1
Signal to Noise Ratio						
FS = 1 GSps Fin = 997 MHz	SNR		59		dBFS	1
FS = 1.5 GSps Fin = 997 MHz			59			1
FS = 1.5 GSps Fin = 1600 MHz			58.5			1
Total Harmonic Distortion (25 harmonics)						
FS = 1 GSps Fin = 997 MHz	THD		63		dBFS	1
FS = 1.5 GSps Fin = 997 MHz			63			1
FS = 1.5 GSps Fin = 1600 MHz			63			1
Spurious Free Dynamic Range						
FS = 1 GSps Fin = 997 MHz	SFDR		70		dBFS	1
FS = 1.5 GSps Fin = 997 MHz			70			1
FS = 1.5 GSps Fin = 1600 MHz			70			1
Broadband performance						
Noise Power Ratio Notch centered on 300 MHz, Notch width 12.5 MHz on 10 MHz &600 MHz band 1.5 GSps at optimum factor loading –14 dBFS	NPR		47		dB	4
IMD3 2Fin1- Fin2, 2Fin2-Fin1, unfilterable Fin1 = 700 MHz & Fin2 = 710 MHz Amplitude In = –7 dBFs on each tone	IMD3		–65		dBFS	4

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
IMD3 2Fin1- Fin2, 2Fin2-Fin1, unfilterable Fin1 = 1450 MHz & Fin2 = 1460 MHz Amplitude In = –7 dBFs on each tone	IMD3		–65		dBFS	4
IMD3 2Fin1- Fin2, 2Fin2-Fin1, unfilterable Fin1 = 700 MHz & Fin2 = 710 MHz Amplitude In = –30 dBFs on each tone	IMD3		–82		dBFS	4
IMD3 2Fin1- Fin2, 2Fin2-Fin1, unfilterable Fin1 = 1450 MHz & Fin2 = 1460 MHz Amplitude In = –30 dBFs on each tone	IMD3		–81		dBFS	4

2.5 Timing Characteristics and Switching Performances

Unless otherwise stated, values here below are typical values (typical conditions of operations) assuming an external clock jitter of 75 fs rms.

Table 2-5. Timing characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
SWITCHING PERFORMANCE AND CHARACTERISTICS						
Clock frequency (1) 1:1 DEMUX Ratio 1:2 DEMUX Ratio		 300 300		 1000 1500	MHz	
Maximum Output Rate per port (Data and Data Ready) 1:1 DEMUX Ratio 1:2 DEMUX Ratio				 1000 750	MSps	
Maximum Output Frequency per port (Data and Data Ready) (3) 1:1 DEMUX Ratio 1:2 DEMUX Ratio				 500 375	MHz	
BER				10^{-12}	Error/sample	
TIMING						
Overvoltage recovery time	ORT			300	ps	4
ADC step response (10% to 90%)			120		ps	4
Overshoot			4		%	4
Ringback			–2		%	4
Clock duty cycle		45	50	55	%	4
Minimum clock pulse width (high)	T_{C1}, T_{C2}	300	330	1500	ps	4
Aperture delay (1) (SDA off)	T_A		50		ps	4

Table 2-5. Timing characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Internal clock Jitter (SDA off)			75		fsrms	
Eye diagram opening @Fs = 1.5 GSps demux 2			500		ps	4
Skew between data			70		ps	4
Output rise/fall time for DATA (20% to 80%) (3)	T_R/T_F	200	250	300	ps	4
Output rise/fall time for DATA READY (20% to 80%) (2)	T_R/T_F	200	250	300	ps	4
Data output delay (4)	T_{OD}	3	3.2	3.5	ns	4
Data Ready output delay (4)	T_{DR}	3	3.2	3.5	ns	4
	$\lvert T_{OD}–T_{DR}\rvert$		0	100	ps	4
Output Data to Data Ready propagation delay (5) 1:1 DEMUX Ratio 1:2 DEMUX Ratio	T_{D1}		 500 660		ps	4
Data Ready to Output Data propagation delay (5) 1:1 DEMUX Ratio 1:2 DEMUX Ratio	T_{D2}		 500 740		ps	
Output Data Pipeline delay 1:1 DEMUX Ratio 1:2 DEMUX Ratio	T_{PD}		 3 3.5		Clock cycle	
Data Ready Pipeline delay 1:1 DEMUX Ratio 1:2 DEMUX Ratio	T_{PDR}		 3.5 4.5		Clock cycle	
SYNC to Data Ready 1:1 DEMUX Ratio 1:2 DEMUX Ratio	T_{RDR}		 2 2		ns	
SYNC to Data Ready pipeline delay 1:1 DEMUX Ratio 1:2 DEMUX Ratio			 3 5		Clock cycle	
SYNC min pulse duration		1			Clock cycle	
SYNC Signal valid timing (See Figure 2-5)	T_1 T_2		–165 –160		ps	

Notes:
1. See Definition Of Terms.
2. Data Ready outputs are active on both rising and falling edges (DR/2 mode)
3. 50Ω // C_{LOAD} = 2 pF termination (for each single-ended output). Termination load parasitic capacitance derating value: 50 ps/pF (ECL).
4. T_{OD} and T_{DR} propagation times are defined at package input/outputs. They are given for reference only. T_{OD} & T_{DR} track each other over full temperature range. Typical $T_{OD} – T_{DR}$ = 0 and dataready is centered on the output data.
5. Values for T_{D1} and T_{D2} are given for a 1.5 GSps in DMUX 1:2 (respectively 1 GSps DMUX1:1) external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: $T_{D1} = T/2 +(\lvert T_{OD} – T_{DR}\rvert)$ and $T_{D2} = T/2 +(\lvert T_{OD} – T_{DR}\rvert)$, where T = clock period. This places the rising edge (True-False) of the differential Data Ready signal in the middle of the Output Data valid window. This gives maximum setup and hold times for external data acquisition

2.6 Timing Diagrams

Figure 2-1. Principle of Operation, DMUX 1:1

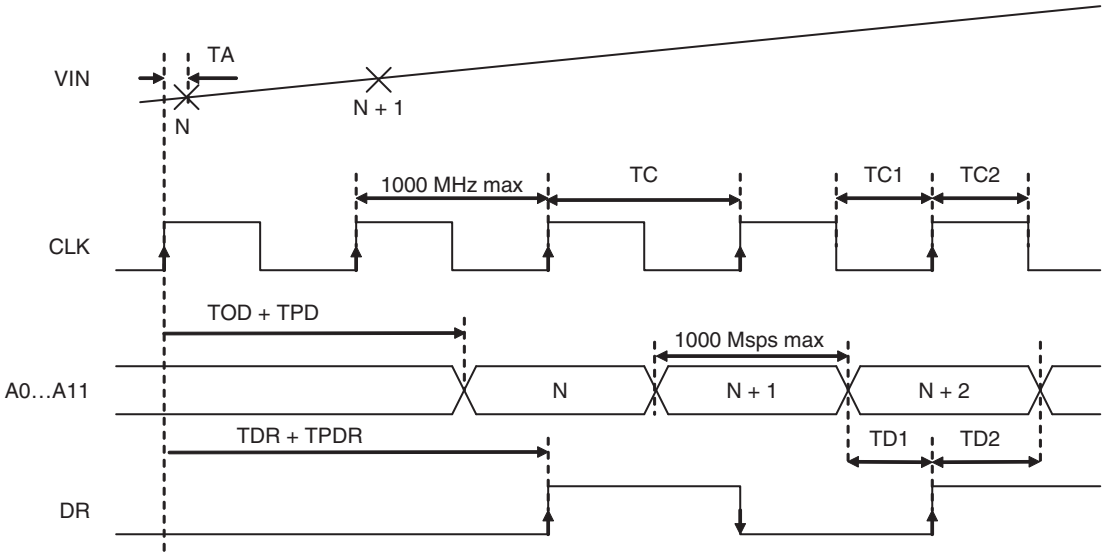


Figure 2-2. Principle of Operation, DMUX 1:2

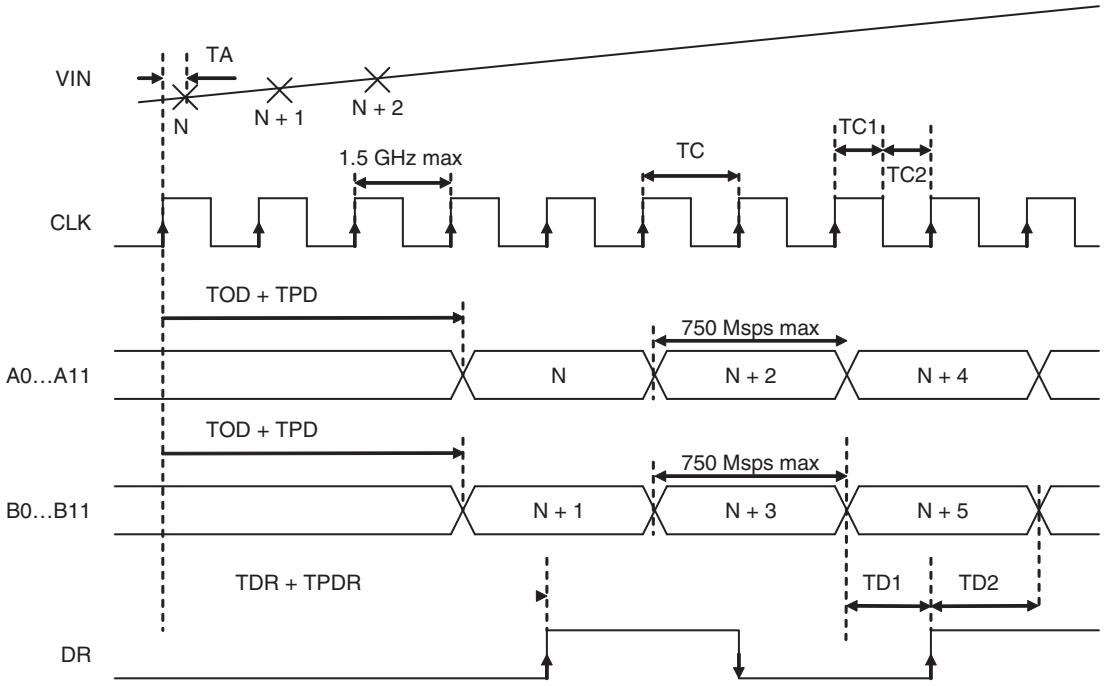
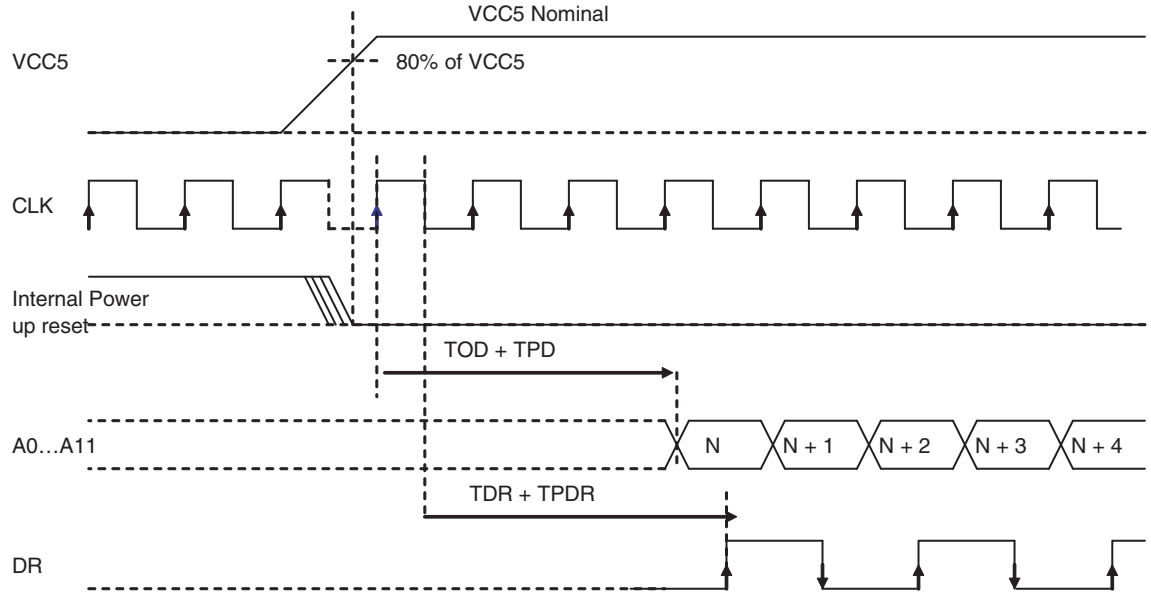


Figure 2-3. Power up Reset Timing Diagram (1:1 DMUX)



Note: V_{cc3} should be applied before V_{cc5}

Figure 2-4. SYNC Timing Diagram (1:2 DMUX & Reset Edge: Falling)

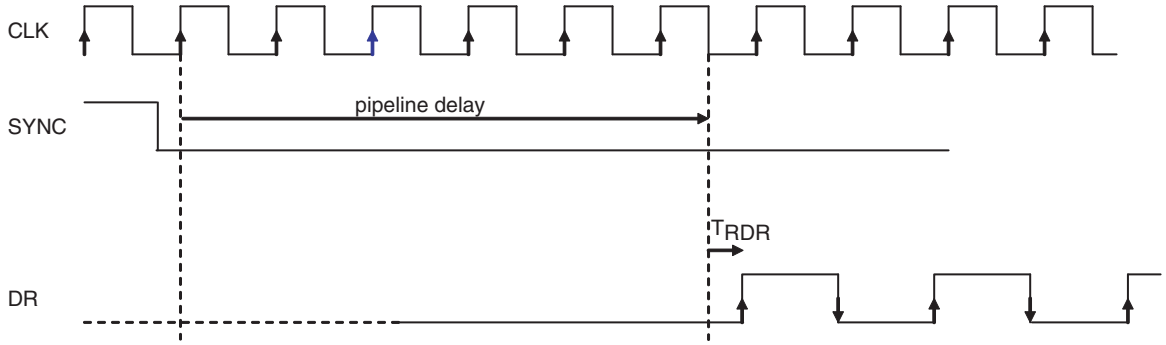
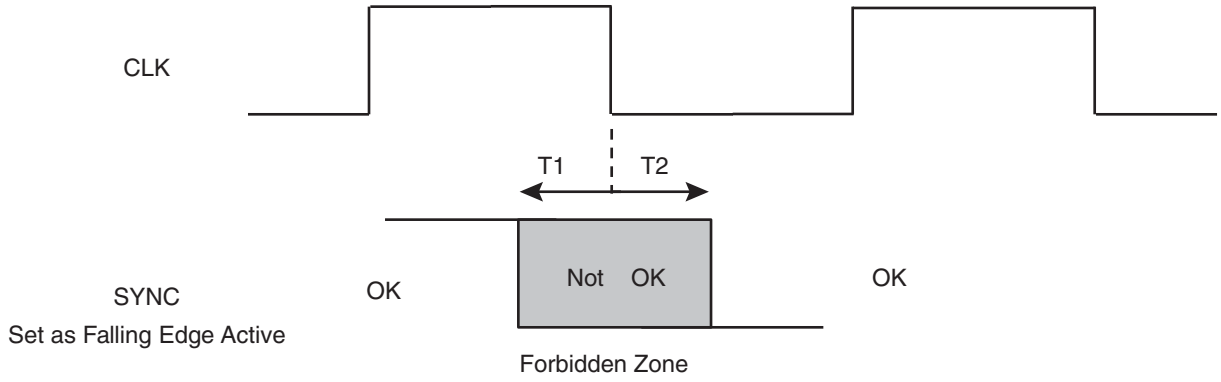


Figure 2-5. T1 & T2 Diagram



The SYNC signal should be timed so that it does not change in the forbidden zone described in the image above.

The SYNC signal is timed from the falling edge of the input clock.

2.7 Explanation of Test Levels

1	100% production tested at +25°C[1].
2	100% production tested at +25°C[1], and sample tested at specified temperatures.
3	Sample tested only at specified temperatures.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value guaranteed by design only.
6	100% production tested over specified temperature range (for D/T and Space Grade[2]).

Note: Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

Notes: 1. Unless otherwise specified.
2. If applicable, please refer to “Ordering Information”

2.8 Coding

Table 2-6. ADC Coding Table

		Digital output
Differential analog input	**Voltage level**	Binary MSB.....LSB
> + 250.06 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1
+ 250.06 mV + 249.94 mV	Top end of full scale + ½ LSB Top end of full scale – ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
+ 125.06 mV + 124.94 mV	3/4 full scale + ½ LSB 3/4 full scale – ½ LSB	1 1 1 1 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1
+ 0.06 mV – 0.06 mV	Mid scale + ½ LSB Mid scale – ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
– 124.94 mV – 124.06 mV	1/4 full scale – ½ LSB 1/4 full scale + ½ LSB	0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
– 249.94 mV – 250.06 mV	Bottom end of full scale – ½ LSB Bottom end of full scale + ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
< – 250.06 mV	< Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0

2.9 Definition of Terms

Table 2-7. Definition of Terms

Abbreviation	Term	Definition
(Fs max)	*Maximum Sampling Frequency*	Performances are warranted up to Fsmax unless specified.
(Fs min)	*Minimum Sampling frequency*	Performances are warranted for sampling frequency above Fsmin.
(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ±128 LSB from the correct code.
(FPBW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (– 1 dBFS).
(SSBW)	*Small Signal Input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –10 dB (– 10 dBFS).
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale (– 1 dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics.
(THD)	*Total harmonic distortion*	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (i.e, related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(ENOB)	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$ Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (V_{IN},V_{INN}) is sampled.
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(ORT)	*Overvoltage recovery time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
(TOD)	*Digital data Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TDR)	*Data ready output delay*	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data ready (zero crossing) with specified load.
(TPDR)	*Data ready pipeline delay*	Number of clock cycles between the sampling edge of an input data and the associated output data ready being made available, (not taking in account the TDR).

Table 2-7. Definition of Terms (Continued)

Abbreviation	Term	Definition
(TD1)	*Time delay from Data transition to Data Ready*	General expression is TD1 = TC1 + TDR – TOD with TC = TC1 + TC2 = 1 encoding clock period.
(TD2)	*Time delay from Data Ready to Data*	General expression is TD2 = TC2 + TDR – TOD with TC = TC1 + TC2 = 1 encoding clock period.
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	*Pipeline Delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TRDR)	*Data Ready reset delay*	Delay between the falling edge of the Data Ready output asynchronous Reset signal (SYNC) and the reset to digital zero transition of the Data Ready output signal (DR) excluding the pipeline delay.
(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (ie. 99% power transmitted and 1% reflected).
(T1, T2)	*Forbidden area bound*	T1 and T2 represent the lower and upper bound of forbidden aera for SYNC signal timing referenced to the clock signal. Figure 2-5.

3. Pin Description

3.1 Pin Mapping

Figure 3-1. Pin Mapping FpBGA (**Top View**)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	A8	A10N	A10	A11	A11N	NC DGND	DR	B11N	B11	B10	B10N	B8	DGND	A
B	NC DGND	NC DGND	A8N	NC DGND	A9	NC DGND	NC DGND	DRN	NC (DGND)	B9	NC DGND	B8N	NC DGND	NC DGND	B
C	A6N	NC DGND	NC DGND	NC DGND	A9N	NC DGND	DGND	DGND	NC (DGND)	B9N	NC DGND	NC DGND	NC DGND	B6N	C
D	A6	A7	A7N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	B7N	B7	B6	D
E	NC (DGND)	PCB_AN	PCB_A	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	PCB_B	PCB_BN	NC (DGND)	E
F	NC (DGND)	A5	A5N	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	B5N	B5	NC (DGND)	F
G	A4	A4N	NC (DGND)	NC (DGND)	DGND	AGND	AGND	AGND	AGND	DGND	NC (DGND)	NC (DGND)	B4N	B4	G
H	A3	A3N	NC (DGND)	NC (DGND)	DGND	AGND	AGND	AGND	AGND	DGND	NC (DGND)	NC (DGND)	B3N	B3	H
J	A2N	A0	A0N	VCC3	VCC3	AGND	AGND	AGND	AGND	VCC3	VCC3	B0N	B0	B2N	J
K	A2	NC (DGND)	NC (DGND)	DGND	DGND	AGND	VCC5	VCC5	AGND	DGND	DGND	NC DGND	NC DGND	B2	K
L	A1	NC (DGND)	NC (DGND)	DGND	RS	VCC5	VCC5	VCC5	VCC5	DGND	mosi	mode_n	NC DGND	B1	L
M	A1N	NC (DGND)	GA	OA	TM_n	VCC5	VCC5	AGND	AGND	SDA	SDAEN_n	reset_n	NC DGND	B1N	M
N	NC (DGND)	DIODEC	SYNCN	DGND	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	reserved	reserved	CMIREF	N
P	DGND	DIODEA	SYNC	DGND	CLK	AGND	AGND	AGND	VIN	VINN	AGND	sclk	sld_n	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

3.2 Pin Description Table

Table 3-1. Pin Description FpBGA196

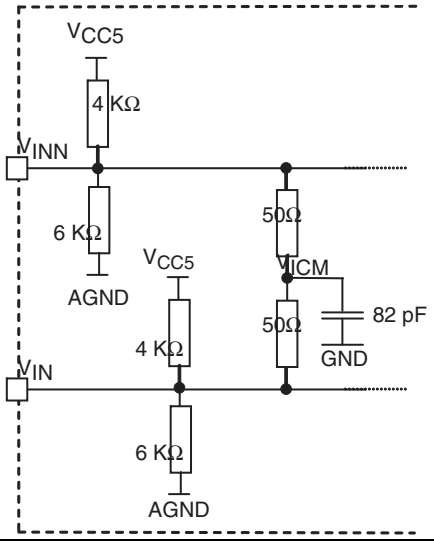
Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
POWER SUPPLIES				
V_{CC5}	K7;K8;L6;L7;L8;L9;M6;M7	5.0V analog supply (Front-end Track & Hold circuitry) Referenced to AGND	N/A	
V_{CC3}	J4;J5;J10;J11	3.3V power supply (ADC Core, Regeneration and Logic, DEMUX circuitry and Timing circuitry) Referenced to AGND	N/A	
V_{CCO}	F4;F5;D6;E6;D7;E7;D8;E8; D9;E9;F10;F11	2.5 or 3.3 V digital power supply (output buffers) Referenced to DGND	N/A	
DGND	A1;A14;C7;C8;D4;D5;D10; D11;E4;E5;E10;E11;G5; G10;H5;H10;K4;K5;K10; K11;L4;L10;N4;P1;P4P14	Digital Ground DGND should be separated from AGND on board (the two planes can be reunited via 0 ohm resistors)	N/A	
AGND	F6;F7;F8;F9;G6;G7;G8;G9; H6;H7;H8;H9;J6.J7;J8;J9; K6;K9;M8;M9;N6;N7;N8;N9; N10;N11;P6;P7;P8;P11	Analog Ground AGND should be separated from DGND on board (the two planes can be reunited via 0 ohm resistors)	N/A	
ANALOG INPUTS				
V_{IN} V_{INN}	P9 P10	Analog input (differential) with internal common mode at 3.1V It should be driven in AC coupling. Analog input is sampled and converted (10-bit) on each positive transition of the CLK input. Equivalent internal differential 100Ω input resistor.	I	

Table 3-1. Pin Description FpBGA196 (Continued)

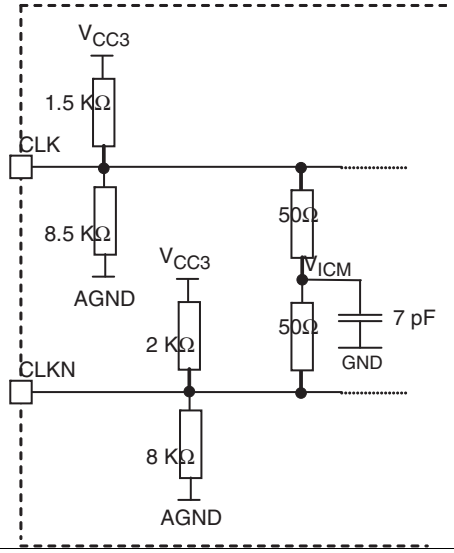
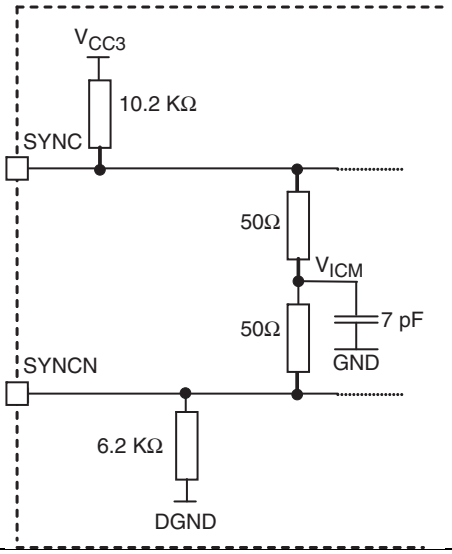
Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
CLOCK INPUTS				
CLK CLKN	P5 N5	Master sampling clock input (differential) with internal common mode. It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	
RESET INPUT				
SYNC SYNCN	P3 N3	Reset input (active low). It is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is Synchronous, it is LVDS compatible. It is active on an Edge (programmable using or falling).	I	

Table 3-1. Pin Description FpBGA196 (Continued)

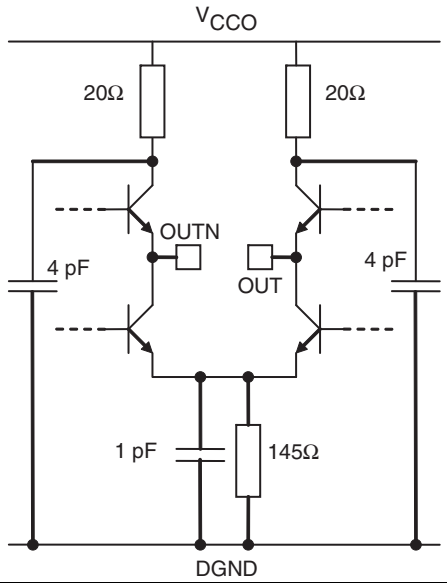
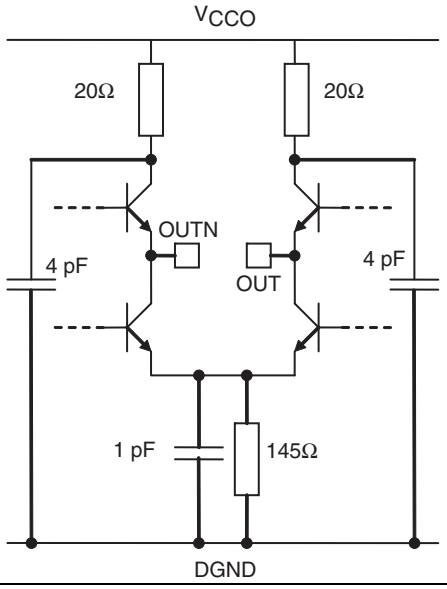
Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
DIGITAL OUTPUTS				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	J2;J3 L1;M1 K1;J1 H1;H2 G1;G2 F2;F3 D1;C1 D2;D3 A2;B3 B5;C5 A4;A3 A5;A6	In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0…11) Differential LVDS signal A0 is the LSB, A11 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	J13;J12 L14;M14 K14;J14 H14;H13 G14;G13 F13;F12 D14;C14 D13;D12 A13;B12 B10;C10 A11; A12 A10;A9	In-phase (Bi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0…11) Differential LVDS signal B0 is the LSB, B11 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 3-1. Pin Description FpBGA196 (Continued)

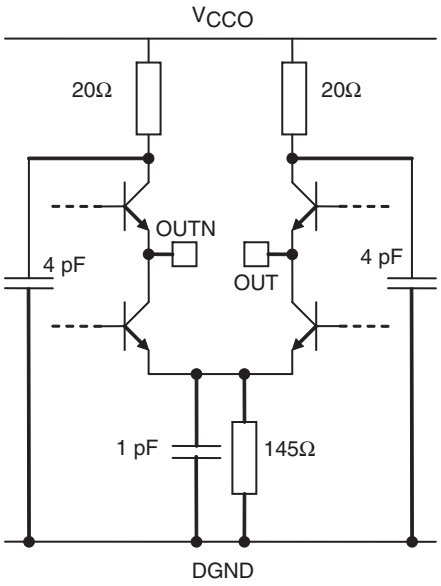
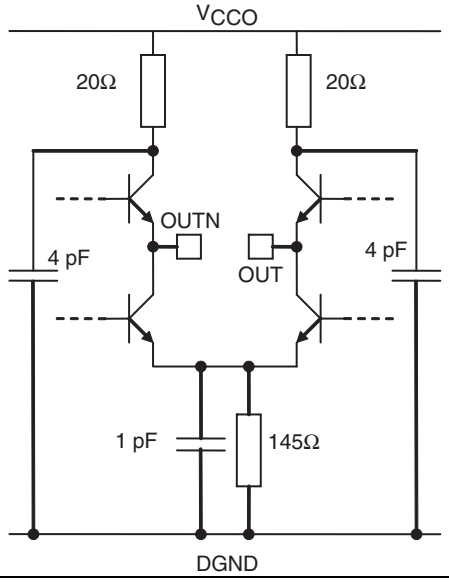
Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
PCB_A PCB_AN	E3; E2	Parity Check Bit port A	O	
PCB_B PCB_BN	E12 E13	Parity Check Bit port B	O	
DR DRN	A8 B8	In-phase (DR) and inverted phase (DRN) global data ready digital output clock Differential LVDS signal The differential digital output clock is used to latch the output data on rising and falling edge. The differential digital output clock rate is (CLK/2) divided by the DMUX ratio (provided by RS0 and RS1 pins). This differential digital output clock should be terminated by 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 3-1. Pin Description FpBGA196 (Continued)

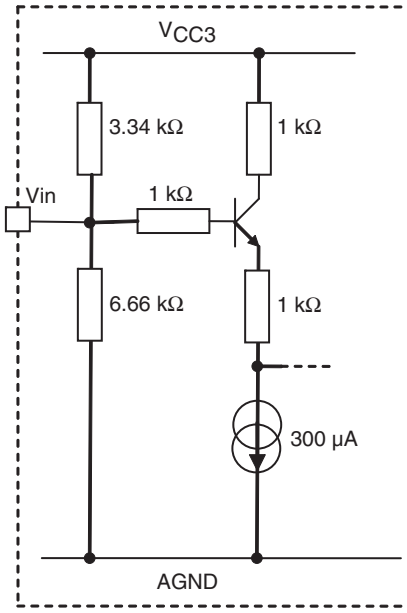
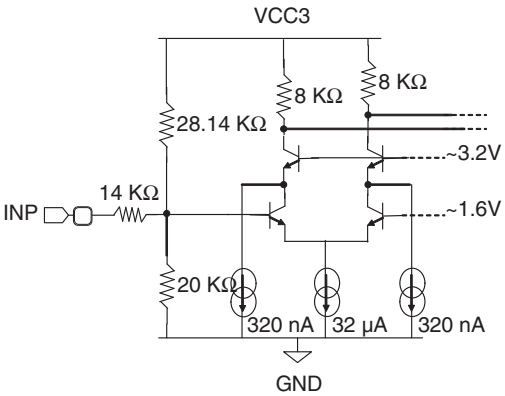
Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
ADDITIONAL FUNCTIONS				
reserved	N12, N13	Reserved / Do not connect	I	
TM_n	M5	Test Mode	I	
RS	L5	DEMUX Ratio Selection	I	
SDAEN_n	M11	Sampling delay adjust enable	I	
SDA	M10	Sampling delay adjust	I	 Variation on AP node: from 2/(VCC3/3) – 0.5 V to 2/(VCC3/3) + 0.5 V must be connected to 2.2V through a potential divider.
GA	M3	Gain Adjust	I	
OA	M4	Offset Adjust	i	
mode_n	L12	3WSI Enable (active Low) “1” : 3WSI not active “0” : 3WSI active	I	
sclk	P12	3WSI write only clock. Serial data on mosi signal is shifted into 3WSI synchronously to this signal on positive transition of sck.	I	
mosi	L11	3WSI write only serial data input. Shifted into 3WSI while sld_n is active (low).	I	
sld_n	P13	3WSI write only Serial load enable input. When this signal is active (low), sck is used to clock data present on mosi signal.	I	
reset_n	M12	3WSI write only asynchronous reset input signal. This signal allows to reset internal values of the 3WSI to their default value.	I	
CMIRef	N14	Input common mode Can be used to supply common mode voltage to DC coupled amplifier	O	

Table 3-1. Pin Description FpBGA196 (Continued)

Signal Name	Pin number	Function	Dir.	Equivalent Simplified Schematics
DIODEA	P2	Die Junction temperature monitoring (anode)		
DIODEC	N2	Die Junction temperature monitoring (cathode)		
NC(DGND)	A7;B1;B2;B4;B6;B7;B9;B11;B13;B14;C2;C3;C4;C6;C9;C11;C12;C13;E1;F1;E14;F14;G3;G4;G11;G12;H3;H4 H11;H12;K2;K3;K12;K13;L2 L3;L13;M2;M13;N1	Non connected pins, to be connected on board to DGND		

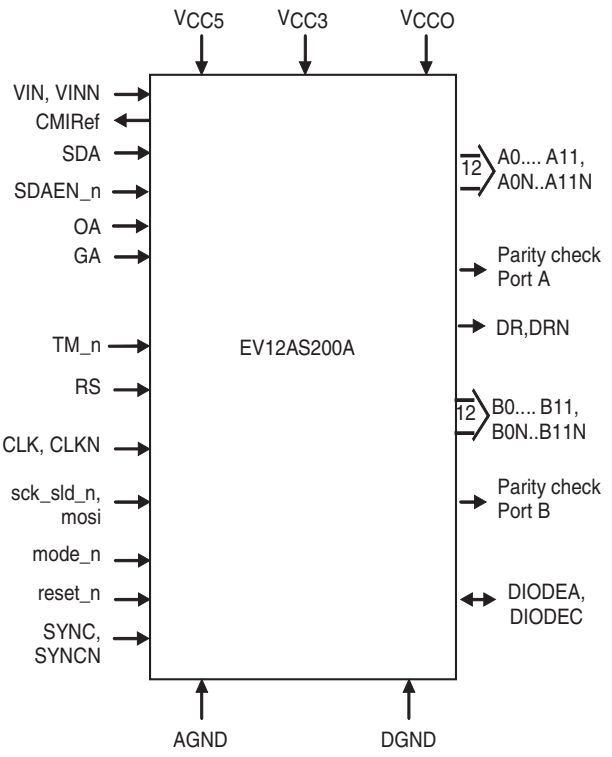
4. Functional Description

4.1 List of Functions

- External synchronous LVDS reset (SYNC, SYNCN)
- Write only 3WSI (SPI like) digital interface
- ADC Gain adjust
- ADC Offset adjust
- Sampling delay adjust
- Dynamic Test Mode (alignment sequence)
- Data Ready common to the 2 output ports
- RES function
- TRIGGER function
- Decimation mode
- Die Junction monitoring

Table 4-1. Function Descriptions

Name	Function
V_{CC5}	5.0V Power supply
V_{CC3}	3.3V Power supply
V_{CC0}	2.5V Power supply
GND	Ground
GNDO	Digital Ground for outputs
VIN,VINN	Differential Analog Input
CLK,CLKN	Differential Clock Input
[A0:A11] [A0N:A11N]	Differential Output Data on port A
PCB_A, PCB_AN	Parity check bit port A
[B0:B11] [B0N:B11N]	Differential Output Data on port B
PCB_B, PCB_BN	Parity check bit port B
DR,DRN	Global Differential Data Ready
RS	DEMUX Ratio select
SYNC, SYNCN	External reset
TM_n	Test Mode Enable
SDA	Sampling Delay Adjust input
SDAEN_n	Sampling Delay Adjust Enable
GA	Gain Adjust input.
OA	Offset adjust input
DIODEA, DIODEC	Diode for die junction temperature monitoring
Sck, sld_n, reset_n, mosi, mode_n	3WSI write only pins
CMIRef	Input common mode reference voltage



The different functions could be enabled by external dedicated command pin and/or 3WSI interface according the table below.

When the 3WSI is activated and used (mode_n active), hardware commands are disabled.

When the hardware command is used (mode_n disabled), value of the register could not be modified and are set to default.

It is however recommended to use the command via the 3WSI interface that offer more flexibility.

Table 4-2. ADC Mode Settings – Summary by External or by the 3WSI

Function	3WSI	External command pin	Description	Standard operation use
TM_n	yes	yes	Test mode ON/OFF (Active LOW)	forbidden
TESTTYPE	yes (2 bit)	no	Test Type: dynamic or static pattern (static pattern: 3WSI only)	forbidden
SDAEN_n	yes	yes (fine only)	Sampling Delay Adjust ON/OFF (Active LOW)	allowed
SDA_fine	yes (10 bit)	yes (2,2V ±0,5V)	SDA Fine tuning (0 -> 1023 for 3WSI or 1,7V -> 2,7V external)	allowed
SDA_coarse	yes (2 bit)	no	SDA Coarse tuning (3WSI Only): "00" -> 0 ps, "01"-> 30 ps, "10"-> 60 ps, "11"-> 90 ps	allowed
RS	yes	yes	Demux Ratio Select: "1": 1:2 mode, "0": 1:1 mode	allowed
GAIN ADJUST	yes (10 bit)	yes (2,2V ±0,5V)	Gain Adjust (0-> 1023 for 3WSI or 1,7V -> 2,7V external)	allowed
OFFSET ADJUST	yes (10 bit)	yes (2,2V ±0,5V)	Offset Adjust (0-> 1023 for 3WSI or 1,7V -> 2,7V external)	allowed
mode_n	no	yes	3WSI ON/OFF (Active LOW, all other settings are external if OFF)	allowed
TRIG_SEL_n	yes	no	SYNC Behavior: "1": Trigger Mode, "0": Syncronization Mode	allowed
RES	yes	no	SYNC Active Edge ("1": falling, "0": rising)	allowed
DEC_n	yes	yes	Decimation mode per 8	forbidden

Forbidden functions are described only for debug purpose and could not be used for standard operation.

4.2 External Reset (SYNC, SYNCN)

An external LVDS reset (SYNC, SYNCN) is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is LVDS compatible. It is active on an Edge (programmable rising or falling).

This signal is asynchronous but is relatched internally to the sampling clock.

To avoid metastability issues on internal SYNC signals, it is mandatory to respect SYNC T1 and T2 time, as any transition of the SYNC signal is forbidden between T1 and T2 time. Please refer to Figure 2-4 and Figure 2-5.

4.3 Mode (mode_n) Function

It is possible to activate the digital interface via the mode_n signal, external command.

The coding table for the mode is given in the table below

Table 4-3. Mode Coding

Function	Logic Level	Electrical Level	Description
Mode_n	0	10Ω to ground	3WSI Digital interface active
	1	10 KΩ to ground	3WSI Digital interface inactive (default mode)
		N/C	

Description of the 3WSI interface are described in Section 4.13 ”ADC 3WSI Description (ADC Controls)” on page 36.

4.4 DEMUX Ratio Select (RS) Function

Two demultiplexer ratios can be selected DMUX 1:1 and DMUX1:2.

The ratio could be selected via the external RS command or via the 3WSI.

Figure 4-1. ADC in 1:1 Ratio

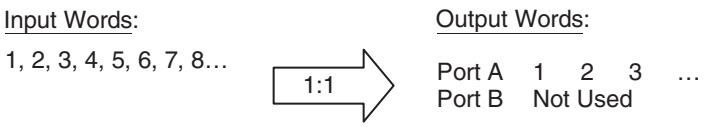
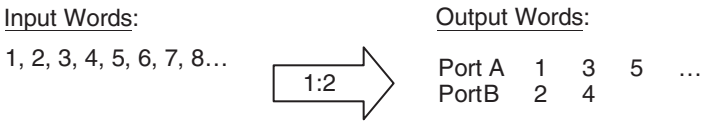


Figure 4-2. ADC in 1:2 Ratio



Note: Data of the different ports are synchronous: they appear at the same instant on each port. Maximum sampling frequency depends on the selected demulitplexer ratio. See Table 2-5.

4.4.1 DEMUX Ratio Selection with the External Command (RS Pin)

Two DEMUX Ratios can be selected thanks to pin RS according to the table below

Table 4-4. Ratio Select coding

Function	Logic Level	Electrical Level	Description
RS	0	10Ω to ground	1:1 DEMUX Ratio (Port A)
	1	10 KΩ to ground	1:2 DEMUX Ratio (Ports A and B)
		N/C	

4.4.2 DEMUX Ratio Selection with 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated and when the bit D0 of the state register (address 0000) is set to 0.

Please refer to state register coding for more details in Section 4.13.3 ”State Register (address 0000)” on page 39.

Table 4-5. State Register Coding

Label		Coding	Description	Default Value
RS	D0	0	1:1 DMUX mode	1
		1	1:2 DMUX mode	

4.5 Test Mode (TM_n) Function

This mode can be selected thanks to pin TM_n either via the external command or via the 3WSI interface.

The purpose of the test mode is to test ADC outputs.

The main test modes consists of an alignment pattern in order:

- To validate the interface between the ADC and the FPGA at full speed in both DMUX 1:1 or DMUX 1:2 modes.
- To check the synchronization of output data between different ADCs (Output data shift after external synchronization pulse).

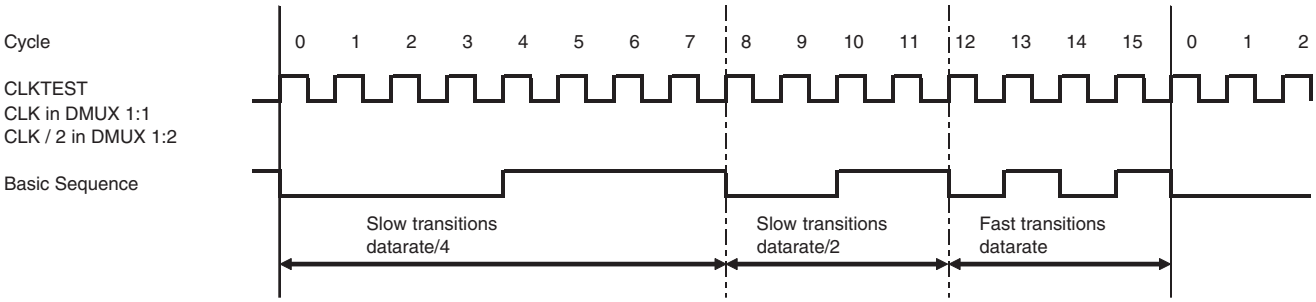
The alignment pattern consists of a sequence as described below and illustrated in Figure 4-3

- Period of 16 cycles at output data rate.
- start with four consecutive “0”
- Slow transitions at datarate over 4 and datarate over 2.
- Fast transitions at data rate.

To note:

- Same data between port A and Port B in DMUX 1:2 mode
- Parity Bit (PC) handled like other bits (no parity calculation) during Test mode.

Figure 4-3. Alignment Pattern Timing Diagram



4.5.1 Test Mode with the External Command (TM_n Pin)

The coding table for the Test mode with the external command is given below

Table 4-6. External Command Test Mode table

Function	Logic Level	Electrical Level	Description
TM_n	0	10Ω to ground	Alignment pattern ON (period of 16)
	1	10 KΩ to ground	Normal conversion mode (default mode)
		N/C	

4.5.2 Test Mode with 3WSI

This mode is selectable via 3WSI interface (Mode_n = 0) when the bit D2 of the state register (address 0000) is set to 0.

Please refer to State register coding for more details in Section 4.13.3 "State Register (address 0000)" on page 39.

Table 4-7. Test Register Coding (Address 0101)

Label		Coding	Description	Default Value
TM_n	D2	0	Test Mode ON (refer to register at address 0101)	1
		1	Test Mode OFF	

Description:

Other test modes are available when selectable via the test register (Address 0101) as described below

Table 4-8. Test Register Coding

Label	Coding	Description	Default Value
TEST TYPE <1:0>	00	V_{OL} Test: All data set to "0"	11
	01	V_{OH} Test: All data set to "1"	
	10	Unused	
	11	Alignment Pattern ON (period 16)	

4.6 Sampling Delay Adjust (SDA)

Sampling delay adjust (SDA pin) allows to tune the sampling ADC aperture delay (TA) around its nominal value.
This feature is particularly interesting for interleaving ADCs to increase sampling rate.
This function could be activated either by external command or the 3WSI.

4.6.1 Sampling Delay Adjust (SDA) Function with the External Command (SDA Pin)

This functionality is enabled thanks to the SDAEN_n signal, which is active at low level (when tied to ground) and inactive at high level (10 KΩ to Ground, or tied to V_{CC3} = 3.3V, or left floating).

The coding table for the SDAEN_n is given in the table below

Table 4-9. SDAEN_n coding with external command

Function	Logic Level	Electrical Level	Description
SDAEN_n	0	10Ω to ground	Sampling delay adjust enabled
	1	10 KΩ to ground	Sampling delay adjust disabled
		N/C	

Description:

With the external command (SDA pin), it is possible to tune the sampling ADC aperture delay by applying a control voltage on SDA pin.

Typical tuning range is from 0 to ~30 ps for applied control voltage varying between ±0.5V around 2/3*Vcc3 on SDA pin around the default value.

This tuneable delay is in addition of the default coarse SDA fixed in the 3WSI register.

If not used, this function should be disabled via SDAEN_n.

4.6.2 Sampling Delay Adjust (SDA) Function with 3WSI Interface

This mode is selectable when 3WSI interface (Mode_n = “0”) is activated and when the bit D1 (SDAEN_n) of the state register (address 0000) is set to “0”.

Table 4-10. SDAEN_n Coding with 3WSI Command

Label		Coding	Description	Default Value
SDAEN_n	D1	0	Sampling Delay adjust Function enabled	1
		1	Sampling Delay adjust Function disabled	

Please refer to State register coding for more details in Section 4.13.3 ”State Register (address 0000)” on page 39.

Description:

Via the 3WSI, the SDA value is coded in the register SDA (Address 0011) and described below.

The SDA resister is composed of 2 registers: the SDA coarse on 2 bit and SDA fine on 10 bit.

Total SDA delay is given by SDA coarse value in addition to SDA fine value.

SDA coarse register [1:0] allows a variation step of 0, 24 ps, 48 ps or 72 ps.

SDA fine register [9:0] allows a fine step of 24fs between a range of 0 to 24 ps

So the Sampling Delay adjusts with the 3WSI interface could vary from 0 ps up to 96 ps with a step of 24fs.

Table 4-11. 3WSI SDA Register Mapping (Address 0011)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SDA coarse<1:0>		SDA fine <9:0>									

Table 4-12. 3WSI SDA Register Description

Description	Default Register Value	Default Parameter Value	Register Value for Max Value	Parameter Max Value	Register Value for Min Value	Parameter Min Value	Step
Sampling Delay Adjust coarse	0x02	48 ps	0x03	72 ps	0x00	0 ps	24 ps
Sampling Delay Adjust fine	0x000	0 ps	0x3FF	24 ps	0x000	0 ps	24 fs

4.7 Gain Adjust (GA) Function

This function allows adjusting ADC Gain so that it can always be tuned to 1.0

This function could be activated either by external command or the 3WSI, while 3WSI operation is recommended.

4.7.1 Gain Adjust Function with the External Command (GA Pin)

Tuning the voltage applied on GA pin by ±0.5V around 2*Vcc3/3 allows to tune the gain by ~±10%.

2*Vcc3/3+0.5V gives the most positive gain variation and 2*Vcc3/3-0.5V gives the most positive offset variation.

4.7.2 Gain Adjust Function with the 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated.

Please refer to State register coding for more details in Section 4.13.3 ”State Register (address 0000)” on page 39.

Description:

The ADC Gain can be tuned by ±10% by step of 0.8LSB according the value coded in GA register mapping (Address 0001) as described below.

Table 4-13. GA Register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

Figure 4-4. Gain versus Gain Adjust (3WSI)

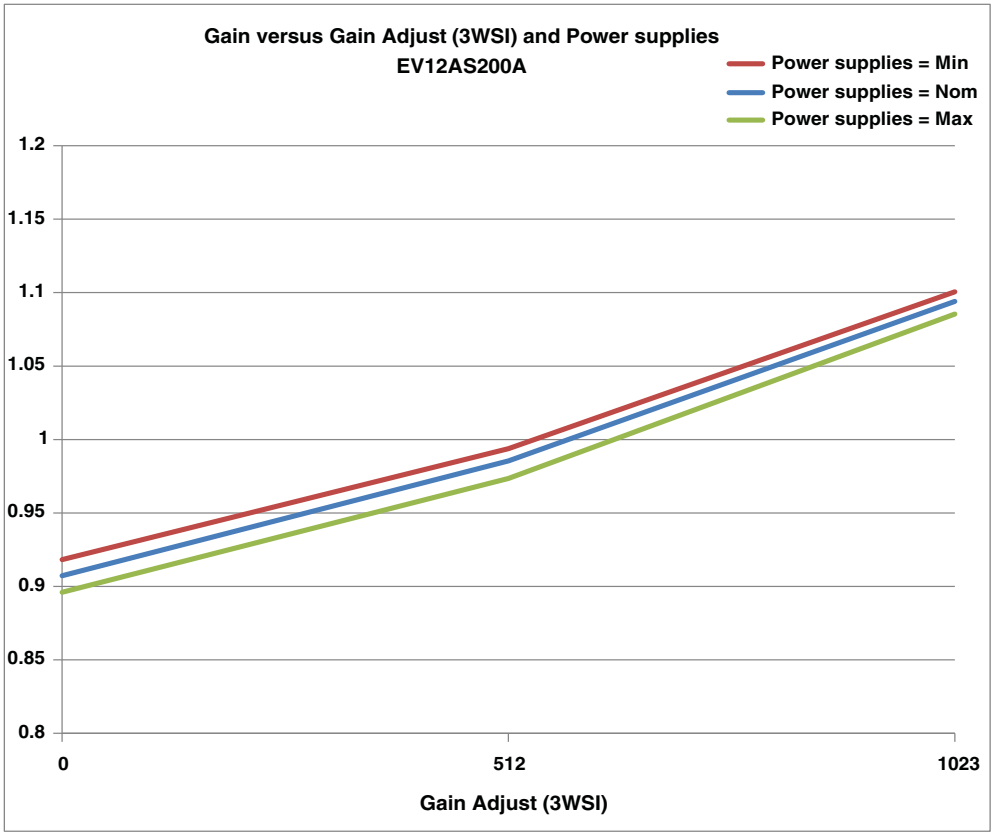


Table 4-14. GA Register Description

Description	Default Register Value	Default Parameter Value	Register Value for Max Value	Parameter Max Value	Register Value for Min Value	Parameter Min Value	Step
GA register <9:0>	0x200	1 (500mVpp)	0x3FF	1.10 (550 mVpp)	0x000	0.90 (450mVpp)	0.0002 (0.097mV)

4.8 Offset Adjust (OA) Function

This function allows adjusting ADC Offset so that it can always be tuned to mid-code 2048.

This function could be activated either by external command or the 3WSI.

4.8.1 Offset Adjust Function with the External Command (OA Pin)

The ADC Offset can be tuned by ±100 LSB (about ± 12 mV) by tuning the voltage applied on OA by ±0.5V around 2*Vcc3/3 in average.

2*Vcc3/3+0.5V gives the most negative offset variation and 2*Vcc3/3-0.5V gives the most positive offset variation.

4.8.2 Offset Adjust Function with the 3WSI

This mode is selectable when 3WSI interface (Mode_n = 0) is activated.

Please refer to State register (address 0000) coding for more details in Section 4.13.3 ”State Register (address 0000)” on page 39.

Description

The ADC offset can be tuned by ±100LSB by step lower than 0.4LSB according to the value coded in offset register mapping (Address 0010) as described below.

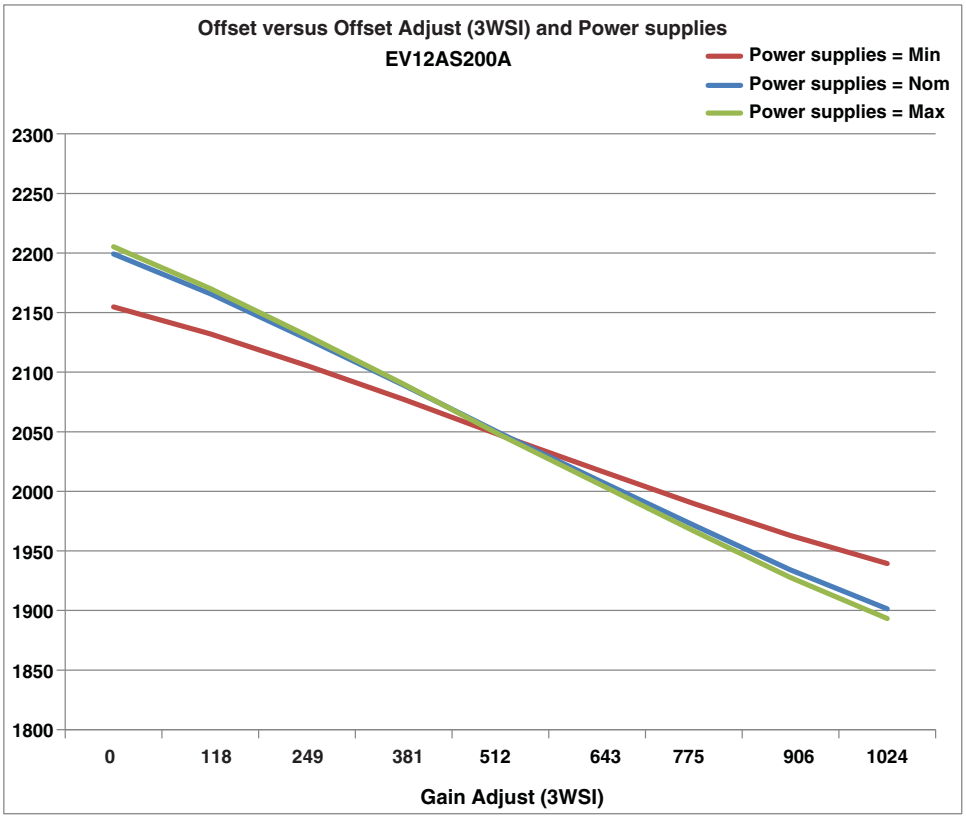
Table 4-15. OA Register Mapping (Address 0010)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		OA<9:0>									

Table 4-16. OA Register Description

Description	Default Register Value	Default Parameter Value	Register Value for Max Value	Parameter Max Value	Register Value for Min Value	Parameter Min Value	Average Step
Offset Adjust	0x200	0 LSB	0x000	+100 LSB (+12 mV)	0x3FF	–100 LSB (–12 mV)	0.4 LSB max (0.05 mV)

Figure 4-5. Offset versus Offset Adjust (3WSI)



4.9 RES Function

This function allows changing the active edge of the SYNC signal.
This function is only selectable via the 3WSI.

Please refer to State register coding for more details in Section 4.13.3 ”State Register (address 0000)” on page 39

Label		Coding	Description	Default Value
RES	D7	0	RESET edge select: rising edge	1
		1	RESET edge select: falling edge	

4.10 Decimation (DEC_n) function

The decimation function should only be used for debug purpose of the ADC and must not be used as standard operation mode.
This function indeed allows reducing the ADC output rate by 8 (assuming a 1:1 DEMUX Ratio), thus allowing for a quick debug phase of the ADC at max speed rate and is compatible with industrial testing environment.

When active, this function makes the ADC output only 1 out of 8 data, thus resulting in a data rate which is 8 times slower than the clock rate. In addition, DEMUX Ratio can be chosen in order to divide the data rate by 16 (DMUX1:2 mode).

This mode is selectable when 3WSI interface (Mode_n = 0) is activated and when the bit D3 (DEC_n) of the state register (address 0000) is set to 0

Please refer to State register coding for more details in Section 4.13.3 ”State Register (address 0000)” on page 39.

Table 4-17. CA register Mapping (Address 0000)

Label		Coding	Description	Default Value
DEC_n	D3	0	Decimation per 8	1
		1	No Decimation	

4.11 DIODE Function

A diode for die junction temperature monitoring is available in this ADC. It is constituted by an ESD diode. Both Anode and cathode of the diode are accessible externally.

In order to monitor the die junction temperature of the ADC, a current of 1 mA has to be applied on the DIODEA pin (anode of the diode). The voltage across the DIODEA pin and the DIODEC pin provides the junction temperature of the die thanks to the intrinsic diode characteristics.

It is recommended to use three protection diodes to avoid any damage due to over-voltages to the internal diode. The recommended implementation is provided in below.

Figure 4-6. Temperature DIODE implementation

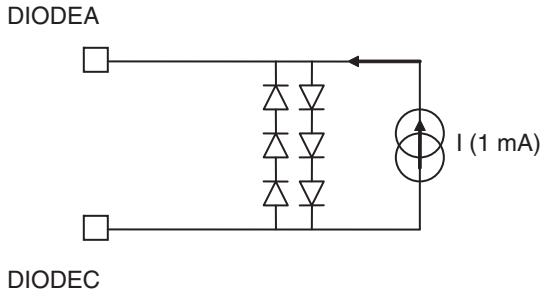
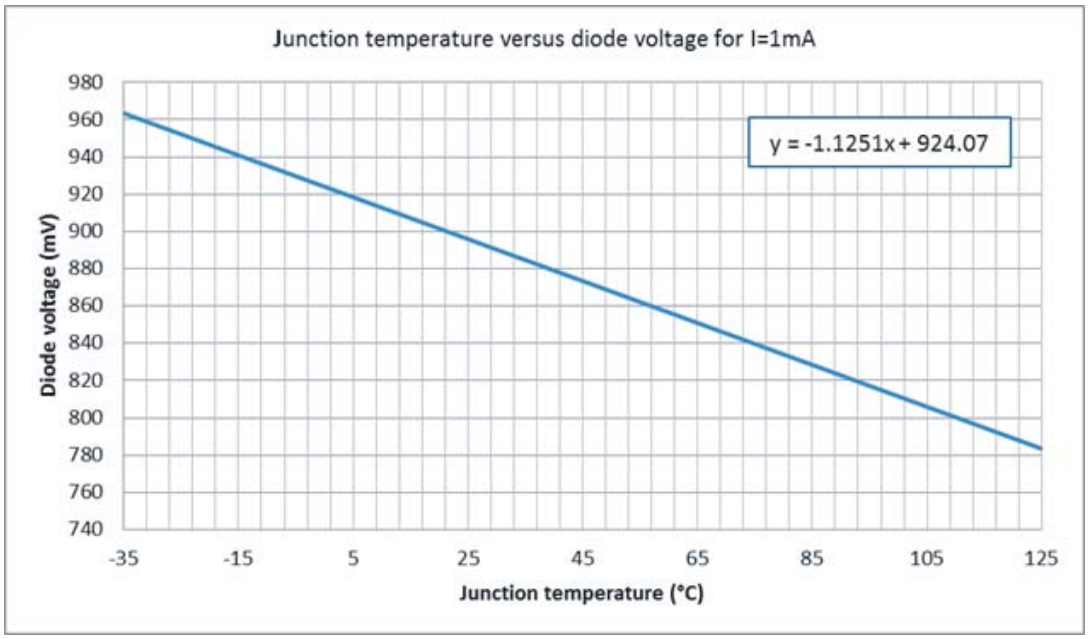


Figure 4-7. Diode characteristics for die junction monitoring



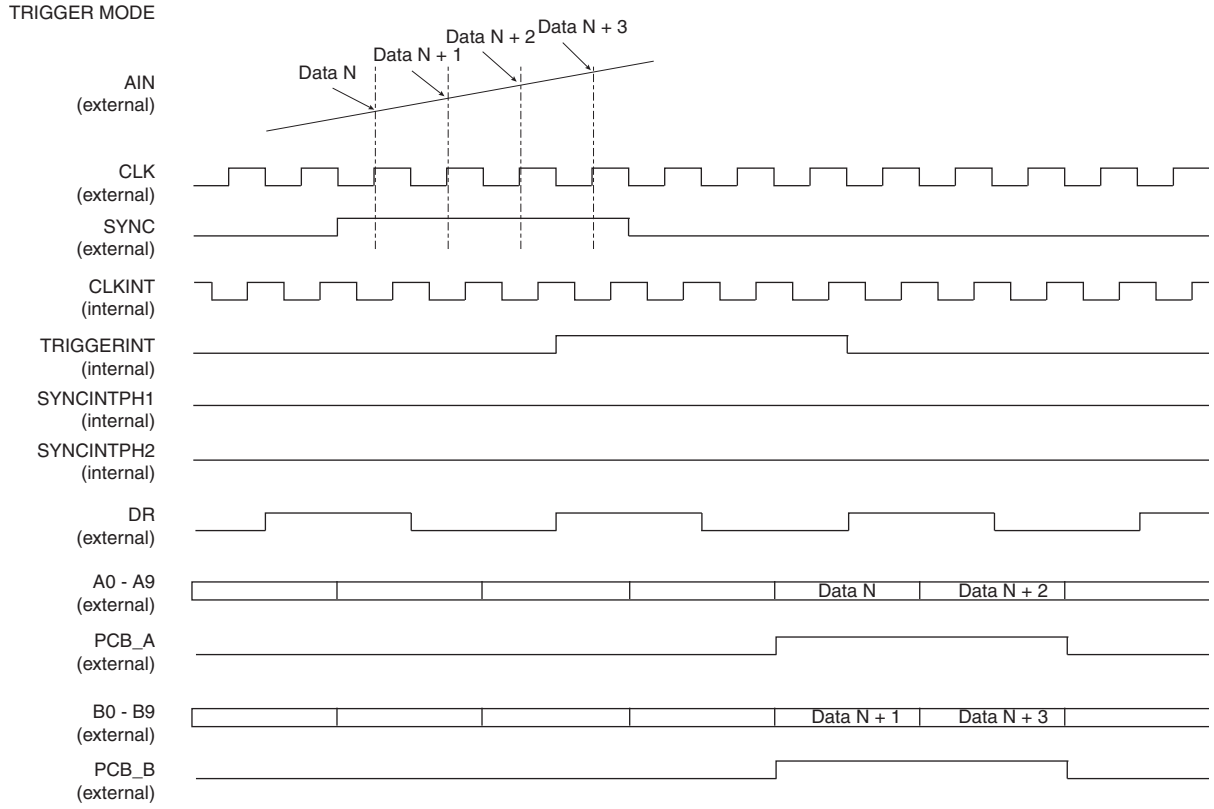
4.12 TRIGGER Function

This function is only selectable via the 3WSI.

This function allows helping to synchronise multiple ADCs and can provide a reference for the output data.

The pulse applied on SYNC is outputted after pipeline on the Parity Check pins (PCB_A) & (PCB_B) in DMUX 1:2.

Figure 4-8. Trigger Mode Diagram



Please refer to State register coding (address 0000) for more details in Section 4.13.3 ”State Register (address 0000)” on page 39.

Table 4-18. TRIGGER Coding Description

Label		Coding	Description	Default Value
TRIG_SEL_n	D8	0	Trigger mode (Trigger on pulse PCB_X if positive pulse edge on SYNC. Internal synchronization inhibited where X = A or B port)	1
		1	Synchronization mode (synchronization of internal functions on positive pulse on SYNC)	

4.13 ADC 3WSI Description (ADC Controls)

The digital interface of the ADC is activated via the mode_n signal (active low).

4.13.1 3WSI Timing Description

The 3WSI is a synchronous write only serial interface made of 4 wires:

- “reset_n”: asynchronous 3WSI reset, active low
- “sck”: serial clock input
- “sld_n”: serial load enable input
- “mosi”: serial data input.

The 3WSI gives a “write-only” access to up to 16 different internal registers of up to 12 bit each.

The input format is fixed with always 4 bit of register address followed by always 12 bit of data.

Address and data are entered MSB first.

The write procedure is fully synchronous with the clock rising edge of “sclk” and described in the write chronogram hereafter.

“sld_n” and “mosi” are sampled on each rising clock edge of “sclk” (clock cycle).

“sld_n” must be set at “1” when no write procedure is done.

A write starts on the first clock cycle with “sld_n” at “0”. “sldn” must stay at “0” during the complete write procedure.

In the first 4 clock cycles with “sld_n” at “0”, 4 bit of register address from MSB (a[3]) to LSB (a[0]) are entered.

In the next 12 clock cycles with “sld_n” at “0”, 12 bit of data from MSB (d[11]) to LSB (d[0]) are entered.

This gives 16 clock cycles with “sld_n” at “0” for a normal write procedure.

A minimum of one clock cycle with “sld_n” returned at “1” is requested to end the write procedure, before the interface is ready for a new write procedure.

Any clock cycle with “sld_n” at “1” before the write procedure is completed interrupts this procedure and no data transfer to internal registers is done.

Additional clock cycles with “sld_n” at “0” after the parallel data transfer to the register (done at 15tth consecutive clock cycle with “sld_n” at “0”) do not affect the write procedure and are ignored.

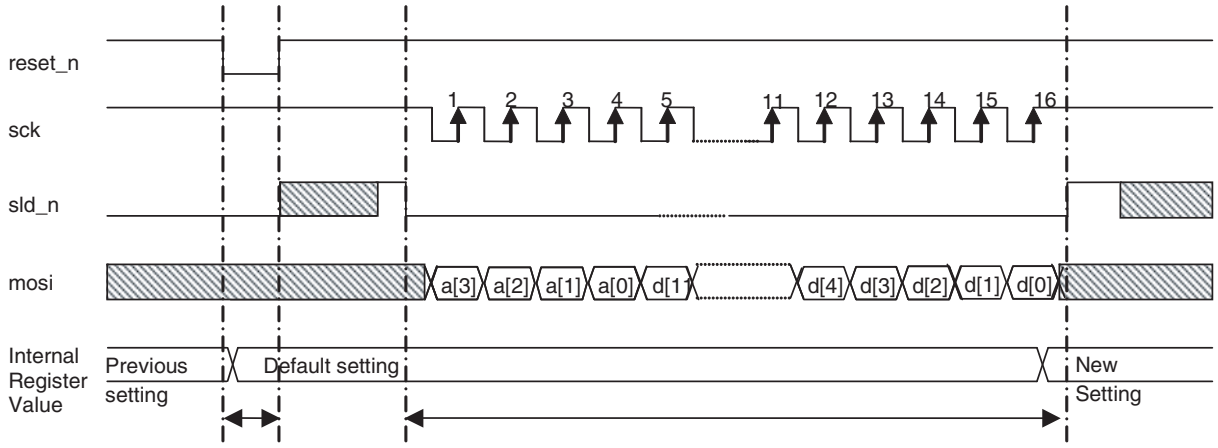
It is possible to have only one clock cycle with “sld_n” at “1” between two following write procedures.

12 bit of data must always be entered even if the internal addressed register has less than 12 bit. Unused bits (usually MSB’s) are ignored. Bit signification and bit position for the internal registers are detailed in the chapter “Registers”.

The “reset” pin combined with the “sld_n” pin can be used as a reset to program the chip to the “reset setting”.

- “reset_n” high: no effect
- “reset_n” low and “sld_n” low: programming of registers to default values

Figure 4-9. 3WSI Timing Diagram



Timings related to 3WSI are given in the table below

Table 4-19. 3WSI Timings

Name	Parameter	Min	Typ	Max	Unit	Note
Tsck	Period of sclk	10			ns	
Twsck	High or low time of sclk	5			ns	
Tssld_n	Setup time of sldn before rising edge of sclk	4			ns	
Thsld_n	Hold time of sld_n after rising edge of sclk	2			ns	
Tsmosi	Setup time of mosi before rising edge of sclk	4			ns	
Thmosi	Hold time of sdata after rising edge of sclk	2			ns	
Twlreset_n	Minimum low pulse width of reset	5			ns	
Tdreset_n	Minimum delay between an edge of reset and the rising edge of sclk	10			ns	

4.13.2 3WSI: Address and Data Description

This 3WSI is activated with the control bit sld_n going low (please refer to “write timing” in next section).

The length of the word is 16 bit: 12 for the data and 4 for the address.

The maximum serial logic clock frequency is 100 MHz.

Table 4-20. Registers Mapping

Address	Label	Description	Default Setting
0000	State Register	DMUX ratio Selection Sampling Delay Adjust Enable Test Mode Enable Output clock division ratio selection Trigger mode selection	0x7FF
0001	GA Register	Gain adjust register	0x200
0010	OA Register	Offset adjust register	0x200
0011	SDA Register	Sampling delay adjust register	0x002
0101	Test Register	Test modes register	0x7
0110		reserved	
0111		reserved	
1000 to 1111		reserved	

4.13.3 State Register (address 0000)

Table 4-21. State register Mapping (Address 0000)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
reserved			TRIG_SEL_N	RES	reserved				TM_n	SDAEN_n	RS

Table 4-22. State register Coding (Address 0000)

Label		Coding	Description	Default Value
RS	D0	0	1:1 DMUX mode	1
		1	1:2 DMUX mode	
SDAEN_n	D1	0	Sampling Delay Adjust function Enabled	1
		1	Sampling Delay Adjust function Disabled	
TM_n	D2	0	Test Mode ON (refer to register at address 0101)	1
		1	Test Mode OFF	
DEC_n	D3	0	Decimation by 8 ON	1
		1	Decimation by 8 OFF	1
Not used	D4			1
Not used	D5			1
Not used	D6			1
RES	D7	0	RESET edge select: rising edge	1
		1	RESET edge select: falling edge	
TRIG_SEL_N	D8	0	Trigger mode (Trigger pulse on PCB_X if positive pulse on SYNC. Internal synchronization inhibited, where X = A or B)	1
		1	Synchronization mode (Synchronization of internal functions on positive pulse on SYNC)	
Not used	D9			1
Not used	D10			1
Not used	D11			1

Notes:
1. when the digital interface is not active, default mode is DMUX 1:1 at half sampling speed.
2. Test pattern function “Always running”: Internal synchronization not affected by mode (TM_n) change.
3. Bit D4, D5, D6, D9, D10, D11 are reserved.
4. Synchronization and Trigger modes.

4.13.4 GA Register (address 0001)

Table 4-23. GA register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

4.13.5 OA Register (address 0010)

Table 4-24. OA register Mapping (Address 0010)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		OA<9:0>									

4.13.6 SDA Register (address 0011)

Table 4-25. SDA register Mapping (Address 0011)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SDA coarse<1:0>		SDA fine <9:0>									

4.13.7 Test Register (address 0101)

Table 4-26. Test Register Mapping (Address 0101)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<Unused>									TH_en	TEST TYPE	

4.13.8 Tuning Register Summary

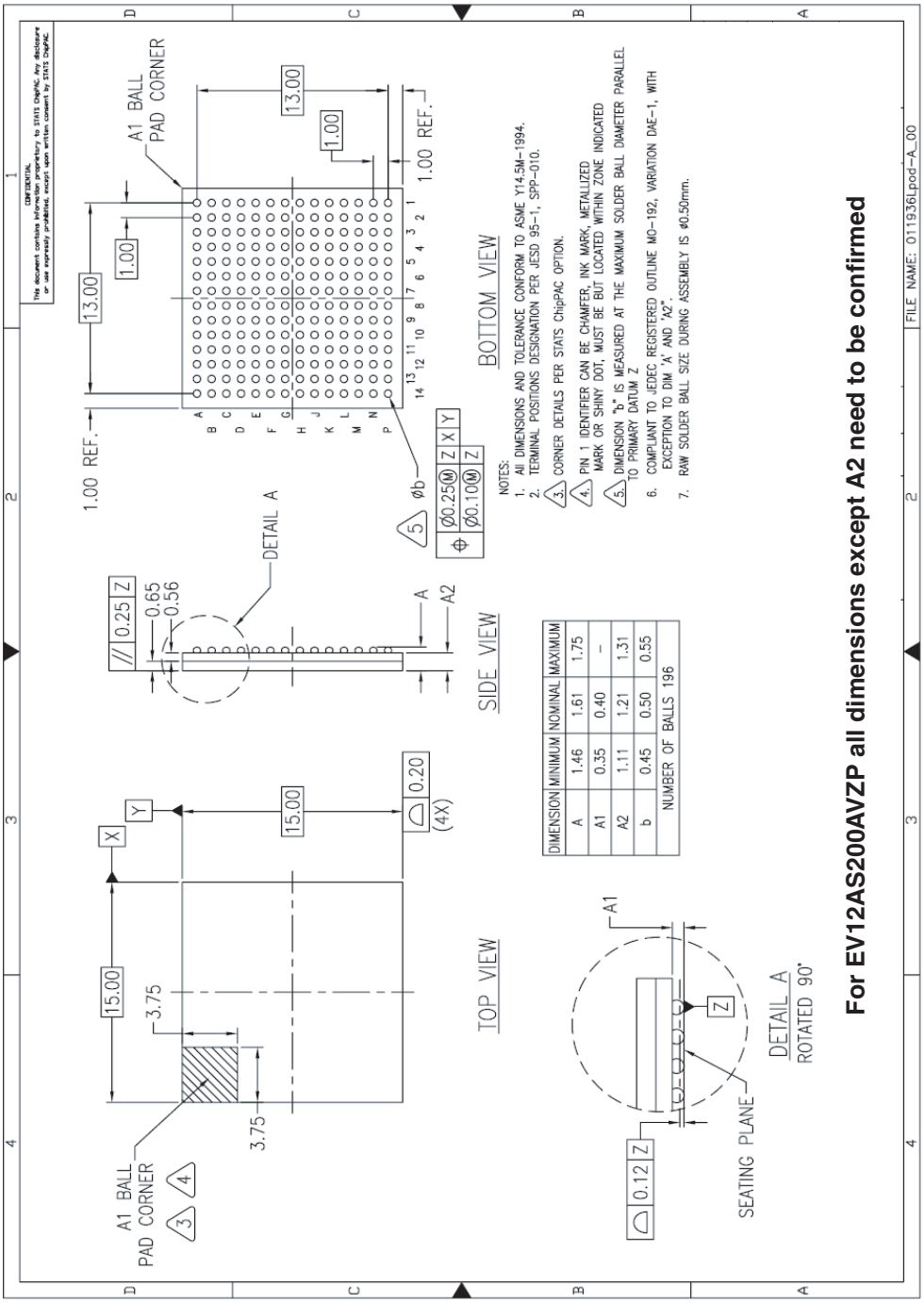
Table 4-27. Registers 0001 to 0100 Summary

Address	Description	Default Register Value	Default Parameter value	Register Value for Max Value	Parameter Max Value	Register Value for Min Value	Parameter Min Value	Step
0001	Gain Adjust	0x200	1 (500 mVpp 4096 LSB)	0x3FF	1.10 (550 mVpp 4506 LSB)	0x000	0.90 (450 mVpp 3686 LSB)	0.032 (0.195 mV 1.6 LSB)
0010	Offset Adjust	0x200	0 LSB	0x000	+100 LSB	0x3FF	–100 LSB	0.4 LSB max
0011	Sampling Delay Adjust coarse	0x02	48 ps	0x03	72 ps	0x00	0 ps	24 ps
	Sampling Delay Adjust fine	0x000	0 ps	0x3FF	24 ps	0x000	0 ps	24 fs

5. Package Description

5.1 FpBGA196 Package Outline

Figure 5-1. FpBGA Top View



All units in mm
Sealring is connected to AGND

5.2 Thermal Characteristics of FpBGA196

Assumptions:

Die thickness = 300 µm

- No convection
- Pure conduction
- No radiation
- Heating zone = 8% of die surface

R_{TH}	Value	Unit
Junction-> Bottom of ball	12.8	°C/Watt
Junction-> Board	17.2	°C/Watt
Junction->Top of case	13.5	°C/Watt
Junction-> Ambiant	31.2	°C/Watt

Delta between Temperature of the die hotspot and the temperature monitored with the diode is 7.5°C

Assumptions:

- Heating zone = 5% of die surface
- Still air, Jedec condition

Rth Junction - ambient (JEDEC) = 31.2°C/W

6. Characterisation Results

Figure 6-1. ENOB vs Fin from 100 MHz to 2000 MHz@1.5 GSps

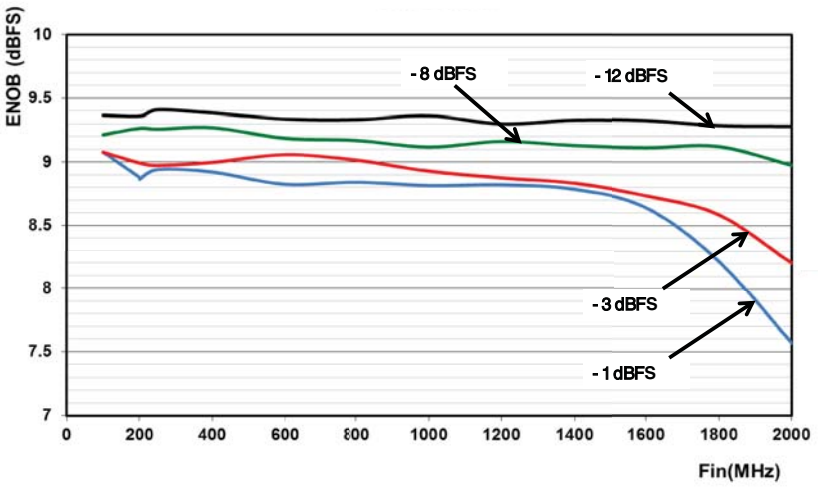


Figure 6-2. SNR vs Fin from 100 MHz to 2000 MHz@1.5 GSps

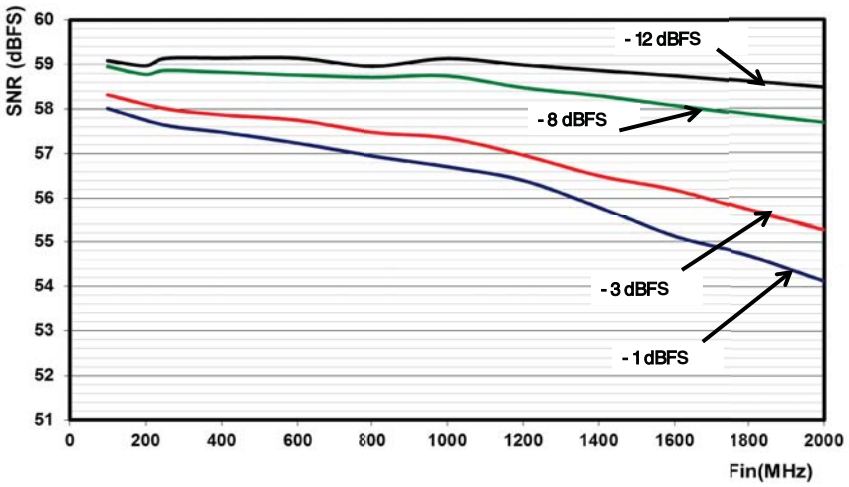


Figure 6-3. SNR vs Fin from 100 MHz to 2500 MHz@1.5 GSps

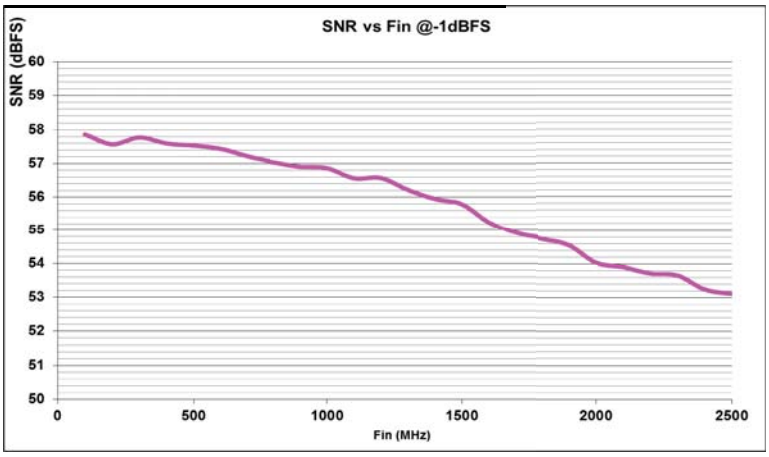


Figure 6-4. SFDR vs Fin from 100 MHz to 2000 MHz@1.5 GSps

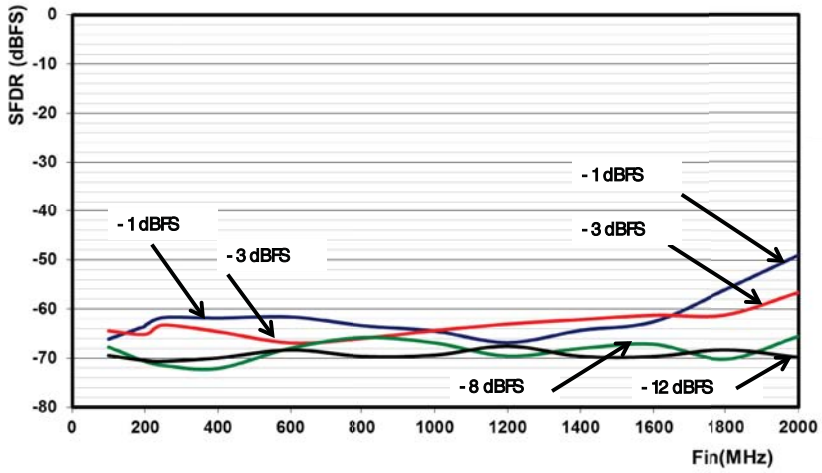


Figure 6-5. THD vs Fin from 100 MHz to 2000 MHz@1.5 GSps

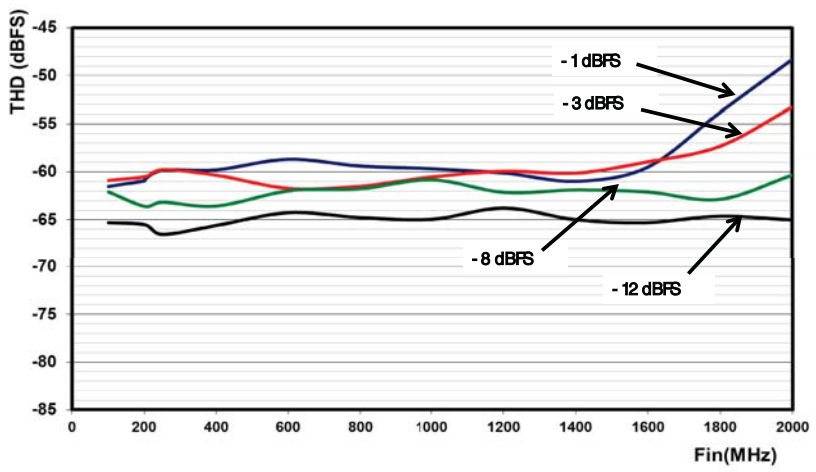


Figure 6-6. FFT 1.5 GSps Fin = 745 MHz@–1 dBFS

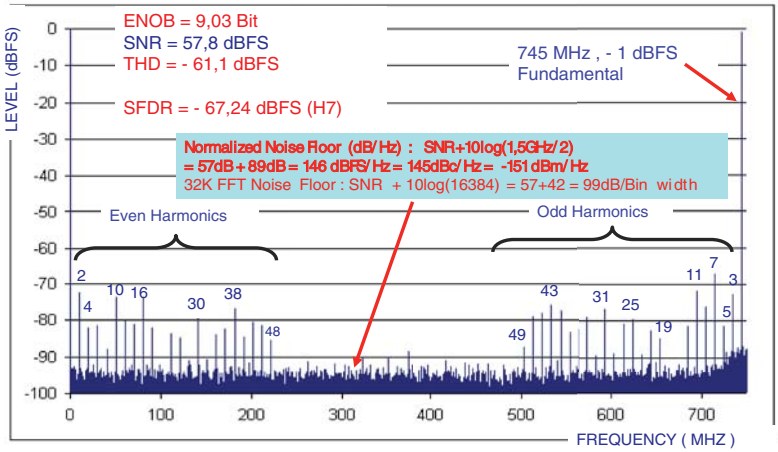


Figure 6-7. FFT 1.5 GSps Fin = 1490 MHz@–1 dBFS

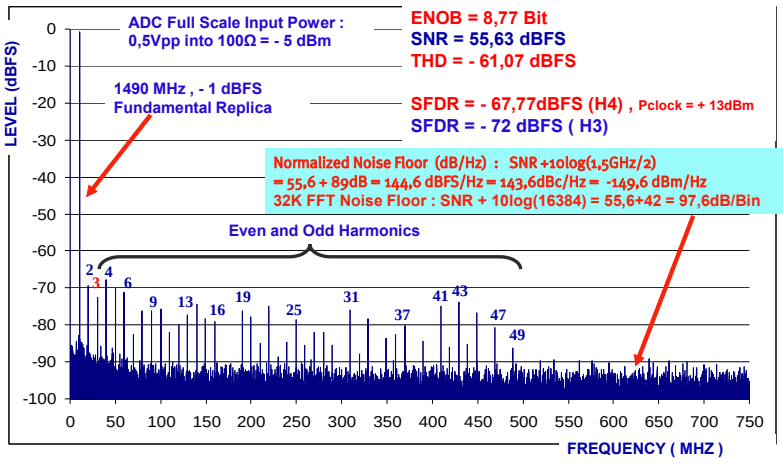


Figure 6-8. FFT 1.5 GSps Fin = 1490 MHz@–8 dBFS

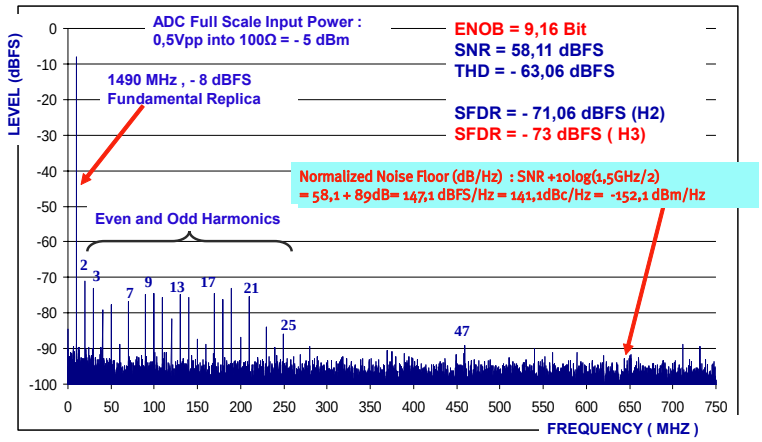


Figure 6-9. FFT 1.5 GSps Fin = 1490 MHz@–12 dBFS

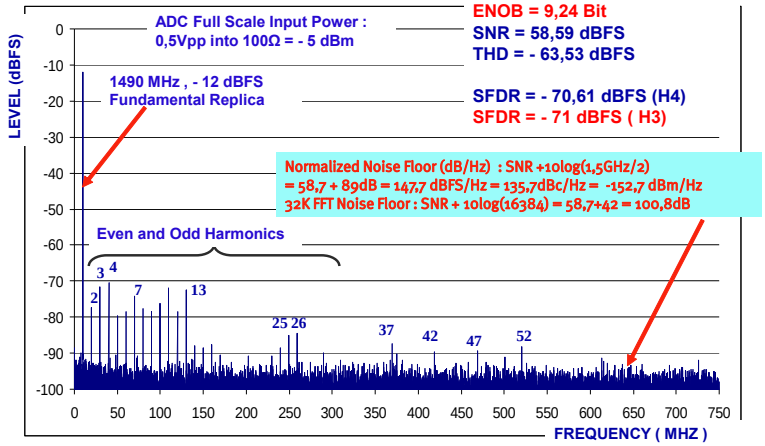


Figure 6-10. NPR@1.5 GSps with 600 MHz noise pattern

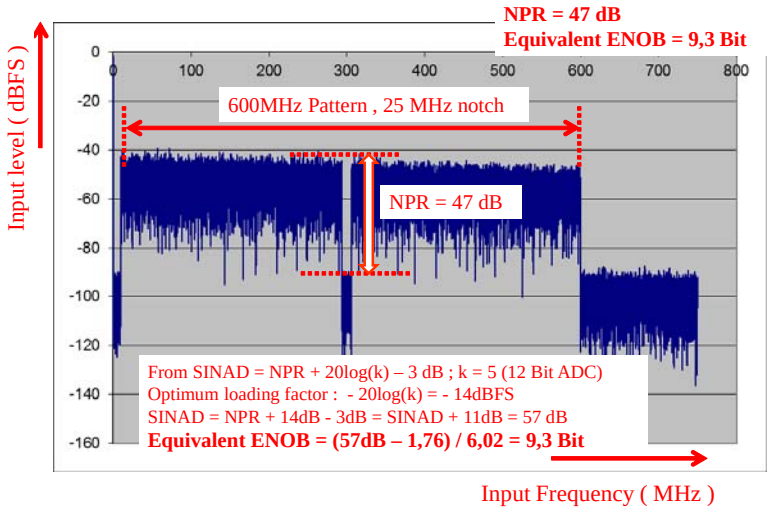


Figure 6-11. NPR@1.5 GSps with 450 MHz noise pattern

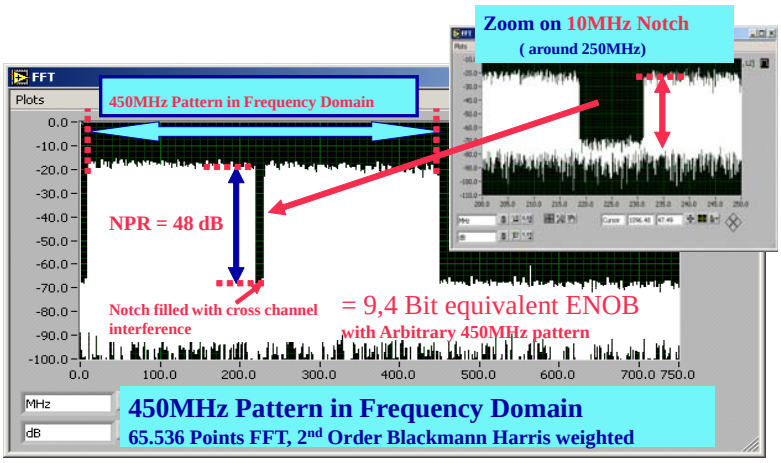


Figure 6-12. 450 MHz time domain noise pattern

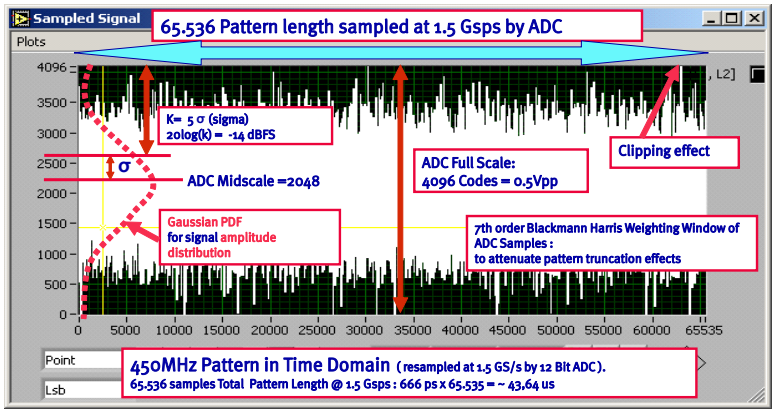


Figure 6-13. Ideal ADCs NPR versus loading factor

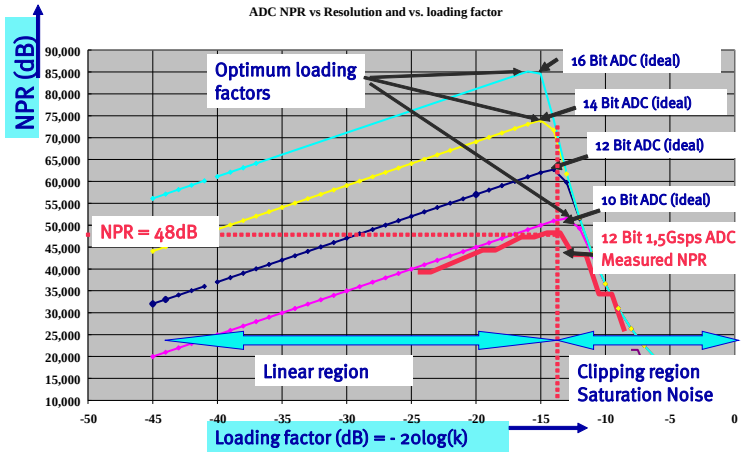


Figure 6-14. Spectral purity@1.5 GSps in first Nyquist

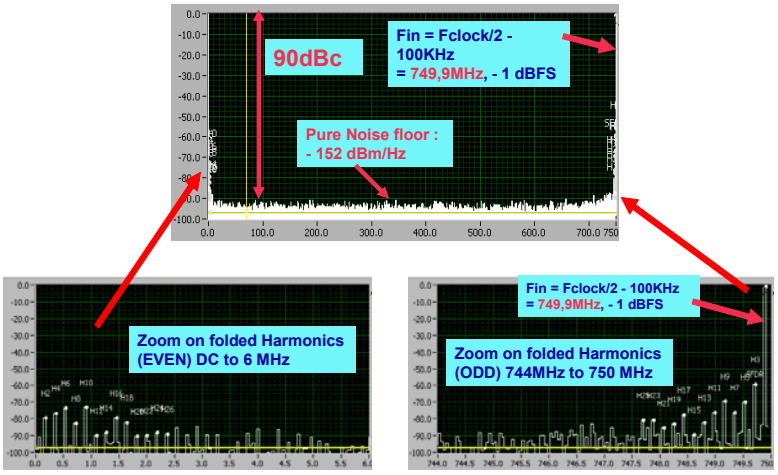


Figure 6-15. Spectral purity@1.5 GSps in second Nyquist

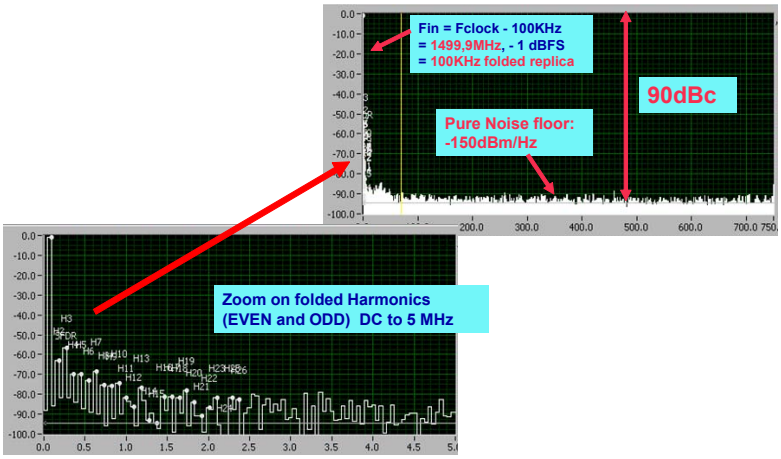


Figure 6-16. SFDR with Dither@1.5 GSps Fin 740 MHz

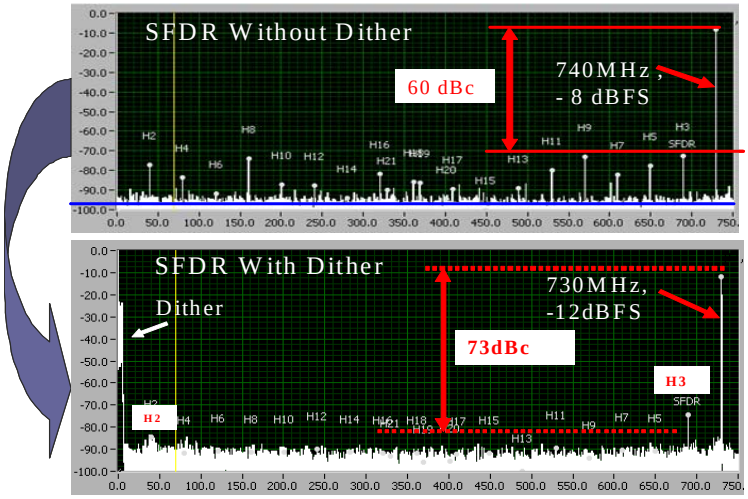


Figure 6-17. SFDR with Dither@1.5 GSps Fin 1480 MHz@–15 dBFS

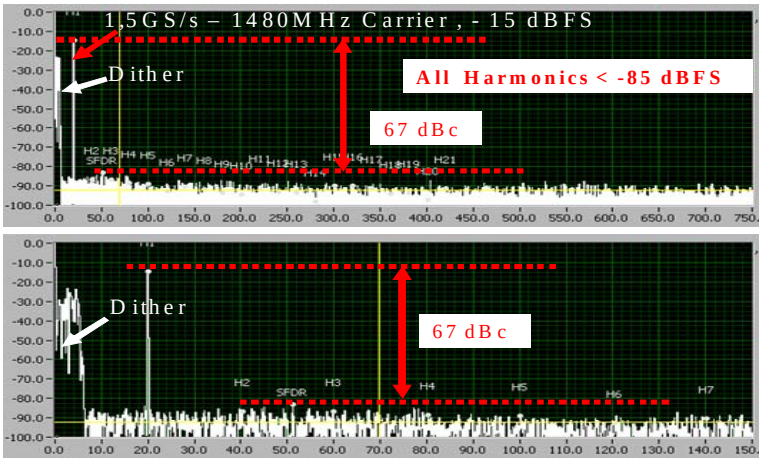


Figure 6-18. ENOB_FS versus Junction Temperature (°C) and Input level@Fin = 740 MHz

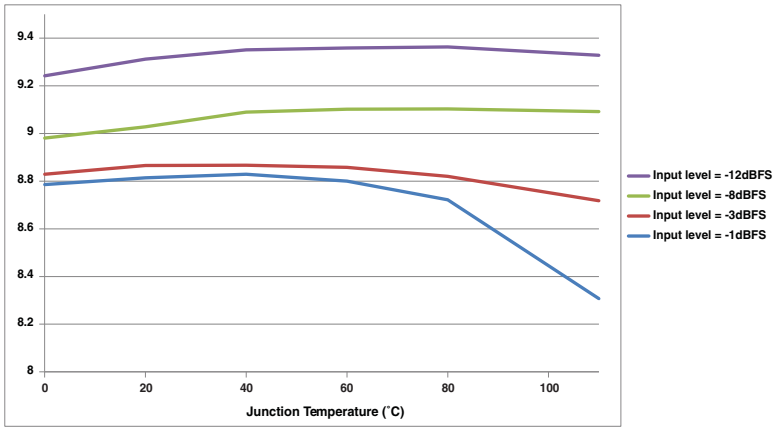


Figure 6-19. SNR_FS versus Junction Temperature (°C) and Input level@Fin = 740 MHz

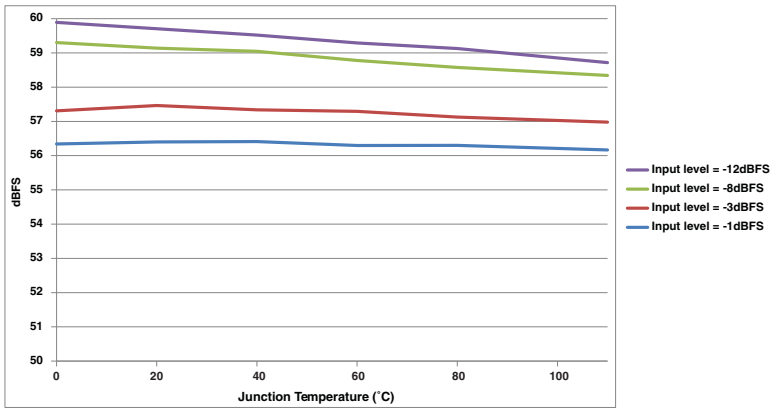


Figure 6-20. THD_FS versus Junction Temperature (°C) and Input level @Fin = 740 MHz

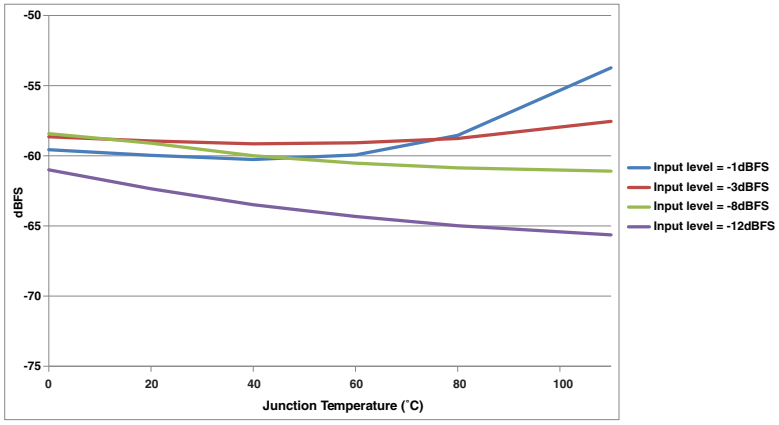


Figure 6-21. SFDR_FS versus Junction Temperature (°C) and Input level @Fin = 740 MHz

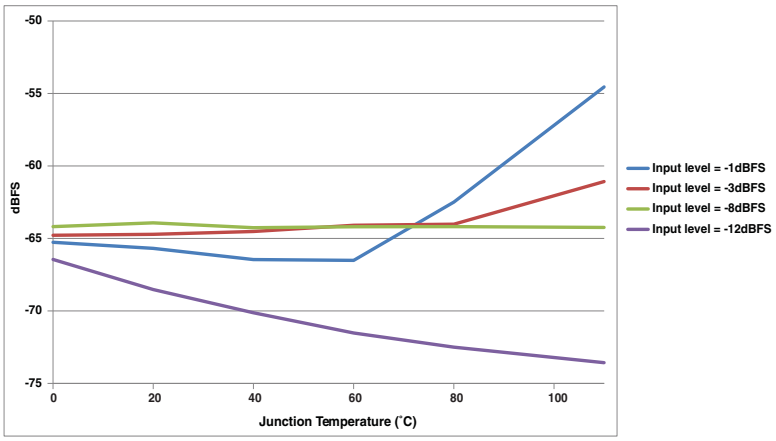


Figure 6-22. ENOB_FS versus Junction Temperature (°C) and Input level @Fin = 1490 MHz

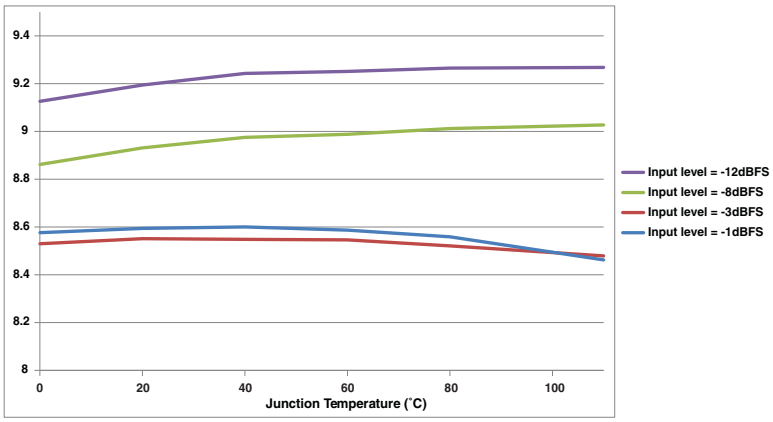


Figure 6-23. SNR_FS versus Junction Temperature (°C) and Input level @Fin = 1490 MHz

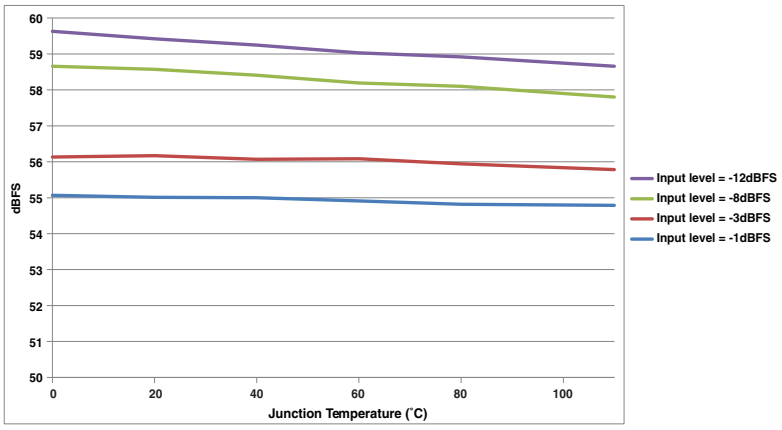


Figure 6-24. THD_FS versus Junction Temperature (°C) and Input level @Fin = 1490 MHz

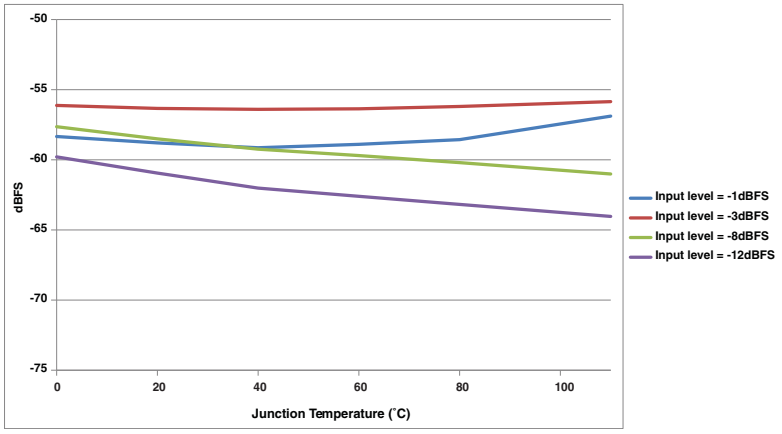


Figure 6-25. SFDR_FS versus Junction Temperature (°C) and Input level @Fin = 1490 MHz

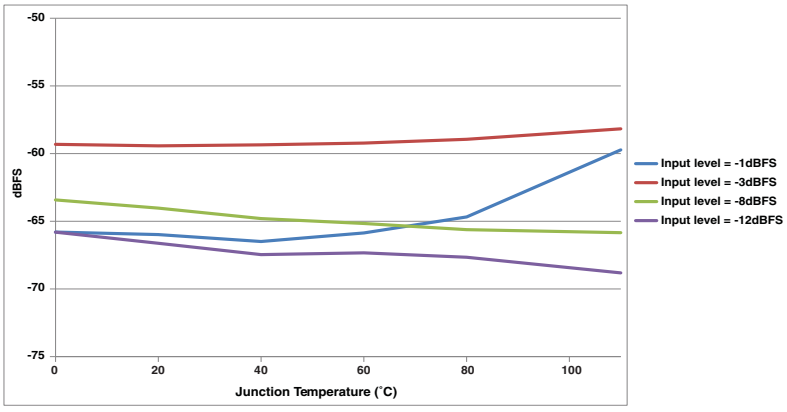


Figure 6-26. DNL Vs Ain @ 1.5 GSps Fin = 1490 MHz

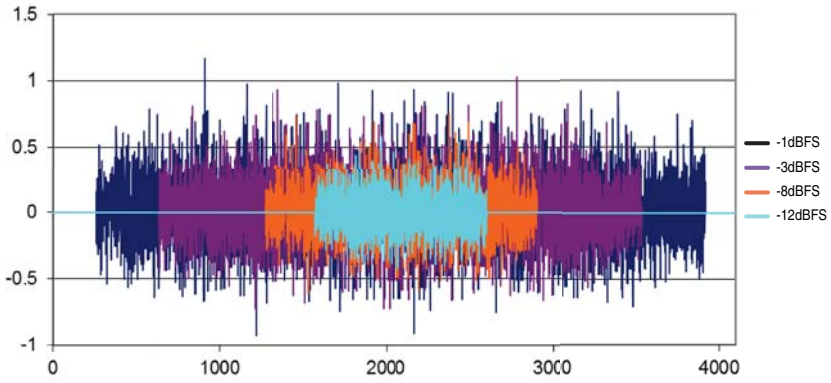


Figure 6-27. INL Vs Ain @ 1.5 GSps Fin = 1490 MHz

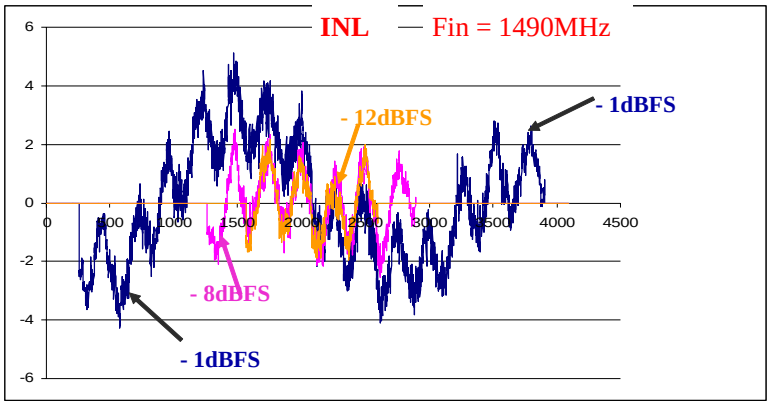


Figure 6-28. IMD3 Vs Input level @ 1.5 GSps Fin1 = 1450 MHz Fin2 = 1460 MHz

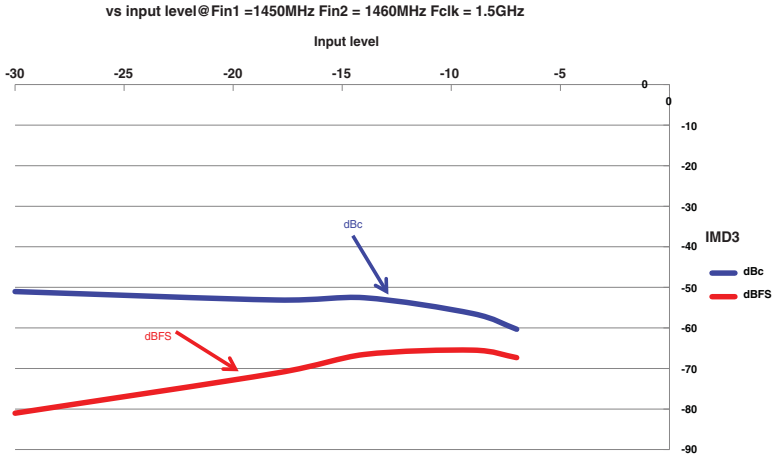


Figure 6-29. FFT IMD3 @ 1.5 GSps Fin1 = 1450 MHz Fin2 = 1460 MHz –7 dBFS

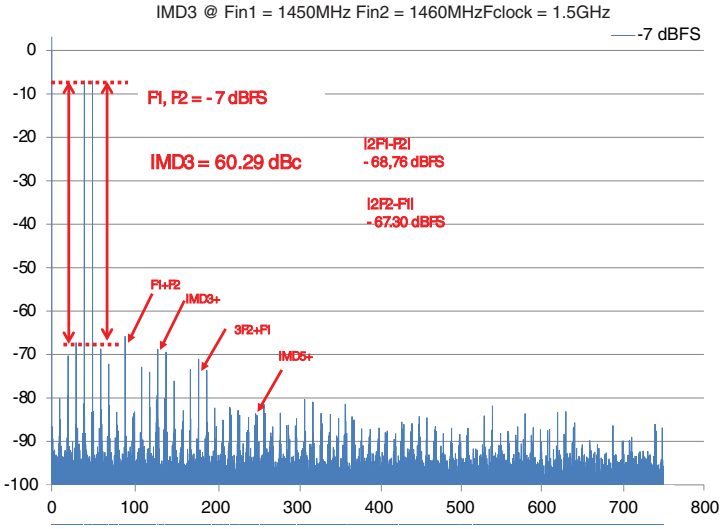


Figure 6-30. FFT IMD3 @ 1.5 GSps Fin1 = 1450 MHz Fin2 = 1460 MHz –7 dBFS

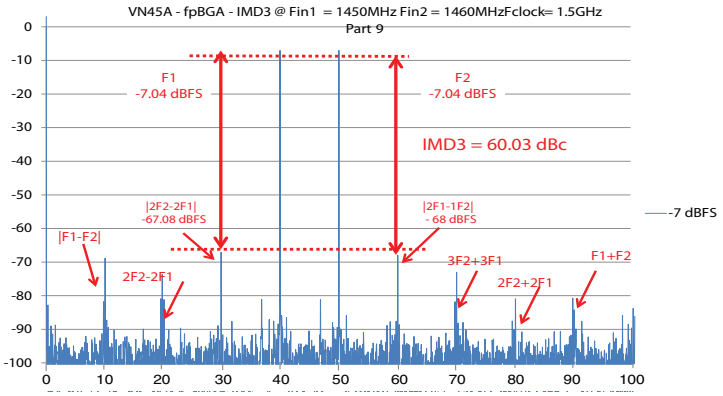
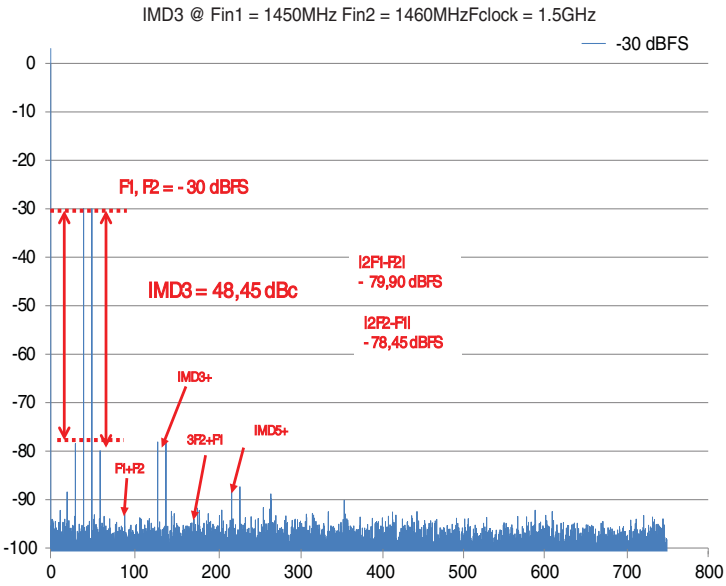


Figure 6-31. FFT IMD3 @ 1.5 GSps Fin1 = 1450 MHz Fin2 = 1460 MHz –30 dBFS



7. Applications

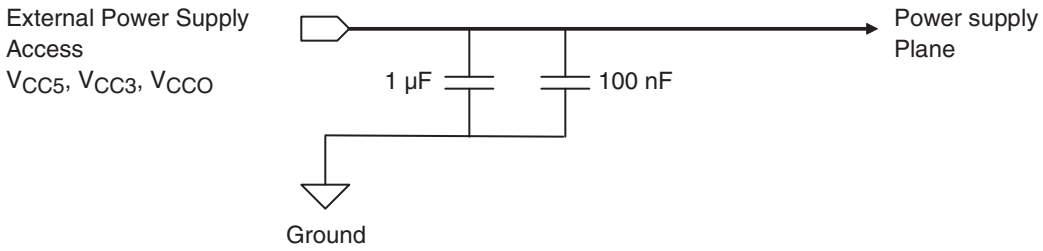
7.1 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor. Each power supply is decoupled as close as possible to the EV12AS200ZPY device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

Figure 7-1. EV12AS200 Power Supplies Decoupling and Grounding Scheme

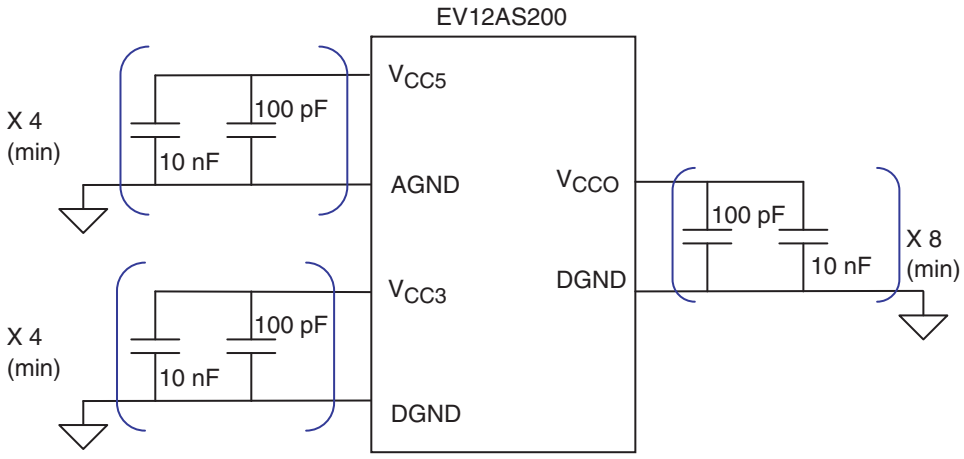


Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required number of pairs of capacitors by power supply type is:

4 for V_{CC5}
4 for V_{CC3}
8 for V_{CCO}

Figure 7-2. EV12AS200 Power Supplies Bypassing Scheme



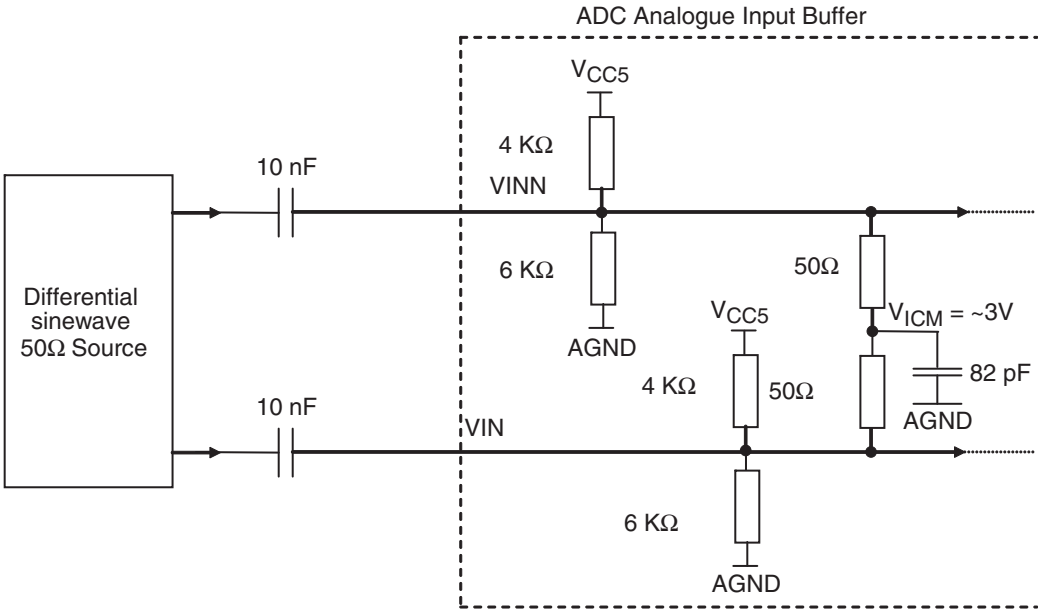
Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 1 µF capacitors.

7.2 Analogue Inputs (V_{IN}/V_{INN})

The analogue input should be used in differential mode. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

The analogue input should be AC coupled as described in figure below.

Figure 7-3. Differential Analogue Input Implementation (AC Coupled)

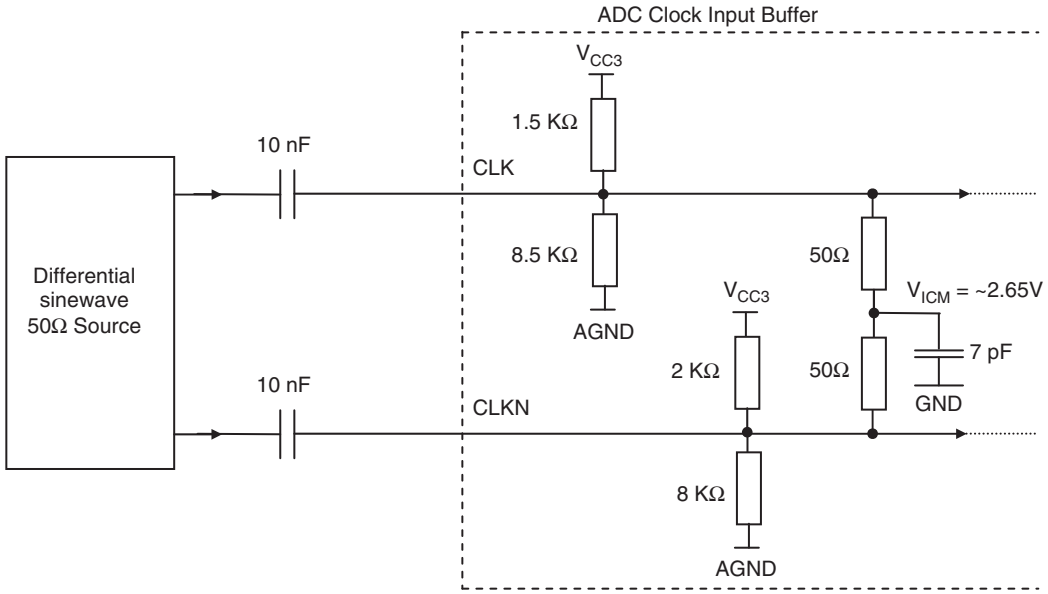


7.3 Clock Inputs (CLK/CLKN)

Differential mode is the recommended input scheme. Single-ended clock input is not recommended due to performance limitations. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

Since the clock input common mode is 2.7V, we recommend to AC couple the input clock as described in figure below.

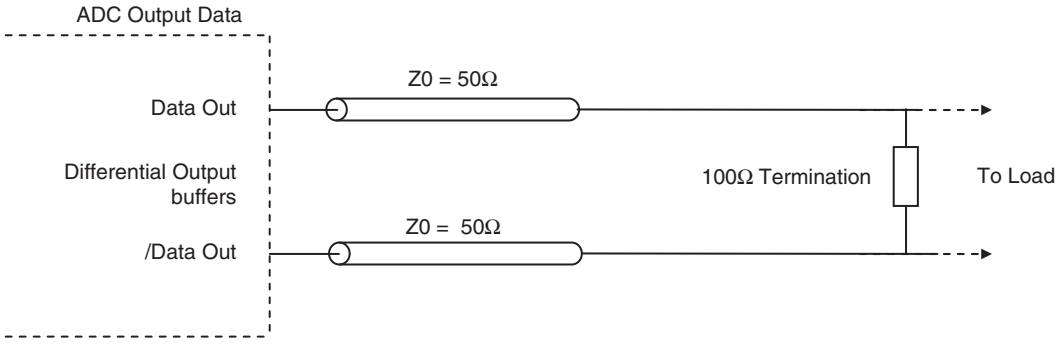
Figure 7-4. Differential Clock Input Implementation (AC Coupled)



7.4 Digital Outputs

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 7-5. Differential Digital Outputs Terminations (100Ω LVDS)



If the ADC is used in 1:1 or 1:2 DMUX modes, the unused ports can be left open (no external termination required).

8. Ordering Information

Table 8-1. Ordering information

Part Number	Package	Lead Finish	Temperature Range	Screening Level	Comments
EVX12AS200AZPY	FpBGA196 ROHS	SAC 305	Ambient	Prototype	
EV12AS200ACZPY	FpBGA196 ROHS	SAC 305	T_c > 0°C T_j < 90°c	Commercial grade	
EV12AS200AVZPY	FpBGA196 ROHS	SAC 305	T_c > –40°C T_j < 110°c	Industrial grade	
EV12AS200AZPY-EB	FpBGA196	NA	Ambient	Prototype	Evaluation board
EV12AS200AZPY-DK	Demonstration kit	NA	Ambient	Prototype	Evaluation board
EVX12AS200AZP	FpBGA196	SnPb 63/37	Ambient	Prototype	
EV12AS200AVZP	FpBGA196	SnPb 63/37	T_c > –40°C T_j < 110°c	Industrial grade	

9. Revision History

This table provides revision history for this document.

Table 9-1. Revision History

Rev. No	Date	Substantive Change(s)
1122C	06/2015	Table 3-1, “Pin Description FpBGA196,” on page 19: Equivalent simplified schematic of VIN/VINN corrected and Typo correction. Section 4.11 ”DIODE Function” on page 34: added temperature diode characteristic. Section 5.1 ”FpBGA196 Package Outline” on page 41: Drawing updated Table 8., “Ordering Information,” on page 56 added part number EV12AS200AVZP
1122B	09/2014	Table 2-2 on page 5 and Table 8-1 on page 56: Temperature range correction Table 8-1: Lead finish column added Typo correction in all document
1122A	07/2014	Initial revision

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