EV8DD700 / EV12DD700
Dual channel Ka-band capable 12 GSps DAC
Space Grade

Preliminary specification

OVERVIEW

The EV8DD700 / EV12DD700 is a Ka-band capable Rad-tolerant Dual current-steering 8-bit/12-bit Digital-to-Analog converter, with conversion rate up to 12 GSps, synthetizing signals at frequencies over 21GHz without up conversion. This DAC embeds digital features like interpolation, Digital Up Conversion (DUC) and Direct Digital Synthesis (DDS) to reduce input data-rate.

FEATURES & MAIN CHARACTERISTICS

- Dual 8-bit/12-bit resolution DAC core
- Conversion rate up to 12 GSps
- -3 dB Analog Bandwidth 25 GHz
- Output signal up to 25 GHz and more
- On chip 100 Ω differential termination
- SPI control
- Programmable Gain
- Selectable output modes:
  - Non Return to Zero (NRZ) up to 12 GSps
  - Radio Frequency (RF) up to 12 GSps
  - Twice RF (2RF) up to 12 GSps (Fc up to 24 GHz)
- Clock and sync distribution capabilities
- Slow clock for synchronization
- Multi-chip deterministic synchronisation
- Low latency serial link interface with ESIstream protocol, speed up to 12 Gbps
- Bypassable digital interpolation x4, x8 or x16
- Digital Up Conversion (DUC) with 32 bit-NCO
- Frequency hopping
- Digital Direct Synthesis (DDS) with chirp
- Digital Butler Matrix function
- Power consumption 5.8 W to 8.9 W
- 20x20 mm Hi-TCE package
- Temperature range: T_{case} = -55 °C to Tj=125 °C

APPLICATIONS

- Radars and jammers
- Instrumentation
- Terrestrial and space telecommunications
- Beamforming
- Software Define Radio
- Direct conversion up to Ka band

PERFORMANCE

- Output signal up to 21 GHz
- Fs = 12 GSps Fout up to 3.7 GHz Pout = 0 dBFs NRZ
  - SFDR 70 dBc
  - HD2 or HD3 70 dBc
  - NSD -154.8 dBm/Hz
- Fs = 12 GSps Fout 7.5 GHz Pout = 0 dBFs RF
  - SFDR 60 dBc
  - HD2 or HD3 60 dBc
  - NSD -154.8 dBm/Hz
- Fs = 12 GSps Fout 11.5 GHz Pout = 0 dBFs RF
  - SFDR 55 dBc
  - HD2 or HD3 57 dBc
  - NSD -154.8 dBm/Hz
- Fs = 12 GSps (Fc = 24 GHz) Fout 18.5 GHz Pout = 0 dBFs 2RF
  - SFDR 58 dBc
  - HD2 or HD3 58 dBc
  - NSD -154.0 dBm/Hz
- NPR at Fs = 12 GHz over 80% Nyquist zone, at optimum loading factor
  - 1st Nyquist 45 dB (NRZ)
  - 2nd Nyquist 40 dB (RF)
  - 3rd Nyquist 37 dB (RF)
  - 4th Nyquist 35 dB (2RF, Fc=24 GHz)

Table of content

An Important Notice at the end of this datasheet addresses availability, warranty, changes, use in critical applications, intellectual property matters and other important disclaimers.

1. REVISION HISTORY

Issue	Date	Comments
A	Oct 2019	Creation from target specification 1188EX
A.1	June 2020	Removed NDA marking
A.2	Sept 2020	Add EVP12DD700UH P/N
A.3	Sept 2020	P/N modifications

B.0	July 2021	EV8DD700 added New pinout (additional pins, renamed pins, numbering scheme IPC-7351B compliancy Single Core A or B updated New registers added DUC / “Digital LO frequency” formula modified Vccd power supply updated ESD section added Decoupling section modified Power-up sequence updated

2. BLOCK DIAGRAM

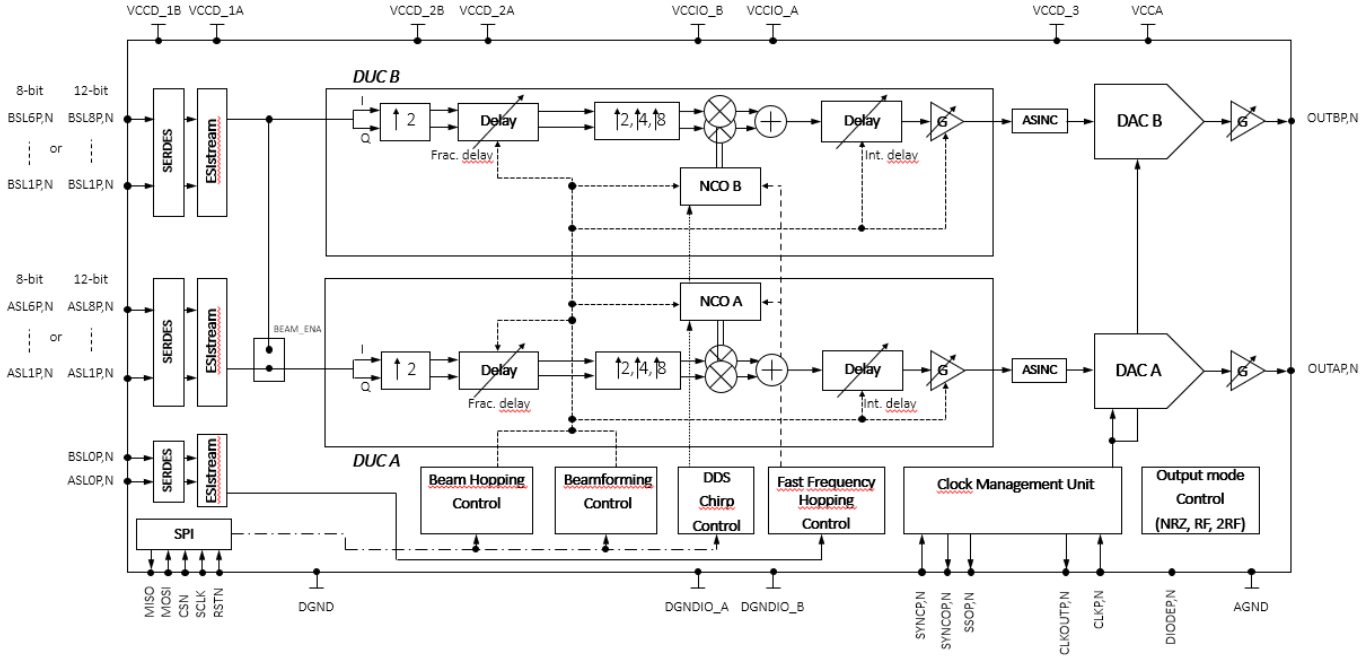


Figure 1: Simplified Block Diagram using Digital Up Converters and Digital features

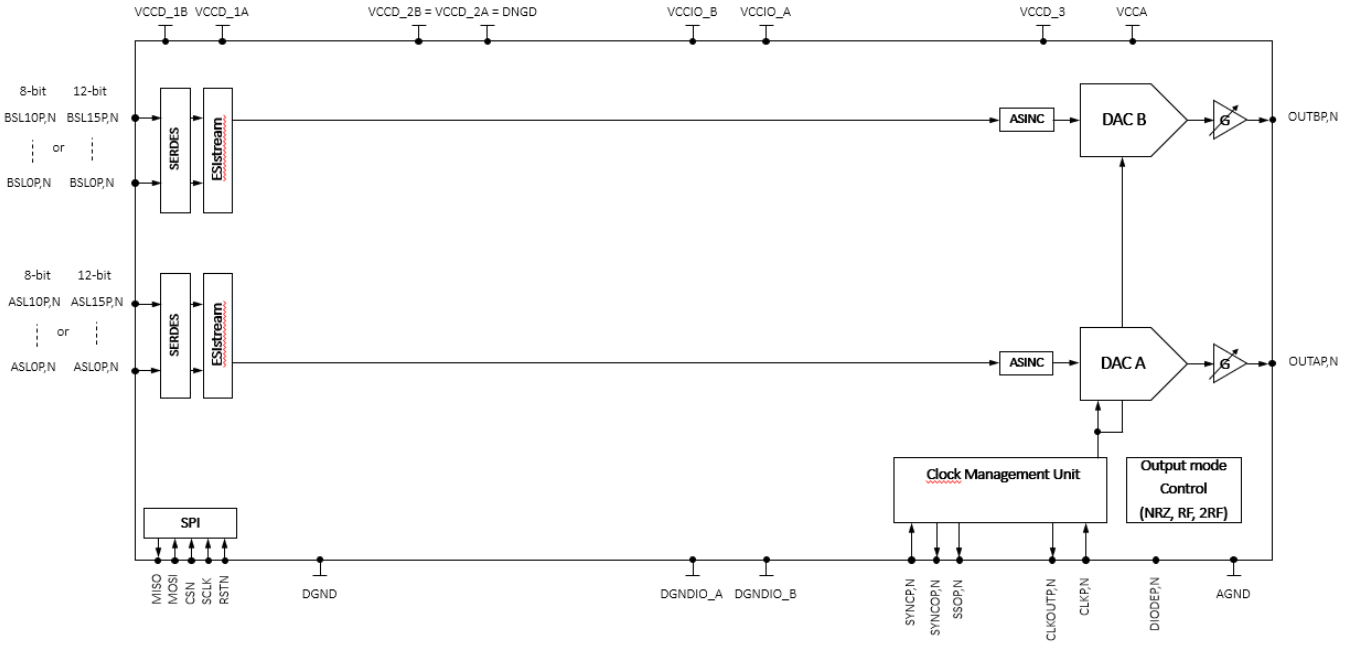


Figure 2: Simplified Block Diagram using Real data

3. DESCRIPTION

The EV8DD700/EV12DD700 has DUAL 8-bit/12-bit DAC cores, converting at 12 GSps (NRZ and RF modes). Conversion rate is still 12 GSps in 2RF mode using an input clock at 24 GHz. Digital data interface is done through a serial link up to 12Gbps, powered by the ESIstream low latency protocol. The DAC embeds digital features like Digital Up Conversion (DUC) with 3 interpolation ratios, Direct Digital Synthesis (DDS), chirp, Beam-Forming, Beam-Hopping and ultra-fast Frequency Hopping. The sinc(x) = sin(x)/x DAC output response can be compensated through the anti Sinc feature (A-SINC).

In addition to classical Non Return to Zero output mode (NRZ), the DAC cores have embedded Radio Frequency (RF) mode and 2RF mode requiring a clock at twice the speed of other modes. Thanks to these output modes, the DAC can directly synthetize frequencies up to 21 GHz without the help of any external up converter, enabling very broadband Software Defined Radios with operation from baseband to Ka-band.

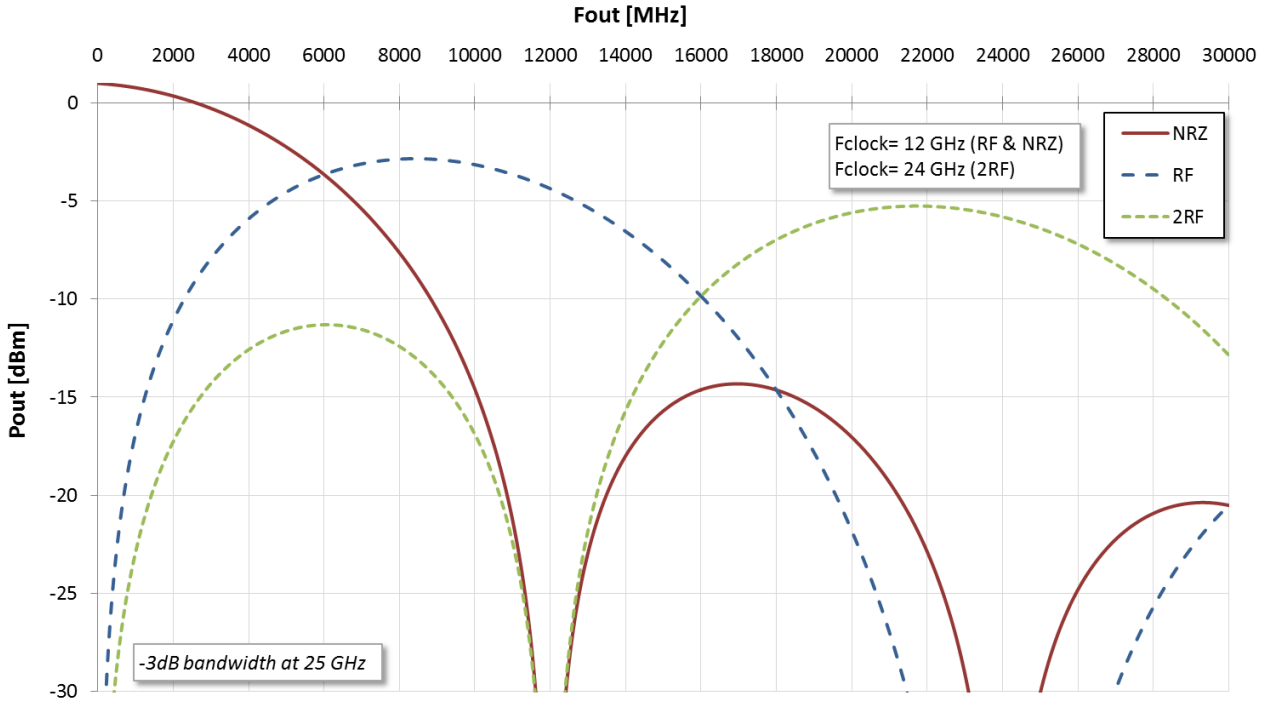


Figure 3: Output DAC response at 12GSps in NRZ and RF mode and 2RF mode with 24GHz clock (include the attenuation due to 25GHz output bandwidth, but does not include additional attenuation due to internal parasitics)

The number of serial lanes (11 HSSLs for the EV8DD700 and 16 HSSLs for the EV12DD700 per core) can be adjusted depending on the mode and the instantaneous bandwidth to be transmitted. Using interpolation and digital upconversion (DUC) allows reduction of the required data stream at DAC input. When DUC is used the data type needs to be complex. When no DUC is used, all serial lanes are used and the data type is real. This is described in the table hereafter.

In NRZ and RF modes, the Nyquist Zone NZ = Fc/2 = Fs/2 (with Fs (sampling rate) = Fc (clock rate) = 12GHz, HSSL speed is 12Gbps)
In 2RF mode, the Nyquist Zone NZ = Fc/4 = Fs/2 (with Fs = 12 GHz and Fc = 24GHz, HSSL speed is 12Gbps)

Table 1. Impact on serial lanes number depending on interpolation ratio

Interpolation Ratio	Instantaneous Bandwidth (GHz)	Number of HSSLs per port	HSSL speed (Gbps)	Data type

		(8-bit/12-bit)		
x1	NZ	11/16	Fs	Real
x4	0.85*NZ/2	6/8	Fs	I+jQ
x8	0.85*NZ/4	3/4	Fs	I+jQ
x16	0.85*NZ/8	2/2	Fs	I+jQ

Table 2. Max sampling rate (GSps) per mode (1)

	Real mode	Interpolation x4	Interpolation x8	Interpolation x16
EV8DD700	10.8	12	12	12
EV12DD700	NA	12	12	12

(1) For NRZ and RF mode, Fc = Fs and for 2RF mode, Fc = 2 Fs

4. SPECIFICATIONS

4.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values (referenced to GND = 0 V), to be applied individually, while other parameters are within specified operating conditions.
Exposure above those conditions may cause permanent damage. Long exposure to maximum ratings may affect device reliability

Table 3. Absolute Maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
Analog supply voltage	V_{CCA}	AGND – 0.3	4	V
Input/Output supply voltage	V_{CCIO}	GNDO – 0.3	2.75	V
Digital supply voltage	V_{CCD}	DGND – 0.3	1.8TBD	V
Serial Link Input peak voltage (with x=0 up to 15)	$\lvert V_{ASLxP} - V_{ASLxN}\rvert$ $\lvert V_{BSLxP} - V_{BSLxN}\rvert$		2.48V (TBC)	Vppdiff
Serial Link Input peak voltage	ASLxP, ASLxN, BSLxP, BSLxN	GNDO – 0.3	V_{CCIO}+ 0.3 (TBC)	V
Clock input swing (mode ON)	$\lvert V_{CLKP} - V_{CLKN}\rvert$		3.2 (TBC)	Vppdiff
Clock input swing (mode OFF)	$\lvert V_{CLKP} - V_{CLKN}\rvert$		See Note 1	Vppdiff
Clock input voltage	V_{CLKP} or V_{CLKN}	AGND – 0.3	V_{CCA}+ 0.3	V
SYNC input swing (mode ON)	$\lvert V_{SYNCP} - V_{SYNCN}\rvert$		4	Vppdiff
SYNC input swing (mode OFF)	$\lvert V_{SYNCP} - V_{SYNCN}\rvert$		See Note 1	Vppdiff
SYNC input peak voltage	V_{SYNCP} or V_{SYNCN}	AGND – 0.3	V_{CCA}+ 0.3	V
SPI input voltage	CSN, SCLK, RSTN, MOSI	DGND - 0.3	V_{CCD} + 0.3 (TBC)	V
Max Junction Temperature	T_{JMAX}		150	°C
Storage Temperature	T_{stg}	-65	150	°C
VDIODEA input voltage to prevent leakage (VDIODEC=GND)	$VDIODE_A$	-0.3	0.30	V
Maximum input current on DIODE	$IDIODE_A$		1	mA

Note:
1. For cold sparing application, see Application Note (TBD)
   All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage

caused by inappropriate handling or storage could range from performance degradation to complete failure.

Input buffers and associated ESD protection have been designed to allow “cold sparing”.

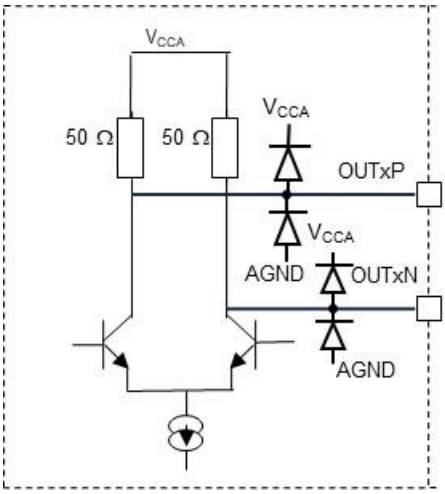


Figure 4: Analog output scheme regarding max ratings

4.2 Recommended conditions of use

Table 4. Recommended conditions of use

Parameter	Symbol	Comments	Recommended Value	Unit
Analog supply voltage	V_{CCA}	Analog Part	3.3	V
Input/Output supply voltage	V_{CCIO}	Input/Output buffers	1.8	V
Digital supply voltage	V_{CCD}	Digital buffers	1.175	V
Clock input power level	P_{CLK} P_{CLKN}		1 (TBC)	dBm
Digital CMOS input	V_D	V_{IL} V_{IH}	0.00 1.8	V
Operating Temperature Range	T_C; T_J		-55 °C <T_C ; T_J< 125 °C	°C

4.3 Electrical parameters characteristics for supplies, Inputs and Outputs

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA}= 3.3 V, V_{CCD} = 1.175 V, V_{CCO} = 1.8 V at ambient temperature with Fs=12 GHz in default mode (Dual DAC, no DUC nor interpolation, with A-SINC compensation, no beamforming), SSO, CLKOUT and SYNCO disabled.
Minimum and Maximum values are given over temperature.

4.3.1 EV8DD700 electrical parameters characteristics for supplies

Table 5. EV8DD700 Electrical characteristics for Supplies

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
RESOLUTION				**8**		**bit**	
POWER REQUIREMENTS							
Power Supply voltage							
- Analog		V_{CCA}	3.20	3.30	3.40	V	
- Input/Output		V_{CCIO}	1.70	1.80	1.90	V	(1)
- Digital		V_{CCD}	1.15	1.175	1.2	V	
Power Supply current in NRZ mode **No digital preprocessing** **Dual / Single DAC mode**							(2)
- Analog		$I_{CCA\_NRZ\_int1}$		1000 / -		mA	
- Input/Output		$I_{CCO\_NRZ\_int1}$		60 / -		mA	
- Digital		$I_{CCD\_NRZ\_int1}$		1450 / -		mA	
Power Supply current in RF mode **No digital preprocessing** **Dual / Single DAC mode**							(2)
- Analog		$I_{CCA\_RF\_int1}$		1050 / 630		mA	
- Input/Output		$I_{CCO\_RF\_int1}$		60 / 35		mA	
- Digital		$I_{CCD\_RF\_int1}$		1450 / 860		mA	
Power Supply current in 2RF mode **No digital preprocessing** **Dual / Single DAC mode**							(2)
- Analog		$I_{CCA\_2RF\_int1}$		TBD / -		mA	
- Input/Output		$I_{CCO\_2RF\_int1}$		TBD / -		mA	
- Digital		$I_{CCD\_2RF\_int1}$		TBD / -		mA	
Power Supply current in NRZ mode **Interpolation by 4** **Dual / Single DAC mode**							(2)
- Analog		$I_{CCA\_NRZ\_int4}$		TBD / -		mA	
- Input/Output							
- no beam forming		$I_{CCO\_NRZ\_int4}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_NRZ\_BFM4}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_NRZ\_int4}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_NRZ\_BFM4}$		TBD / TBD		mA	
Power Supply current in RF mode **Interpolation by 4** **Dual / Single DAC mode**							(2)
- Analog		$I_{CCA\_RF\_int4}$		TBD / -		mA	
- Input/Output							
- no beam forming		$I_{CCO\_RF\_int4}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_RF\_BFM4}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_RF\_int4}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_RF\_BFM4}$		TBD / TBD		mA	

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Power Supply current in 2RF mode **Interpolation by 4** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_2RF\_int4}$		TBD / TBD		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_2RF\_int4}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_2RF\_BFM4}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_2RF\_int4}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_2RF\_BFM4}$		TBD / TBD		mA	
Power Supply current in NRZ mode **Interpolation by 8** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_NRZ\_int8}$		TBD / -		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_NRZ\_int8}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_NRZ\_BFM8}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_NRZ\_int8}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_NRZ\_BFM8}$		TBD / TBD		mA	
Power Supply current in RF mode **Interpolation by 8** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_RF\_int8}$		TBD / -		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_RF\_int8}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_RF\_BFM8}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_RF\_int8}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_RF\_BFM8}$		TBD / TBD		mA	
Power Supply current in 2RF mode **Interpolation by 8** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_2RF\_int8}$		TBD / -		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_2RF\_int8}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_2RF\_BFM8}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_2RF\_int8}$		TBD / TBD		mA	
beam forming		$I_{CCD\_2RF\_BFM8}$		TBD / TBD		mA	
Power Supply current in NRZ mode **Interpolation by 16** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_NRZ\_int16}$		TBD / -		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_NRZ\_int16}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_NRZ\_BFM16}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_NRZ\_int16}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_NRZ\_BFM16}$		TBD / TBD		mA	
Power Supply current in RF mode **Interpolation by 16** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_RF\_int16}$		TBD / -		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_RF\_int16}$		TBD / TBD		mA	
- beam forming		$I_{CCO\_RF\_BFM16}$		TBD / TBD		mA	
- Digital							
- no beam forming		$I_{CCD\_RF\_int16}$		TBD / TBD		mA	
- beam forming		$I_{CCD\_RF\_BFM16}$		TBD / TBD		mA	

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Power Supply current in 2RF mode **Interpolation by 16** **Dual / Single DAC mode** - Analog - Input/Output - no beam forming - beam forming - Digital - no beam forming - beam forming		 $I_{CCA\_2RF\_int116}$ $I_{CCO\_2RF\_int16}$ $I_{CCO\_2RF\_BFM16}$ $I_{CCD\_2RF\_int16}$ $I_{CCD\_2RF\_BFM16}$		 TBD / - TBD / TBD TBD / TBD TBD / TBD TBD / TBD		 mA mA mA mA mA	 (2)
Power Supply current standby mode **No digital preprocessing** **Dual / Single DAC mode** - Analog (NRZ and RF mode) - Analog (2RF mode with Fc=24 GHz) - Input/Output - Digital		 I_{CCA} I_{CCA} I_{CCIO} I_{CCD}		 TBD / - TBD / TBD TBD / - TBD / TBD		 mA mA mA mA	
Power dissipation in NRZ mode **Dual / Single DAC mode** **Full power mode without beam forming** - no interpolation - interpolation x4 - interpolation x8 - interpolation x16 **Full power mode with beam forming** - interpolation x4 - interpolation x8 - interpolation x16		 $P_{D\ NRZ}$		 5.1 / - TBD / TBD TBD / TBD TBD / TBD TBD / TBD TBD / TBD TBD / TBD		 W W W W W W W	 (2)
Power dissipation in RF mode **Dual / Single DAC mode** **Full power mode without beam forming** - no interpolation - interpolation x4 - interpolation x8 - interpolation x16 **Full power mode with beam forming** - interpolation x4 - interpolation x8 - interpolation x16		 $P_{D\ RF}$		 5.3 / 3.3 TBD / TBD TBD / TBD TBD / TBD TBD / TBD TBD / TBD TBD / TBD		 W W W W W W W	 (2)
Power dissipation (2RF mode) **Dual / Single DAC mode** **Full power mode without beam forming** - no interpolation - interpolation x4 - interpolation x8 - interpolation x16 **Full power mode with beam forming** - interpolation x4 - interpolation x8 - interpolation x16		 $P_{D\ 2RF}$		 TBD / - TBD / TBD TBD / TBD TBD / TBD TBD / TBD TBD / TBD TBD / TBD		 W W W W W W W	 (2) (3)
Power dissipation in stand-by mode		$P_{D\ std\text{-}by}$		TBD / 0.5		W	
Maximum number of power-ups		NbPWRup	1 million				(4)

Note:

1. Different V_{CCD} are used for dedicated blocks (V_{CCD1}, V_{CCD2} and V_{CCD3}).
2. Current and power consumption values make the hypothesis that unused features are completely powered down in grounding some VCC values at board level.
3. Power consumption makes the assumptions that unused output HSSLs are powered OFF. Refer to Table 21, Table 56 and Table 57.
4. Maximum number of power-ups is limited by the maximum number of OTP reading.

4.3.2 EV12DD700 electrical parameters characteristics for supplies

Table 6. EV12DD700 Electrical characteristics for Supplies

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
RESOLUTION				**12**		**bit**	
POWER REQUIREMENTS							
Power Supply voltage - Analog - Input/Output - Digital		 V_{CCA} V_{CCIO} V_{CCD}	 3.20 1.70 1.15	 3.30 1.80 1.175	 3.40 1.90 1.2	 V V V	(1)
Power Supply current in NRZ mode **No digital preprocessing** **Dual / Single DAC mode** - Analog - Input/Output - Digital		 $I_{CCA\_NRZ\_int1}$ $I_{CCO\_NRZ\_int1}$ $I_{CCD\_NRZ\_int1}$		 NA NA NA		 mA mA mA	(2)
Power Supply current in RF mode **No digital preprocessing** **Dual / Single DAC mode** - Analog - Input/Output - Digital		 $I_{CCA\_RF\_int1}$ $I_{CCO\_RF\_int1}$ $I_{CCD\_RF\_int1}$		 NA NA NA		 mA mA mA	(2)
Power Supply current in 2RF mode **No digital preprocessing** **Dual / Single DAC mode** - Analog - Input/Output - Digital		 $I_{CCA\_2RF\_int1}$ $I_{CCO\_2RF\_int1}$ $I_{CCD\_2RF\_int1}$		 NA NA NA		 mA mA mA	(2)
Power Supply current in NRZ mode **Interpolation by 4** **Dual / Single DAC mode** - Analog - Input/Output - no beam forming - beam forming - Digital - no beam forming - beam forming		 $I_{CCA\_NRZ\_int4}$ $I_{CCO\_NRZ\_int4}$ $I_{CCO\_NRZ\_BFM4}$ $I_{CCD\_NRZ\_int4}$ $I_{CCD\_NRZ\_BFM4}$		 1000 / 650 60 / 30 35 / - 2500 / 1300 2300 / -		 mA mA mA mA mA	(2)
Power Supply current in RF mode **Interpolation by 4** **Dual / Single DAC mode** - Analog - Input/Output - no beam forming - beam forming - Digital - no beam forming - beam forming		 $I_{CCA\_RF\_int4}$ $I_{CCO\_RF\_int4}$ $I_{CCO\_RF\_BFM4}$ $I_{CCD\_RF\_int4}$ $I_{CCD\_RF\_BFM4}$		 1095 / 670 60 / 30 35 / - 2500 / 1300 2300 / -		 mA mA mA mA mA	(2)
Power Supply current in 2RF mode **Interpolation by 4** **Dual / Single DAC mode** - Analog - Input/Output - no beam forming - beam forming - Digital - no beam forming - beam forming		 $I_{CCA\_2RF\_int4}$ $I_{CCO\_2RF\_int4}$ $I_{CCO\_2RF\_BFM4}$ $I_{CCD\_2RF\_int4}$ $I_{CCD\_2RF\_BFM4}$		 1140 / 690 60 / 30 35 / - 2500 / 1300 2300 / -		 mA mA mA mA mA	(2)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Power Supply current in NRZ mode **Interpolation by 8** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_NRZ\_int8}$		1050 / 650		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_NRZ\_int8}$		36 / 20		mA	
- beam forming		$I_{CCO\_NRZ\_BFM8}$		25 / -		mA	
- Digital							
- no beam forming		$I_{CCD\_NRZ\_int8}$		2250 / 1160		mA	
- beam forming		$I_{CCD\_NRZ\_BFM8}$		2110 / -		mA	
Power Supply current in RF mode **Interpolation by 8** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_RF\_int8}$		1095 / 670		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_RF\_int8}$		36 / 20		mA	
- beam forming		$I_{CCO\_RF\_BFM8}$		25 / -		mA	
- Digital							
- no beam forming		$I_{CCD\_RF\_int8}$		2250 / 1160		mA	
- beam forming		$I_{CCD\_RF\_BFM8}$		2110 / -		mA	
Power Supply current in 2RF mode **Interpolation by 8** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_2RF\_int8}$		1140 / 690		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_2RF\_int8}$		36 / 20		mA	
- beam forming		$I_{CCO\_2RF\_BFM8}$		25 / -		mA	
- Digital							
- no beam forming		$I_{CCD\_2RF\_int8}$		2250 / 1160		mA	
beam forming		$I_{CCD\_2RF\_BFM8}$		2110 / -		mA	
Power Supply current in NRZ mode **Interpolation by 16** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_NRZ\_int16}$		1050 / 650		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_NRZ\_int16}$		25 / 15		mA	
- beam forming		$I_{CCO\_NRZ\_BFM16}$		20 / -		mA	
- Digital							
- no beam forming		$I_{CCD\_NRZ\_int16}$		2050 / 1060		mA	
- beam forming		$I_{CCD\_NRZ\_BFM16}$		2000 / -		mA	
Power Supply current in RF mode **Interpolation by 16** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_RF\_int16}$		1095 / 670		mA	
- Input/Output							
- no beam forming		$I_{CCO\_RF\_int16}$		25 / 15		mA	(2)
- beam forming		$I_{CCO\_RF\_BFM16}$		20 / -		mA	
- Digital							
- no beam forming		$I_{CCD\_RF\_int16}$		2050 / 1060		mA	
- beam forming		$I_{CCD\_RF\_BFM16}$		2000 / -		mA	
Power Supply current in 2RF mode **Interpolation by 16** **Dual / Single DAC mode**							
- Analog		$I_{CCA\_2RF\_int116}$		1140 / 690		mA	
- Input/Output							(2)
- no beam forming		$I_{CCO\_2RF\_int16}$		25 / 14		mA	
- beam forming		$I_{CCO\_2RF\_BFM16}$		20 / -		mA	
- Digital							
- no beam forming		$I_{CCD\_2RF\_int16}$		2050 / 1060		mA	
- beam forming		$I_{CCD\_2RF\_BFM16}$		2000 / --		mA	

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Power Supply current standby mode **No digital preprocessing** **Dual / Single DAC mode** - Analog (NRZ and RF mode) - Analog (2RF mode with Fc=24 GHz) - Input/Output - Digital		 I_{CCA} I_{CCA} I_{CCIO} I_{CCD}		 70 / - 70 / - 10 TBD / TBD		 mA mA mA mA	
Power dissipation in NRZ mode **Dual / Single DAC mode** **Full power mode without beam forming** - no interpolation - interpolation x4 - interpolation x8 - interpolation x16 **Full power mode with beam forming** - interpolation x4 - interpolation x8 - interpolation x16		 $P_{D\ NRZ}$		 5.7 / 3.3 6.55 / 3.75 6.2 / 3.55 5.95 / 3.42 6.25 / - 6 / - 5.85 / -		 W W W W W W W	 (2)
Power dissipation in RF mode **Dual / Single DAC mode** **Full power mode without beam forming** - no interpolation - interpolation x4 - interpolation x8 - interpolation x16 **Full power mode with beam forming** - interpolation x4 - interpolation x8 - interpolation x16		 $P_{D\ RF}$		 5.85 / 3.35 6.7 / 3.82 6.35 / 3.62 6.1 / 3.5 6.4 / - 6.15 / - 6 / -		 W W W W W W W	 (2)
Power dissipation (2RF mode) **Dual / Single DAC mode** **Full power mode without beam forming** - no interpolation - interpolation x4 - interpolation x8 - interpolation x16 **Full power mode with beam forming** - interpolation x4 - interpolation x8 - interpolation x16		 $P_{D\ 2RF}$		 6 / 3.4 6.85 / 3.9 6.5 / 3.7 6.25 / 3.58 6.55 / - 6.3 / - 6.15 / -		 W W W W W W W	 (2) (3)
Power dissipation in stand-by mode		$P_{D\ std\text{-}by}$		< 0.5		W	
Maximum number of power-ups		NbPWRup	1 million				(4)

Note:

1. Different V_{CCD} are used for dedicated blocks (V_{CCD1}, V_{CCD2} and V_{CCD3}).
2. Current and power consumption values make the hypothesis that unused features are completely powered down in grounding some VCC values at board level.
3. Power consumption makes the assumptions that unused output HSSLs are powered OFF. Refer to Table 21, Table 56 and Table 57.
4. Maximum number of power-ups is limited by the maximum number of OTP reading.

4.3.3 Electrical parameters characteristics for Inputs and Ouputs

Table 7. Electrical characteristics for Inputs and Outputs

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
ANALOG OUTPUTS							
Common mode compatibility for analog outputs			AC or DC				
Output Common Mode		V_{OCM}	2.3	2.45	2.6	V	

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Full Scale Input Voltage range on **each differential ended output**		V_{OUT-pp}		1000		mVpp Diff	
Analog Output Full Scale power Level (NRZ mode close to DC assuming on board 100 Ω differential load)		P_{OUT}		+1		dBm	
Output Resistance (differential)		R_{OUT}	80	100	120	Ω	(1)
Cross-talk between outputs • Fout=2 GHz • Fout=4 GHz • Fout=5 GHz • Fout=7 GHz • Fout=14 GHz • Fout=20 GHz				 70 70 65 60 55 50		dB	
CLOCK INPUTS							
Source Type		Low Phase noise Differential Sinewave					
DAC intrinsic clock jitter ▪ NRZ and RF modes ▪ 2RF mode				 90 70		fs_{rms}	
Spectral requirement for Fc ≥ 12 GHz ▪ 100 Hz from clock frequency ▪ 10 kHz from clock frequency ▪ 10 MHz from clock frequency ▪ 1 GHz from clock frequency					 -70 -100 -150 -165	dBc/Hz	
Clock input common mode voltage		V_{CM}	2.6	2.7	2.8	V	
Clock input power level in 100 Ω		$P_{CLK, CLKN}$	-3	+1	+7	dBm	
Clock input voltage on each single ended input		V_{CLK} or V_{CLKN}	±158	±250	±500	mV	
Clock input voltage into 100 Ω differential clock input		$\lvert V_{CLKP} - V_{CLKN} \rvert$	0.632	1	2	Vpp	(2)
Clock input minimum slew rate (square or sinewave clock)		SR_{CLK}	8	12		GV/s	
Clock input capacitance (die + package)		C_{CLK}		1		pF	
Clock input resistance (differential)		R_{CLK}	80	100	120	Ω	(1)
12 GHz Clock Jitter (max. allowed on clock source, CW pattern) in NRZ and RF modes		Jitter			100	fs_{rms}	
24 GHz Clock Jitter (max. allowed on clock source, CW pattern) in 2RF mode		Jitter			60	fs_{rms}	
Clock Duty Cycle		Duty Cycle	45	50	55	%	
12 GHz Clock input matching		S11			-13	dB	
24 GHz Clock input matching		S11			-8	dB	
CLOCK output (CLKOUT)							
Logic Compatibility			CML				
Output levels (swing adjust off = full swing) 50 Ω transmission lines, 100 Ω (2 x50 Ω) differential termination ▪ Logic low ▪ Logic high ▪ Differential output ▪ Common mode		 V_{OL} V_{OH} V_{OH}- V_{OL} V_{OCM}		 V_{CCA} – 0.45 V_{CCA} – 0.05 400 V_{CCA} - 0.25		 V V mVp V	

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Output levels (swing adjust on = reduced swing) 50 Ω transmission lines, 100 Ω (2 x50 Ω) differential termination ▪ Logic low ▪ Logic high ▪ Differential output ▪ Common mode		 V_{OL} V_{OH} V_{OH}- V_{OL} V_{OCM}		 V_{CCA} – 0.25 V_{CCA} – 0.05 200 V_{CCA}- 0.15		 V V mVp V	
SYNC, SYNCN Signal LVDS							
Input Voltages to be applied ▪ Swing ▪ Common Mode		V_{IH}- V_{IL} V_{ICM}	100 1.125	350 1.25	450 1.8	mV V	
SYNCP, SYNCN input capacitance		C_{SYNC}		1		pF	
SYNCP, SYNCN input resistance		R_{SYNC}	80	100	120	Ω	
Input digital signals (CSN, SCLK, RSTN, MOSI, DIG_INx, DIG_MODEx) CMOS							
Low level threshold of Schmitt trigger		Vtminusc			0.35 * V_{CCIO}	V	
High level threshold of Schmitt trigger		Vtplusc	0.65 * V_{CCIO}			V	
CMOS Schmitt trigger hysteresis		Vhystc	0.10 * V_{CCIO}			V	
CMOS low level input current (Vinc=0 V) ▪ CSN, RSTN ▪ Other pins		lilc			50 0.300	µA	
CMOS high level input current (Vinc=V_{CCIO} max) ▪ CSN, RSTN ▪ Other pins		lihc			 15 16	µA	(3)
Output digital signal (MISO, DIG_OUTx) CMOS							
CMOS low level output voltage (Iolc = 3 mA)		Volc			0.20 * V_{CCIO}	V	
CMOS high level output voltage (Iohc = 3 mA)		Vohc	0.8 * V_{CCIO}			V	
LVDS OUTPUTS (SSO, SYNCO)							
Logic Compatibility			LVDS				
Output levels (full swing) 50 Ω transmission lines, 100 Ω (2 x 50 Ω) differential termination ▪ Logic low ▪ Logic high ▪ Differential output ▪ Common mode		 V_{OL} V_{OH} V_{OH}- V_{OL} V_{OCM}	 1.25 250 1.125	 350 1.25	 1.25 450 1.375	 V V mVpdiff V	
Output levels (reduced swing) ▪ Differential output ▪ Common mode		V_{OH}- V_{OL} V_{OCM}	165 1.1	235	300 1.4	mVpdiff V	
SERIAL LINK INPUTS (ASLx,BSLx) with x=0 up to 15 for EV12DD700 and x = 0 up to 10 for EV8DD700							
Logic Compatibility			CML				
input levels (swing adjust off) 50 Ω transmission lines, 100 Ω (2 x 50 Ω) differential termination ▪ Differential input ▪ Common mode		 V_{IH}- V_{IL} V_{ICM}	 100 1.32	 1.4	 500 1.48	 mVp V	

Note:

1. For optimal performance in term of VSWR, Board input impedance must be 50Ω± 10%
2. Maximum clock input voltage without stress when power is OFF is 2Vpp differential
3. SPI load on MOSI 25 pF max

4.4 Converter Characteristics

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA}= 3.3V, V_{CCD} = 1.05V, V_{CCO} = 1.8 V at ambient with Fs=12GHz in default mode (Dual DAC, no DUC nor interpolation, with A-SINC compensation, no beamforming), SSO, CLKOUT and SYNCO disabled.
Minimum and Maximum values are given over temperature.

Table 8. Low frequency characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
DC ACCURACY							
Gain central value		Go	-0.5	1	2.5	dBm/dBFs	(1)
Gain variation versus temperature		G(T)	- 0.5		+0.5	dB	
DC offset		OFFSET	-0.25	0	+0.25	LSB	
Fsampling = 12 GSps per core, Fout = 30 MHz, 0 dBFS							
DNLrms		DNLrms			0.25	LSB	
Differential non linearity		DNL	-0.8		0.8	LSB	
INLrms		INLrms			0,5	LSB	
Integral non linearity		INL	TBD		TBD	LSB	

Note: 1. Gain central value is measured at Fout = 30 MHz. This value corresponds to the maximum deviation from part to part of different wafer batches before gain tuning by SPI register (see 11.1).

Table 9. AC Analog Output Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
AC ANALOG OUTPUTS							
Full Power Output Bandwidth		FPBW		25		GHz	
Output power • Fout=1.0GHz NRZ mode • Fout=2.5GHz NRZ mode • Fout=3.7GHz NRZ mode • Fout=7.5GHz RF mode • Fout=11.5GHz RF mode • Fout=18.5GHz 2RF mode (Fc=24 GHz) • Fout=21.0GHz 2RF mode (Fc=24 GHz)		Pout $_{th}$		-1,5 -2.3 -3.5 -8.5 -8.6 -15.4 -14.9		dBm	(1)
Output impedance matching / reflection coefficient • Up to 6 GHz • 6 to 12 GHz • 12 to 18 GHz • 18 to 21 GHz		S11		-14 -8 -13 -13		dB	

Note:
1. Refer to Figure 3.

Table 10. Dynamic Performance

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
DYNAMIC PERFORMANCE							
Spurious Free Dynamic Range Single tone at output level 0 dBFS / Fc=12GHz • Fout=1.0GHz NRZ mode • Fout=3.7GHz NRZ mode • Fout=7.5GHz RF mode • Fout=11.5GHz RF mode • Fout=14GHz RF mode Single tone at output level 0 dBFS / Fc=24GHz • Fout=18.5GHz 2RF mode • Fout=21GHz 2RF mode		|SFDR|		66 65 54 50 TBD 52 58		dBc	(2)
Clock related spurs • Fc = 12 GHz ○ Fout=Fc/4 ○ Fout=Fc/2 ○ Fout=3Fc/4 ○ Fout=Fc • Fc = 24 GHz ○ Fout=Fc/8 ○ Fout=Fc/4 ○ Fout=Fc/2				-80 (TBC) -96 -74 -56 -74 (TBC) -69 (TBC) -44 (TBC)		dBm	(1)
Noise Spectral Density Single tone at output level 0 dBFS / Fc=12GHz • Fout=1.0GHz NRZ mode • Fout=3.7GHz NRZ mode • Fout=7.5GHz RF mode • Fout=11.5GHz RF mode • Fout=14GHz RF mode Single tone at output level 0 dBFS / Fc=24GHz • Fout=18.5GHz 2RF mode • Fout=21GHz 2RF mode		NSD		-156.8(TBC) -154.8(TBC) -154.8(TBC) -154.8(TBC) -154.8(TBC) -154.0(TBC) -154.0(TBC)		dBm/Hz	
Noise Power Ratio (NPR) @ optimum loading factor on 80% of Instantaneous bandwidth for real data mode • 1st Nyquist NRZ (Fs = 12GHz) • 2nd Nyquist RF (Fs = 12GHz) • 3rd Nyquist RF (Fs = 12GHz) • 4th Nyquist 2RF (Fs = 24GHz)		NPR		8-bit / 12-bit TBD / 45 37 / 40 TBD / 40 TBD / 35		dB	
SNR …. • 1st Nyquist NRZ (Fs = 12GHz) • 2nd Nyquist RF (Fs = 12GHz) • 3rd Nyquist RF (Fs = 12GHz) • 4th Nyquist 2RF (Fs = 24GHz)		SNR		8-bit / 12-bit TBD / 54 46 / 49 TBD / 49 TBD / 44		dB	(3)
ENOB …. • 1st Nyquist NRZ (Fs = 12GHz) • 2nd Nyquist RF (Fs = 12GHz) • 3rd Nyquist RF (Fs = 12GHz) • 4th Nyquist 2RF (Fs = 24GHz)		ENOB		8-bit / 12-bit TBD / 8.7 7.3 / 7 .8 TBD / 7.8 TBD / 7		bit	(4)

Note:

1. In NRZ and RF modes, Fc = Fs, while in 2RF mode Fs=Fc/2
2. Could be improved with SDA_MUX21, A_LOOP_CFG, B_LOOP_CFG adjustment and Vccd3_min
3. $SNR_{[dB]} = NPR_{[dB]} + |LF_{[dB]}| - 3$
4. ENOB = (SNR- 1.76) / 6.02

4.5 Transient and Switching Characteristics

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA}= 3.3V, V_{CCD} = 1.05V, V_{CCO} = 1.8 V at ambient with Fs = 12GHz in default mode (Dual DAC, no DUC nor interpolation, with A-SINC compensation, no beamforming), CLKOUT and SYNCO disabled.
Minimum and Maximum values are given over temperature.

Table 11. Transient characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
TRANSIENT PERFORMANCE							
Serial link Bit Error Rate at 12 Gbps		BER		10^{-15}		Error/ sample	
DAC rise time (10%- 90%)		RT		15		ps	(1)

Note: 1. RT is correlated with FPBW, RT * FPBW ≈ 0.35.

Table 12. Switching characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
SWITCHING PERFORMANCE AND CHARACTERISTICS (Any Output Mode)							
External Clock frequency for performances NRZ and RF modes 2RF mode		F_c	1 (TBC) 2 (TBC)		12 24	GHz GHz	(6)
Serial link speed NRZ and RF modes 2RF mode		F_{HSSL}	2 (TBC) 2 (TBC)	F_c $F_c/2$		Gbps Gbps	
Conversion Clock to CLKOUT delay		Tclkout		TBD		ps	
Max crosstalk from CLKOUT on clock input signal@ 12Gbps		XTALK_CKO2CK			-40	dB	
CLKOUT jitter		Jitterclkout		60		fs_{rms}	
Digital reset duration			10			µs	
DAC settling time after power up		TS		TBD		µs	
SWITCHING PERFORMANCE AND CHARACTERISTICS (SYNC)							
Minimum SYNC pulse width		TSYNC		TBD		External Clock cycles	
Minimum SYNC rise time		TR_{SYNC}			400	ps	
SWITCHING PERFORMANCE AND CHARACTERISTICS (SSO, SYNCO)							
Recommended SSO output frequency		F_{SSO}		375		MHz	(5)
Output rise time (20%-80%)		TR		70		ps	(2)
Output fall time (20%-80%)		TF		70		ps	(2)
SSO and SYNCO pipeline delay		TPD_{SSO}		TBD		External Clock cycles	(4)
SWITCHING PERFORMANCE AND CHARACTERISTICS (Serial input)							
Output Data delay (pipeline + delay)		TPD		TBD		External Clock cycles	(4)
		TOD		TBD		ps	
Total jitter @ 12Gbps		2XT1		61.6		ps	(3)
Minimum buffer amplitude time @ 12Gbps		XT2		44		ps	(3)
Maximum buffer amplitude @ 12Gbps		YT1		550		mV	(3)
Minimum buffer amplitude @ 12Gbps		YT2		100		mV	(3)
Skew between serial input signal P and N		Tskew			0.6	ps	(3)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
crosstalk between xSL1 and xSL0@ 12Gbps (x= A, or B)		XTALK_SL2SL		-40	-20	dB	(3)
Max crosstalk between input serial link and analog output signal @ 12Gbps		XTALK_SL2IN			-80	dB	(3)
LATENCY							
No interpolation A-SINC OFF No interpolation A-SINC ON		LAT_DUC_OFF		886 919		External Clock cycles	(4)
Interpolation by 4 A-SINC OFF • no beamforming • beamforming Interpolation by 4 A-SINC ON • no beamforming • beamforming		LAT_INT4		1379 1579 1412 1612		External Clock cycles	(4)
Interpolation by 8 A-SINC OFF • no beamforming • beamforming Interpolation by 8 A-SINC ON • no beamforming • beamforming		LAT_INT8		1779 2171 1812 2204		External Clock cycles	(4)
Interpolation by 16 A-SINC OFF • no beamforming • beamforming Interpolation by 16 A-SINC ON • no beamforming • beamforming		LAT_INT16		2579 3355 2612 3388		External Clock cycles	(4)

Notes: 1. See Definition of Terms.
2. PCB line 25 cm
3. PCB line 25 cm
4. When used in 2RF mode, unit is twice the external clock cycles
5. SSO frequency is linked to the clock input frequency and can be adjusted. Refer to section 11.4.
6. Sampling frequency Fs = Fc in NRZ and RF mode, while in 2RF mode Fs = Fc/2

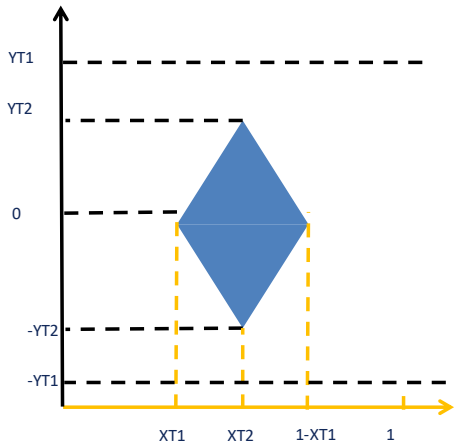


Figure 5 - Serial link eye diagram

Table 13. SPI Timing characteristics

Parameter	Test Level	Symbol	Value			Unit	Note
			Min	Typ	Max		
RSTN pulse length		T_{RSTN}	10			µs	
SCLK frequency		F_{SCLK}			70	MHz	
CSN to SCLK delay		$T_{CSN-SCLK}$	0.5			T_{SCLK}	
MOSI setup time		T_{setup}	3			ns	

Parameter	Test Level	Symbol	Value			Unit	Note
			Min	Typ	Max		
MOSI hold time		T_{hold}	3			ns	
MISO output delay		T_{delay}			7	ns	(1)

Note:

1. Output load on MOSI 25 pF

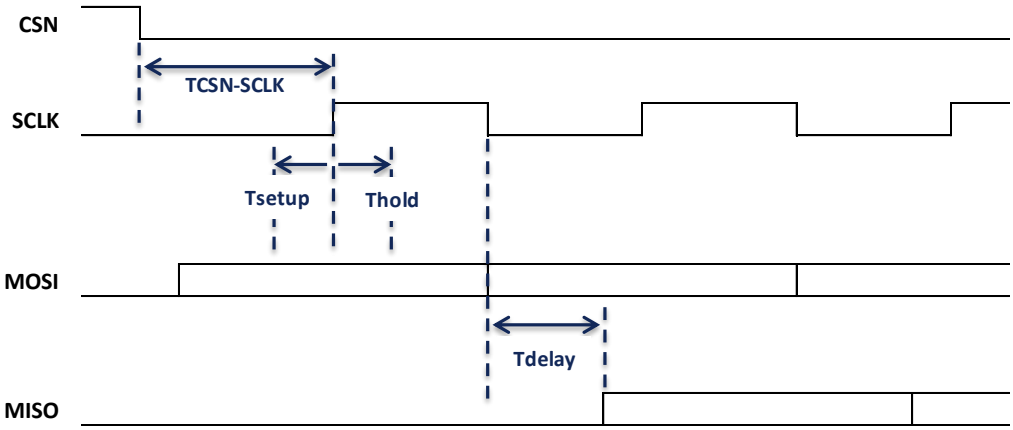


Figure 6 - SPI timing diagram

4.6 Digital Output Coding

Table 14. DAC Digital output coding table

Binary MSB (bit 11).....LSB (bit 0)		Differential Analog output
Unsigned (1)	Signed	
0000 0000 0000	1000 0000 0000	-500mV
0100 0000 0000	1100 0000 0000	-250mV
0110 0000 0000	1110 0000 0000	-125mV
0111 1111 1111	1111 1111 1111	-0.122mV
1000 0000 0000	0000 0000 0000	0.122mV
1010 0000 0000	0010 0000 0000	+125mV
1100 0000 0000	0100 0000 0000	+250mV
1111 1111 1111	0111 1111 1111	+500mV

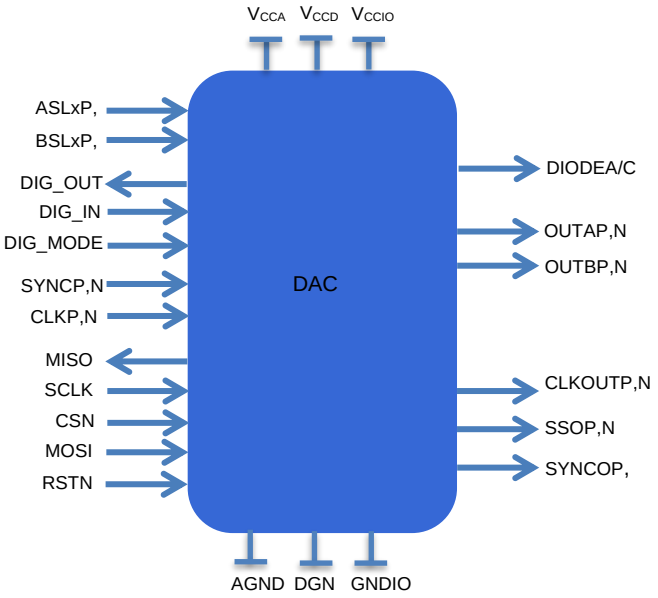
Note: 1. Not possible when DUC is enabled. Unsigned is the default configuration when DUC is disabled.

5. PIN CONFIGURATION AND FUNCTIONS DESCRIPTION

5.1 Pin descriptions

Table 15. Pin descriptions

Name	Function
V_{CCA}	Analog Power Supply
V_{CCD} : V_{CCD_1B} V_{CCD_1A} V_{CCD_2B} V_{CCD_2A} V_{CCD_3}	Digital Power Supply (different pin groups for power down on used digital features): V_{CCD_1B}: Supply for HSSLs, ESIstream (core B) and SPI interface, DIG_OUT0 & 1 V_{CCD_1A}: Supply for HSSLs, ESIstream (core A), DIG_INx, DIG_MODx, DIG_OUT2 & 3 V_{CCD_2B}: DUC supply for core B V_{CCD_2A}: DUC supply for core A. V_{CCD_3}: Analog blocks supply (always switched ON)
V_{CCIO_B} V_{CCIO_A}	Input/Output buffer Power Supply
AGND	Analog Ground
DGND	Digital Ground
GND_{IO_B} GND_{IO_A}	Ground for Input/Output buffer
OUTBP, OUTBN	Differential Analog output for DAC B
OUTAP, OUTAN	Differential Analog output for DAC A
CLKP,CLKN	Differential Clock Input
ASLxP, ASLxN	Channel A input (CML), serial link x (0..15 for 12-bit and 0..10 for 8-bit)
BSLxP, BSLxN	Channel B input (CML), serial link x (0..15 for 12-bit and 0..10 for 8-bit)
SSOP, SSON	Slow Synchro Output clock
DIODEA, DIODEC	Diode Anode and Cathode Inputs for die junction temperature monitoring
CLKOUTP, CLKOUTN	Differential output clock (copy of CLK)
SYNCP, SYNCN	LVDS input: Synchronization of internal clocks
SYNCOP, SYNCON	Synchro output, resynchronized SYNC signal



DIG_MODEx	Digital input
DIG_INx	Digital input
DIG_OUTx	Flag output for serial links control
CSN	SPI Chip Select Input (Active Low)
RSTN	SPI Asynchronous Reset Input (Active Low)
SCLK	SPI Input Clock
MOSI	SPI input Data (Master Out Slave In)
MISO	SPI Output Data (Master In Slave Out)

5.2 Pinout top view

5.2.1 EV8DD700 pinout top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		GNDIOA	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	AGND	AGND	AGND	SSON	SSOP	AGND	AGND	AGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	GNDIOB		A
B	GNDIOA	GNDIOA	DNC	DNC	GNDIOA	VCCD2A	DGND	AGND	SYNCON	SYNCOP	AGND	AGND	SYNCP	SYNCN	AGND	DGND	VCCD2B	GNDIOB	DNC	DNC	GNDIOB	GNDIOB	B
C	DNC	DNC	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	DNC	DNC	C
D	GNDIOA	GNDIOA	DNC	DNC	GNDIOA	VCCD2A	DGND	AGND	CLK OUTN	CLK OUTP	AGND	AGND	CLKP	CLKN	AGND	DGND	VCCD2B	GNDIOB	DNC	DNC	GNDIOB	GNDIOB	D
E	DNC	DNC	GNDIOA	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	GNDIOB	DNC	DNC	E
F	GNDIOA	GNDIOA	ASL10P	ASL10N	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	DGND	AGND	AGND	DGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	BSL10N	BSL10P	GNDIOB	GNDIOB	F
G	DNC	DNC	GNDIOA	GNDIOA	VCCIOA	VCCIOA	VCCIOA	VCCIOA	VCCD2A	DGND	AGND	AGND	DGND	VCCD2B	VCCIOB	VCCIOB	VCCIOB	VCCIOB	GNDIOB	GNDIOB	DNC	DNC	G
H	GNDIOA	GNDIOA	ASL8P	ASL8N	GNDIOA	VCCIOA	DGND	VCCD1A	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	VCCD1B	DGND	VCCIOB	GNDIOB	BSL8N	BSL8P	GNDIOB	GNDIOB	H
J	ASL9P	ASL9N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	VCCD1A	DGND	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	DGND	VCCD1B	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL9N	BSL9P	J
K	GNDIOA	GNDIOA	ASL6P	ASL6N	GNDIOA	GNDIOA	DGND	VCCD1A	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	VCCD1B	DGND	GNDIOB	GNDIOB	BSL6N	BSL6P	GNDIOB	GNDIOB	K
L	ASL7P	ASL7N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	DGND	VCCD1A	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	VCCD1B	DGND	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL7N	BSL7P	L
M	GNDIOA	GNDIOA	ASL4P	ASL4N	GNDIOA	GNDIOA	DGND	VCCD1A	DGND	VCCD2A	DGND	DGND	VCCD2B	DGND	VCCD1B	DGND	GNDIOB	GNDIOB	BSL4N	BSL4P	GNDIOB	GNDIOB	M
N	ASL5P	ASL5N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	DGND	VCCD1A	DGND	AGND	VCCA	VCCA	AGND	DGND	VCCD1B	DGND	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL5N	BSL5P	N
P	GNDIOA	GNDIOA	ASL2P	ASL2N	GNDIOA	VCCIOA	VCCD1A	DGND	AGND	AGND	VCCA	VCCA	AGND	AGND	DGND	VCCD1B	VCCIOB	GNDIOB	BSL2N	BSL2P	GNDIOB	GNDIOB	P
R	ASL3P	ASL3N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	DGND	AGND	AGND	AGND	VCCD3	VCCD3	AGND	AGND	AGND	DGND	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL3N	BSL3P	R
T	GNDIOA	GNDIOA	ASL0P	ASL0N	GNDIOA	GNDIOA	GNDIOA	VCCA	AGND	VCCA	AGND	AGND	VCCA	AGND	VCCA	GNDIOB	GNDIOB	GNDIOB	BSL0N	BSL0P	GNDIOB	GNDIOB	T
U	ASL1P	ASL1N	GNDIOA	GNDIOA	GNDIOA	GNDIOA	GNDIOA	VCCA	VCCA	VCCA	AGND	AGND	VCCA	VCCA	VCCA	GNDIOB	GNDIOB	GNDIOB	GNDIOB	GNDIOB	BSL1N	BSL1P	U
V	GNDIOA	GNDIOA	GNDIOA	GNDIOA	DIG IN2	DIG OUT3	AGND	VCCA	AGND	DNC	DNC	DIODEC	DIODEA	AGND	VCCA	AGND	DIG OUT1	CSN	GNDIOB	GNDIOB	GNDIOB	GNDIOB	V
W	GNDIOA	GNDIOA	GNDIOA	GNDIOA	GNDIOA	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDIOB	GNDIOB	GNDIOB	GNDIOB	GNDIOB	W
Y	DIG MODE0	DIG MODE1	GNDIOA	DIG OUT2	GNDIOA	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDIOB	DNC	GNDIOB	MISO	MOSI	Y
AA	GNDIOA	GNDIOA	DIG IN1	GNDIOA	GNDIOA	AGND	AGND	OUTAN	OUTAP	AGND	AGND	AGND	AGND	OUTBP	OUTBN	AGND	AGND	GNDIOB	GNDIOB	RSTN	GNDIOB	GNDIOB	AA
AB		GNDIOA	DIG IN3	DIG IN0	GNDIOA	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDIOB	DIG OUT0	SCLK	GNDIOB		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 7 – EV8DD700 Pinout

5.2.2 EV12DD700 pinout top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		GNDIOA	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	AGND	AGND	AGND	SSON	SSOP	AGND	AGND	AGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	GNDIOB		A
B	GNDIOA	GNDIOA	ASL14P	ASL14N	GNDIOA	VCCD2A	DGND	AGND	SYNCON	SYNCOP	AGND	AGND	SYNCP	SYNCN	AGND	DGND	VCCD2B	GNDIOB	BSL14N	BSL14P	GNDIOB	GNDIOB	B
C	ASL15P	ASL15N	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	BSL15N	BSL15P	C
D	GNDIOA	GNDIOA	ASL12P	ASL12N	GNDIOA	VCCD2A	DGND	AGND	CLK OUTN	CLK OUTP	AGND	AGND	CLKP	CLKN	AGND	DGND	VCCD2B	GNDIOB	BSL12N	BSL12P	GNDIOB	GNDIOB	D
E	ASL13P	ASL13N	GNDIOA	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	GNDIOB	BSL13N	BSL13P	E
F	GNDIOA	GNDIOA	ASL10P	ASL10N	GNDIOA	GNDIOA	GNDIOA	VCCD2A	DGND	DGND	AGND	AGND	DGND	DGND	VCCD2B	GNDIOB	GNDIOB	GNDIOB	BSL10N	BSL10P	GNDIOB	GNDIOB	F
G	ASL11P	ASL11N	GNDIOA	GNDIOA	VCCIOA	VCCIOA	VCCIOA	VCCIOA	VCCD2A	DGND	AGND	AGND	DGND	VCCD2B	VCCIOB	VCCIOB	VCCIOB	VCCIOB	GNDIOB	GNDIOB	BSL11N	BSL11P	G
H	GNDIOA	GNDIOA	ASL8P	ASL8N	GNDIOA	VCCIOA	DGND	VCCD1A	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	VCCD1B	DGND	VCCIOB	GNDIOB	BSL8N	BSL8P	GNDIOB	GNDIOB	H
J	ASL9P	ASL9N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	VCCD1A	DGND	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	DGND	VCCD1B	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL9N	BSL9P	J
K	GNDIOA	GNDIOA	ASL6P	ASL6N	GNDIOA	GNDIOA	DGND	VCCD1A	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	VCCD1B	DGND	GNDIOB	GNDIOB	BSL6N	BSL6P	GNDIOB	GNDIOB	K
L	ASL7P	ASL7N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	DGND	VCCD1A	VCCD2A	VCCD2A	DGND	DGND	VCCD2B	VCCD2B	VCCD1B	DGND	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL7N	BSL7P	L
M	GNDIOA	GNDIOA	ASL4P	ASL4N	GNDIOA	GNDIOA	DGND	VCCD1A	DGND	VCCD2A	DGND	DGND	VCCD2B	DGND	VCCD1B	DGND	GNDIOB	GNDIOB	BSL4N	BSL4P	GNDIOB	GNDIOB	M
N	ASL5P	ASL5N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	DGND	VCCD1A	DGND	AGND	VCCA	VCCA	AGND	DGND	VCCD1B	DGND	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL5N	BSL5P	N
P	GNDIOA	GNDIOA	ASL2P	ASL2N	GNDIOA	VCCIOA	VCCD1A	DGND	AGND	AGND	VCCA	VCCA	AGND	AGND	DGND	VCCD1B	VCCIOB	GNDIOB	BSL2N	BSL2P	GNDIOB	GNDIOB	P
R	ASL3P	ASL3N	GNDIOA	GNDIOA	GNDIOA	VCCIOA	DGND	AGND	AGND	AGND	VCCD3	VCCD3	AGND	AGND	AGND	DGND	VCCIOB	GNDIOB	GNDIOB	GNDIOB	BSL3N	BSL3P	R
T	GNDIOA	GNDIOA	ASL0P	ASL0N	GNDIOA	GNDIOA	GNDIOA	VCCA	AGND	VCCA	AGND	AGND	VCCA	AGND	VCCA	GNDIOB	GNDIOB	GNDIOB	BSL0N	BSL0P	GNDIOB	GNDIOB	T
U	ASL1P	ASL1N	GNDIOA	GNDIOA	GNDIOA	GNDIOA	GNDIOA	VCCA	VCCA	VCCA	AGND	AGND	VCCA	VCCA	VCCA	GNDIOB	GNDIOB	GNDIOB	GNDIOB	GNDIOB	BSL1N	BSL1P	U
V	GNDIOA	GNDIOA	GNDIOA	GNDIOA	DIG IN2	DIG OUT3	AGND	VCCA	AGND	DNC	DNC	DIODEC	DIODEA	AGND	VCCA	AGND	DIG OUT1	CSN	GNDIOB	GNDIOB	GNDIOB	GNDIOB	V
W	GNDIOA	GNDIOA	GNDIOA	GNDIOA	GNDIOA	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDIOB	GNDIOB	GNDIOB	GNDIOB	GNDIOB	W
Y	DIG MODE0	DIG MODE1	GNDIOA	DIG OUT2	GNDIOA	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDIOB	DNC	GNDIOB	MISO	MOSI	Y
AA	GNDIOA	GNDIOA	DIG IN1	GNDIOA	GNDIOA	AGND	AGND	OUTAN	OUTAP	AGND	AGND	AGND	AGND	OUTBP	OUTBN	AGND	AGND	GNDIOB	GNDIOB	RSTN	GNDIOB	GNDIOB	AA
AB		GNDIOA	DIG IN3	DIG IN0	GNDIOA	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDIOB	DIG OUT0	SCLK	GNDIOB		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 8 – EV12DD700 Pinout

5.3 Skew on HSSLs inputs

5.3.1 Introduction

The values are relative to the same reference. ASL1P skew value is 40.7 ps and ASL1N skew value is 34.7 ps. The relative skew value between ASL1P and ASL1N is 6.0 ps.

5.3.2 EV8DD700 skew on HSSLs inputs

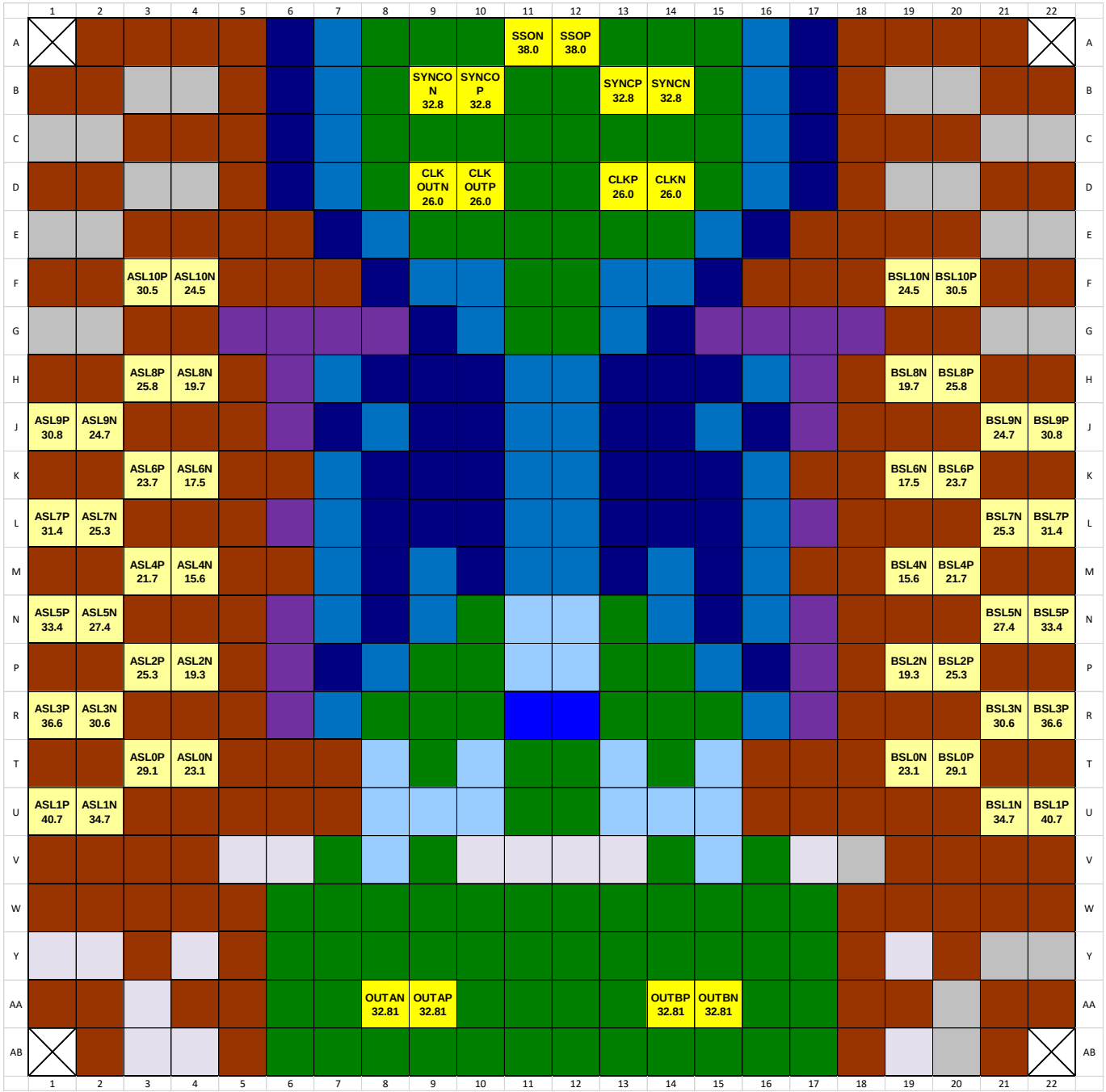


Figure 9 – EV8DD700 relative skews on HSSL, AOUT and Clock signals (values are in ps)

5.3.3 EV12DD700 skew on HSSLs inputs

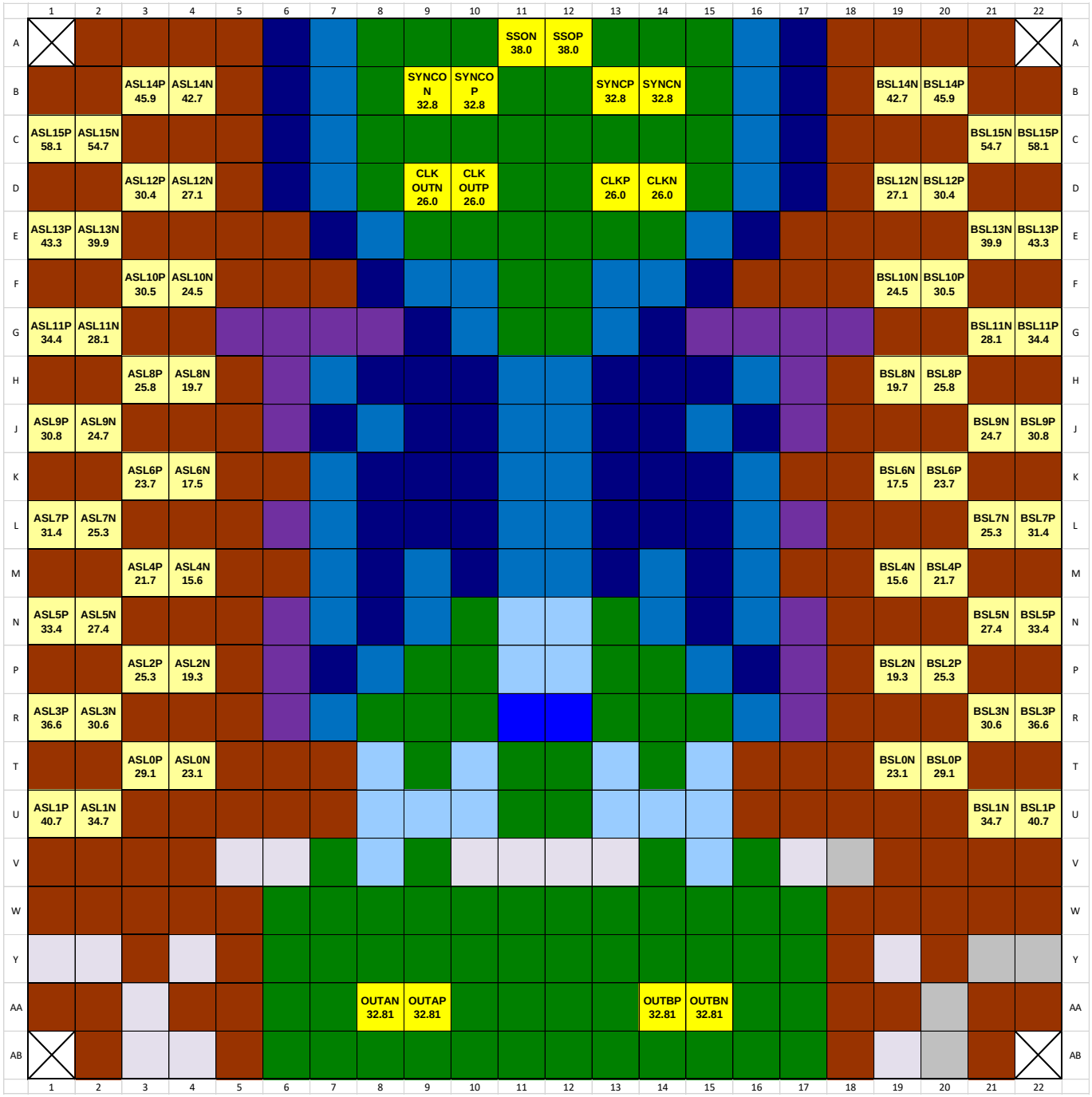


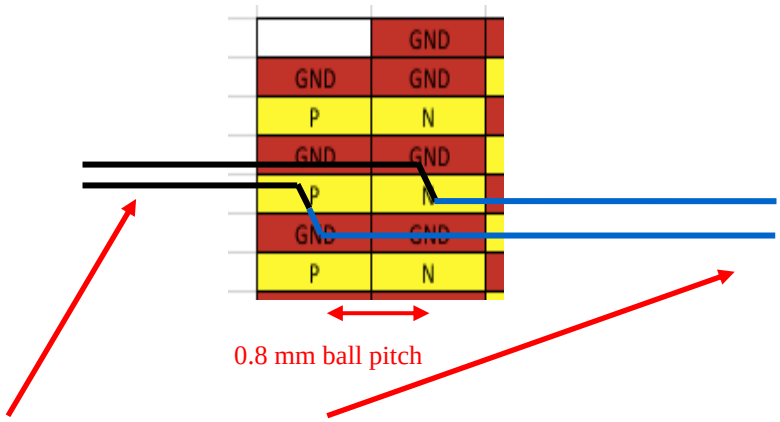
Figure 10 – EV12DD700 relative skews on HSSL, AOUT and Clock signals (values are in ps)

5.3.4 Routing compensation between N and P

In this section, information about xSL0..xSL10 is valid for EV8DD700/EV12DD700 and information about xSL11..xSL15 is valid for EV12DD700 only.

From ASL0P to ASL11P (and BSL0P to BSL11P), P signal ball has a relative skew to N signal ball of 5.9 to 6.2 ps in excess.
For ASL15P and ASL13P (and BSL15P and BSL13P), P signal ball has a relative skew to N signal ball of 3.3 ps in excess.
For ASL14P and ASL12P (and BSL14P and BSL12P), P signal ball has a relative skew to N signal ball of 3.3 ps in excess.

With a special care on the board routing, it is possible to compensate the relative skew between differential serial links (N&P).



Length on board and length on package are almost the same on N and P (less routing on board for P results from more routing inside package for P).

Figure 11 – Routing compensation between P and N

Additional routing in board to connect N compared to P will compensate for 0.966 mm that is 0.966*SQRT(3.5)*3.335 ps = 6.0 ps in a board material with Dk = 3.5, so ASL0P to ASL11P (and BSL0P to BSL11P) are well matched when considering package and board.

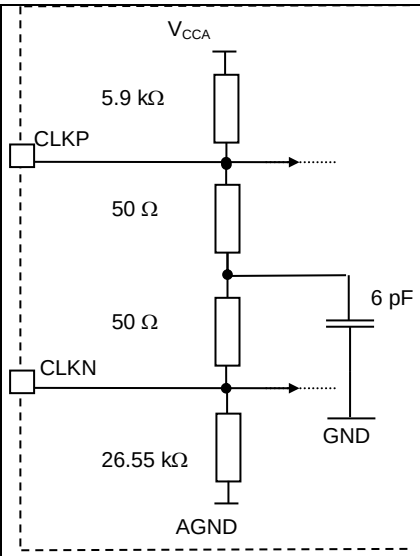
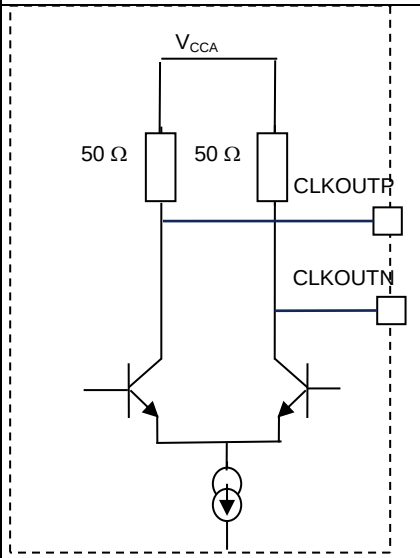
ASL12P, ASL13P, ASL13P, ASL14P, BSL12P, BSL13P, BSL13P and BSL14P which have only 3.3 ps in excess in package will be overcompensated by 6.0 ps in board.
If sufficient eye diagram is expected elsewhere then it could be neglected.
If eye diagram is expected too tight in width then an extra compensation of 0.43 mm can be added to P trace on board to add 2.7 ps.

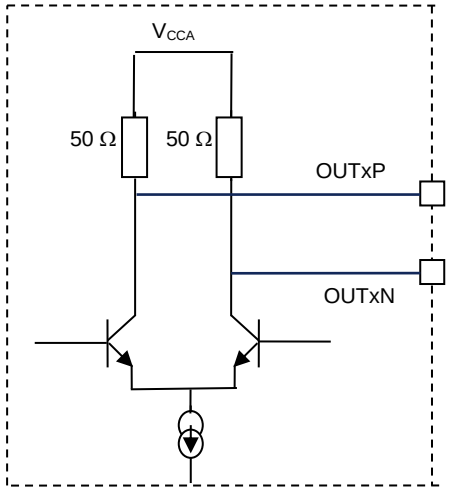
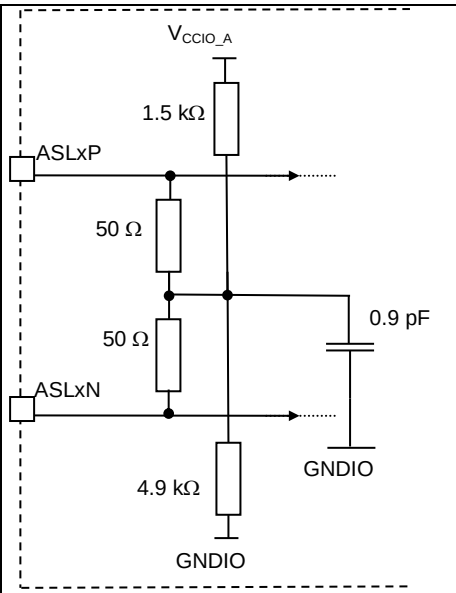
5.4 Pinout table

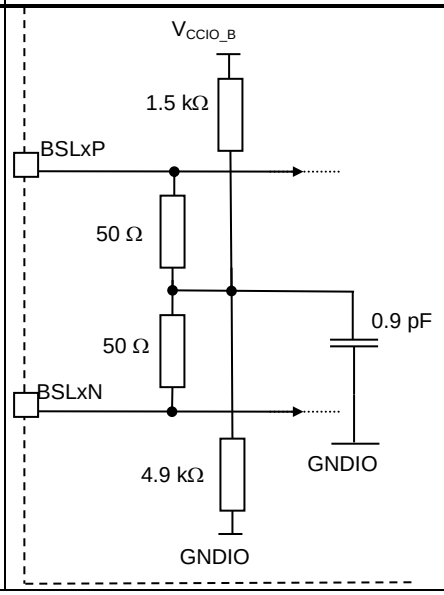
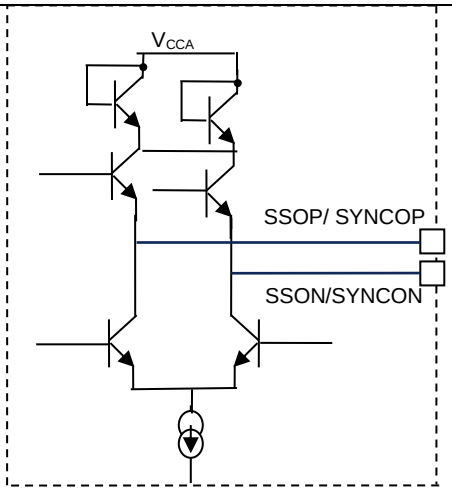
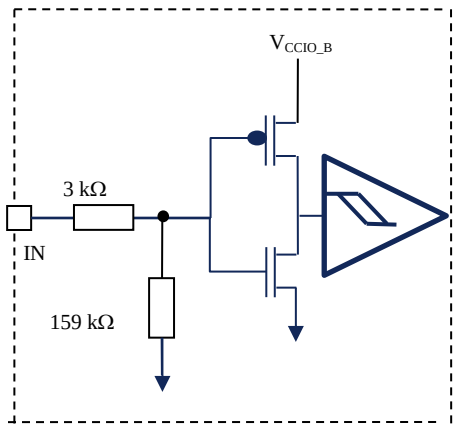
Table 16. Pinout Table

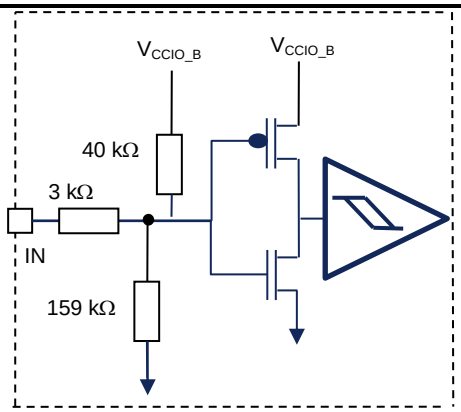
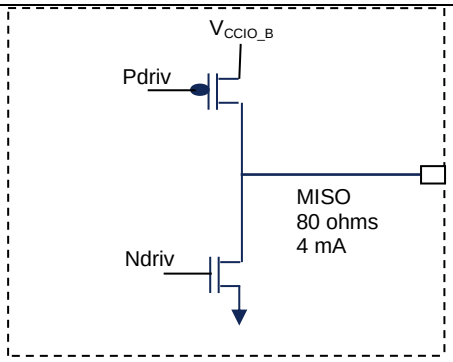
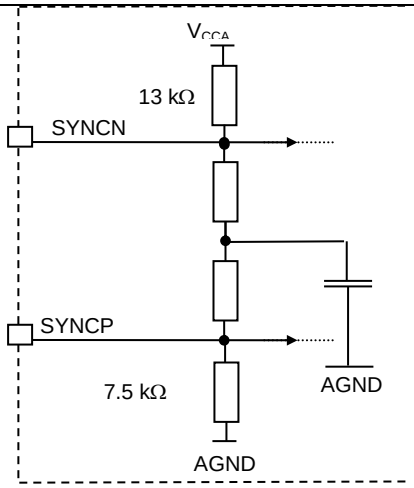
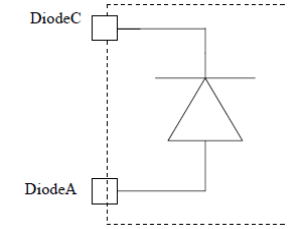
Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies				
AGND	A8, A9, A10, A13, A14, A15, B8, B11, B12, B15, C8, C9, C10, C11, C12, C13, C14, C15, D8, D11, D12, D15, E9, E10, E11, E12, E13, E14, F11, F12, G11, G12, N10, N13, P9, P10, P13, P14, R8, R9, R10, R13, R14, R15, T9, T11, T12, T14, U11, U12, V7, V9, V14, V16, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, AA6, AA7, AA10, AA11, AA12, AA13, AA16, AA17, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17	Analog ground All ground pins must be connected to a one solid ground plane on PCB Common ground		

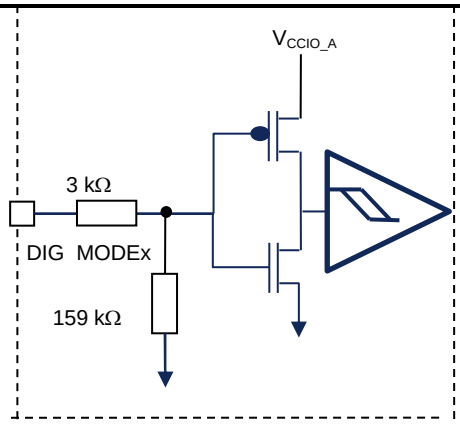
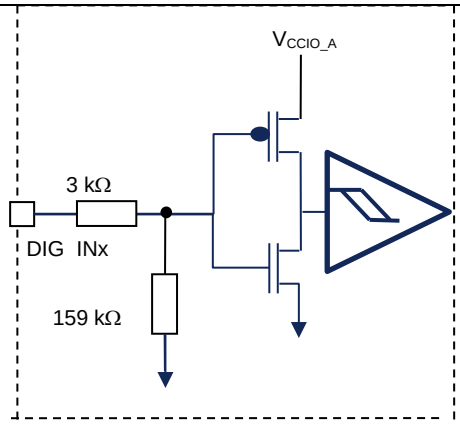
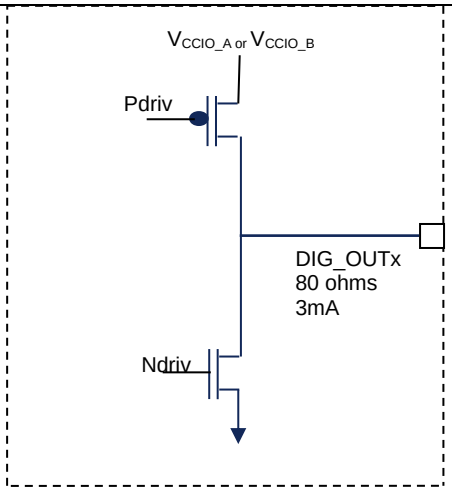
Pin Label	Pin number	Description	Direction	Simplified electrical schematics
DGND	A7, A16, B7, B16, C7, C16, D7, D16, E8, E15, F9, F10, F13, F14, G10, G13, H7, H11, H12, H16, J8, J11, J12, J15, K7, K11, K12, K16, L7, L11, L12, L16, M7, M9, M11, M12, M14, M16, N7, N9, N14, N16, P8, P15, R7, R16	Digital ground All ground pins must be connected to a one solid ground plane on PCB Common ground		
GNDIO	A2, A3, A4, A5, A18, A19, A20, A21, B1, B2, B5, B18, B21, B22, C3, C4, C5, C18, C19, C20, D1, D2, D5, D18, D21, D22, E3, E4, E5, E6, E17, E18, E19, E20, F1, F2, F5, F6, F7, F16, F17, F18, F21, F22, G3, G4, G19, G20, H1, H2, H5, H18, H21, H22, J3, J4, J5, J18, J19, J20, K1, K2, K5, K6, K17, K18, K21, K22, L3, L4, L5, L18, L19, L20, M1, M2, M5, M6, M17, M18, M21, M22, N3, N4, N5, N18, N19, N20, P1, P2, P5, P18, P21, P22, R3, R4, R5, R18, R19, R20, T1, T2, T5, T6, T7, T16, T17, T18, T21, T22, U3, U4, U5, U6, U7, U16, U17, U18, U19, U20, V1, V2, V3, V4, V5, V19, V20, V21, V22, W1, W2, W3, W4, W5, W18, W19, W20, W21, W22, Y1, Y2, Y3, Y5, Y18, Y20, AA1, AA2, AA3, AA4, AA5, AA18, AA19, AA21, AA22, AB2, AB3, AB4, AB5, AB18, AB21	Ground for Input/Output buffers		
V_{CCA}	N11, N12, P11, P12, T8, T10, T13, T15, U8, U9, U10, U13, U14, U15, V8, V15	Analog power supply		
V_{CCD_1B}	H15, J16, K15, L15, M15, N15, P16	Digital power supply for HSSL, ESIstream (core B) and SPI interface, DIG_OUT0 &1		
V_{CCD_1A}	H8, J7, K8, L8, M8, N8, P7	Digital power supply for HSSL, ESIstream (core A), DIG_OUT2&3, DIG_INx, DIG_MODEx		
V_{CCD_2B}	A17, B17, C17, D17, E16, F15, G14, H13, H14, J13, J14, K13, K14, L13, L14, M13	Digital power supply for DUC (core B)		
V_{CCD_2A}	A6, B6, C6, D6, E7, F8, G9, H9, H10, J9, J10, K9, K10, L9, L10, M10	Digital power supply for DUC (core A)		

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
V_{CCD_3}	R11, R12	Digital power supply for analog blocks		
V_{CCIO_B}	G15, G16, G17, G18, H17, J17, L17, N17, P17, R17	Power supply for BSLxP & N DIG_OUT0&1 and SPI I/O buffers		
V_{CCIO_A}	G5, G6, G7, G8, H6, J6, L6, N6, P6, R6	Power supply for ASLxP & N, DIG_OUT2&3, DIG_INx, DIG_MODEx I/O buffers		
Clock signal				
CLKP CLKN	D13, D14	In phase and Out of phase input clock signal	I	
CLKOUTP CLKOUTN	D10, D9	In phase and Out of phase out clock signal	O	
Analog signals				

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
OUTBP OUTBN	AA14, AA15	In phase analog output B Out of phase analog output B	O	
OUTAP OUTAN	AA9, AA8	In phase analog output A Out of phase analog output A	O	
Digital Input signals (CML)				
ASL0-10P, ASL0-10N	T3, T4, U1, U2, P3, P4, R1, R2, M3, M4, N1, N2, K3, K4, L1, L2, H3, H4, J1, J2, F3, F4	Channel A input data serial link 0 to 10	I	
ASL11-15P, ASL11-15N	G1, G2, D3, D4, E1, E2, B3, B4, C1, C2	Channel A input data serial link 11 to 15 (1)	I	
BSL0-10P, BSL0-10N	T20, T19, U22, U21, P20, P19, R22, R21, M20, M19, N22, N21, K20, K19, L22, L21, H20, H19, J22, J21, F20, F19	Channel B input data serial link 0 to 10	I	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
BSL11-15P, BSL11-15N	G22, G21, D20, D19, E22, E21, B20, B19, C22, C21	Channel B input data serial link 11 to 15 (1)	I	
Digital output Signal (LVDS)				
SSOP, SSON	A12, A11	In phase and out of phase Slow Synchro Output. Fsso=Fs/32	O	
SYNCOP, SYNCON	B10, B9	In phase and out of phase Sync Output.	O	
Digital I/0 (CMOS)				
SCLK	AB20	SPI signal : Input serial Clock Serial data is shifted into and out SPI synchronously to this signal on falling transition of SCLK. Internal pull-down	I	
MOSI	Y22	SPI signal: Data Input signal (Master Out Slave In) Serial data input is shifted into SPI while CSN is active low Internal pull-down	I	
CSN	V18	SPI signal Input Chip Select signal (Active low)	I	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
		When this signal is active low, SCLK is used to clock data present on MOSI or MISO signal. Internal pull-up		
RSTN	AA20	SPI signal Input Digital asynchronous reset (Active low) This signal allows to reset the internal value of SPI to their default value Internal pull-up	I	
MISO	Y21	SPI signal Data output SPI signal (Master In Slave Out) Serial data output is shifted out SPI while CSN is active low.	O	
DIGITAL INPUT (LVDS)				
SYNCP SYNCN	B13, B14	Differential Input Synchronization signal (LVDS) Active high signal Equivalent internal differential 100Ω input resistor	I	
Miscellaneous				
DiodeA, DiodeC	V13, V12	Junction Temperature Monitoring diode Anode Junction Temperature Monitoring diode Cathode Cathode must be connected to ground (AGND) externally	I	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
DIG_MODE0 DIG_MODE1	Y1 Y2	Digital input pin Internal pull-down	I	
DIG_IN0 DIG_IN1 DIG_IN2 DIG_IN3	AB4 AA3 V5 AB3	Digital input pin Internal pull-down	I	
DIG_OUT0 DIG_OUT1 DIG_OUT2 DIG_OUT3	AB19, V17, Y4, V6	Digital output pin	O	
DNC	V10, V11, Y19	Do not connect		

(1) Available for EV12DD700 only

6. DEFINITION OF TERMS

Table 17. Definition of terms

Abbreviation	Term	Definition
(BER)	Bit Error Rate	percentage of bits with errors divided by the total number of bits that have been transmitted, received or processed over a given time period
(FPBW)	Full power output bandwidth	Analog output frequency at which the fundamental component in the output spectrum has fallen by 3 dB with respect to the theoretical sin(x)/x curve, for output at Full Scale (0 dBFS).
(Fs max)	Maximum conversion Frequency	Maximum conversion frequency
(Fs min)	Minimum conversion frequency	Minimum conversion Frequency
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, set at Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It is reported in dBc (i.e, related to output signal level).
(HSL)	Highest Spur Level	Power of the highest spurious spectral component expressed in dBm
(ENOB)	Effective Number Of Bits	ENOB is determinate from NPR measurement with the formula : ENOB = ($NPR_{[dB]}$ + $\|LF_{[dB]}\|$ -3 - 1.76) / 6.02 Where LF is the loading factor is the ratio between the Gaussian noise standard deviation versus amplitude full scale.
(SNR)	Signal to noise ratio	SNR is determinate from NPR measurement with the formula : $SNR_{[dB]} = NPR_{[dB]} + \|LF_{[dB]}\| - 3$ Where LF is the loading factor is the ratio between the Gaussian noise standard deviation versus amplitude full scale.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the DAC performance with broadband output signals. When applying a notch-filtered broadband gaussian-noise pattern as the input to the DAC under test, the Noise Power Ratio is defined as the ratio of the average noise measured on the shoulder of the notch and inside the notch on the same integration bandwidth.
(DNL)	Differential non linearity	The Differential Non Linearity for a given code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there is no missing point and that the transfer function is monotonic.
(INL)	Integral non linearity	The Integral Non Linearity for a given code i is the difference between the measured voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(TPD/TOD)	Output delay	The analog output delay measured between the rising edge of the differential input data on serial lane (zero crossing point of 1st bit of ESIstream frame) to the zero crossing point of a full-scale analog output voltage step. TPD corresponds to the pipeline delay plus an internal

		propagation delay (TOD) including package access propagation delay and internal (on-chip) delays such as clock input buffers and DAC conversion time.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the insertion loss linked to power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected).
(NRZ)	Non Return to Zero mode	Non Return to Zero mode on analog output
(RF)	Radio Frequency mode	RF mode on analog output
(2RF)	Twice RF	2RF mode on analog output

7. PACKAGE DESCRIPTION

7.1 Type /Outline

HiTCE Ceramic Ball Grid Array CBGA480

- High TCE Glass-Ceramic substrate
- Body size : 20x20mm
- Number of balls : 480
- Conductor : cofired copper
- NiAu finish (FC and BGA sides)
- SnAg 1.8 bumps

Package interconnection

- 22x22 BGA matrix (480 balls, 4 corner balls removed)
- 0.80mm ball pitch
- Ball type : RoHs SAC or Pb90Sn10 (2 variants available)
- MSL3 (non-hermetic)

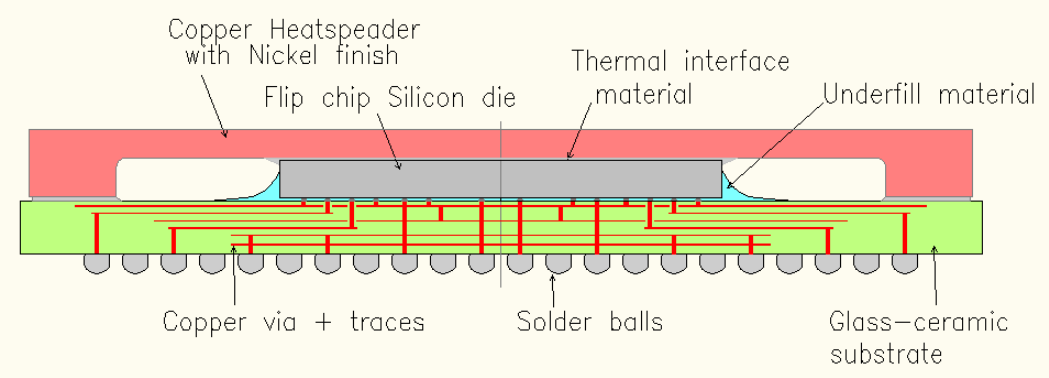


Figure 12 – Ceramic package cross-section

7.2 Mechanical outline drawing

7.2.1 Mechanical outline drawing with SAC balls

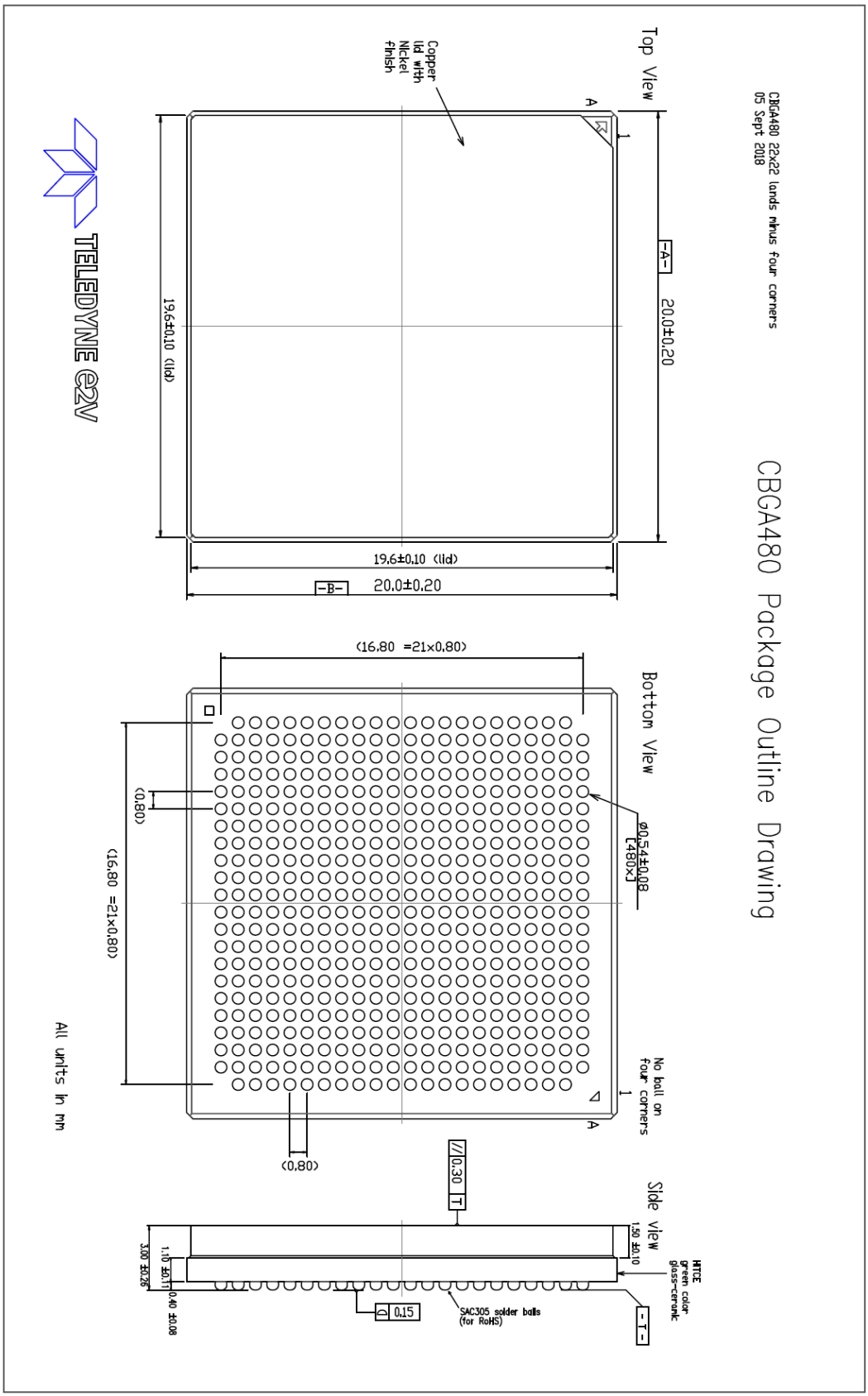


Figure 13 – Mechanical outline drawing with SAC balls

7.2.2 Mechanical outline drawing with Pb90Sn10 balls

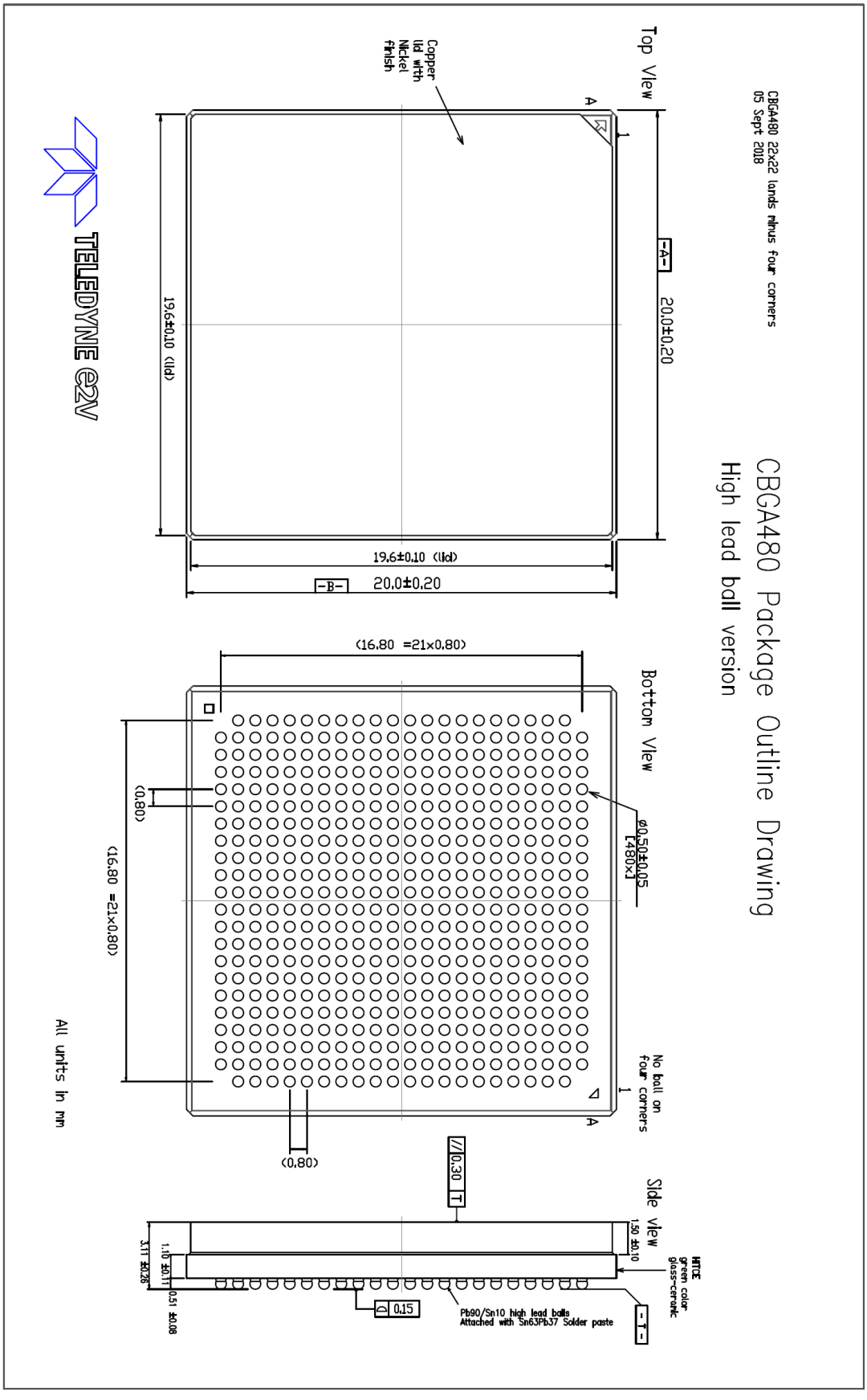


Figure 14 – Mechanical outline drawing with Pb90Sn10 balls

7.3 Thermal characteristics

Table 18. Thermal characteristics

Parameter	Symbol	Value	Unit	Note
Thermal resistance from junction to bottom of balls	$Rth_{Junction\ to\ Bottom\ of\ balls}$	3.33	°C/Watt	(1)(2)
Thermal resistance from junction to board (JEDEC JESD51-8)	$Rth_{junction\ -\ board}$	4.9	°C/Watt	(1)(2)(4)
Thermal resistance from junction to top of lid	$Rth_{Junction\ –\ lid}$	1.86	°C/Watt	(1)(2)
Thermal resistance from junction to ambient (JEDEC standard)	$Rth_{Junction\ –\ ambient}$	4.9	°C/Watt	(1)(3)
Delta temperature Hot spot – temperature from diode		6.5	°C	

Notes:

1. Rth are calculated from hot spot, not from average temperature of the die
   These figures are thermal simulation results (finite elements method) with nominal cases assuming a 8.13W power consumption:
   - Nominal supplies,
   - CLKOUT, SSO & SYNCO features OFF,
   - 2RF output mode,
   - interpolation by 4,
   - No beamforming,
   - Unused HSSLs are powered OFF
2. Assumptions : no air, pure conduction, no radiation
3. Assumptions:
   - Convection according to JEDEC
   - Still air
   - Horizontal 2s2p board
   - Board size 114.3 x 76.2 mm, 1.6 mm thickness
4. Assumptions: 2s2p board

8. THEORY OF OPERATION

The EV8DD700/EV12DD700 is a 8-bit/12-bit dual RF/microwave DAC with a high-speed serial interface based on the flexible, efficient and simple ESIstream protocol. ESIstream is an open license free, high efficiency serial interface protocol based on 14b/16b encoding. Its main benefits are low overhead and ease of hardware implementation. Each DAC core can convert either real data or complex data through their respective Digital Up-Converter (DUC). Each functions of the DAC can be controlled through a Serial Peripheral Interface (SPI).
An external high performance clock signal is necessary to clock the DAC cores. The clock management unit drives each core from this external clock signal and derives the different clock domains for the other circuit blocks such as the SERDES and along the digital data path.
The device can be operated in different output modes with respect to the performance targeted over the full operating bandwidth. The -3dB bandwidth is 25 GHz for a direct signal synthesis without up-conversion stages in the RF front-end. The appropriate output mode is selectable to achieve the best compromise between output power and dynamic range. NRZ/ RF and 2RF modes are used with a clock frequency signal up to 12 GHz and 24 GHz, respectively.
The output gain is adjustable and the output frequency response can be flatten by the anti-sinc function filter (A-SINC).
In real data mode (no interpolation), a very wide Nyquist Zone or maximum instantaneous bandwidth of 6 GHz is synthesized. 11 HSSLs (EV8DD700) or 16 HSSLs (EV12DD700) at 12 Gbps per DAC core are used to provide the digital data to the device.
In complex data mode, interpolation factors (by 4, 8 or 16) can be applied to single cores or both to reduce the overall data rate and reduce the number of HSSLs. Innovative functions are available to control amplitude and phase delays as well as frequency in the digital data path. These functions are Beamforming (enabled by BEAM_ENA), Beam Hopping (to hop up to 4 zones), Fast Frequency Hopping and DDS/chirp. Beamforming, Beam Hopping and DDS/chirp are configured through Serial Peripheral Interface (SPI). Fast Frequency Hopping can also be controlled through ASL0/BSL0 for fast reconfiguration. To allow better spectral efficiency, a DUC is used. This complex mixer translates baseband I/Q signal to digital LO frequency, thanks to a programmable 32-bit Numerically Controlled Oscillator (NCO).
The DAC is capable of multi-device synchronization in a deterministic latency manner either through a synchronization chaining approach or a point-to-point architecture. The SYNC signal can be propagated to another DAC (sync chain) through the SYNCO pin.
The DAC can provide a Slow Synchronous Output (SSO) frequency reference to the FPGA which is a programmable ratio of the input clock.
The list of available modes and their possible combination are found in Table 19 and Table 20. In case of single channel DAC mode, please refer to chapter 13.1.3

Table 19. List of modes in 12-bit/8-bit mode

	Nb of HSSL Core A	Nb of HSSL Core B	DUC Core A power	DUC Core B power	Number of channels
Interpolation by 4 with core A	8/6	0	ON	OFF	Single
Interpolation by 8 with core A	4/3	0	ON	OFF	Single
Interpolation by 16 with core A	2/2	0	ON	OFF	Single
Interpolation by 4 with core B	0	8/6	OFF	ON	Single
Interpolation by 8 with core B	0	4/3	OFF	ON	Single
Interpolation by 16 with core B	0	2/2	OFF	ON	Single
Interpolation by 4 with core A & B	8/6	8/6	ON	ON	Dual
Interpolation by 8 with core A & B	4/3	4/3	ON	ON	Dual
Interpolation by 16 with core A & B	2/2	2/2	ON	ON	Dual
Interpolation by 4 + Beamforming	0	8/6	ON	ON	Dual
Interpolation by 8 + Beamforming	0	4/3	ON	ON	Dual
Interpolation by 16 + Beamforming	0	2/2	ON	ON	Dual
Interpolation by 4 + Beam-Hopping	0	8/6	ON	ON	Dual
Interpolation by 8 + Beam-Hopping	0	4/3	ON	ON	Dual
Interpolation by 16 + Beam-Hopping	0	2/2	ON	ON	Dual

	Nb of HSSL Core A	Nb of HSSL Core B	DUC Core A power	DUC Core B power	Number of channels
DDS/CHIRP mode with core A (interpolation by 4, 8 or 16)	0	0	ON	OFF	Single
DDS/CHIRP mode with core B (interpolation by 4, 8 or 16)	0	0	OFF	ON	Single
DDS/CHIRP mode with core A & B (interpolation by 4, 8 or 16)	0	0	ON	ON	Dual
Frequency Hopping programmed by SPI					
Frequency Hopping (interpolation by 4) with core A	8/6	0	ON	OFF	Single
Frequency Hopping (interpolation by 8) with core A	4/3	0	ON	OFF	Single
Frequency Hopping (interpolation by 16) with core A	2/2	0	ON	OFF	Single
Frequency Hopping (interpolation by 4) with core B	0	8/6	OFF	ON	Single
Frequency Hopping (interpolation by 8) with core B	0	4/3	OFF	ON	Single
Frequency Hopping (interpolation by 16) with core B	0	2/2	OFF	ON	Single
Frequency Hopping (interpolation by 4) with core A & B	8/6	8/6	ON	ON	Dual
Frequency Hopping (interpolation by 8) with core A & B	4/3	4/3	ON	ON	Dual
Frequency Hopping (interpolation by 16) with core A & B	2/2	2/2	ON	ON	Dual
Frequency Hopping programmed by HSSL0					
Frequency Hopping (interpolation by 4) with core A	9/7	0	ON	OFF	Single
Frequency Hopping (interpolation by 8) with core A	5/4	0	ON	OFF	Single
Frequency Hopping (interpolation by 16) with core A	3/3	0	ON	OFF	Single
Frequency Hopping (interpolation by 4) with core B	0	9/7	OFF	ON	Single
Frequency Hopping (interpolation by 8) with core B	0	5/4	OFF	ON	Single
Frequency Hopping (interpolation by 16) with core B	0	3/3	OFF	ON	Single
Frequency Hopping (interpolation by 4) with core A & B	9/7	9/7	ON	ON	Dual
Frequency Hopping (interpolation by 8) with core A & B	5/4	5/4	ON	ON	Dual
Frequency Hopping (interpolation by 16) with core A & B	3/3	3/3	ON	ON	Dual
Real data with core A	16/11	0	OFF	OFF	Single
Real data with core B	0	16/11	OFF	OFF	Single
Real data with core A & B	16/11	16/11	OFF	OFF	Dual
Test mode (ramp, flash, static value etc…)	0	0	OFF	OFF	Single or dual

Table 20. Possible combination of operating modes

✓ Modes are compatible
■ Modes are not compatible

	No interpolation (real data)	DUC interpolation (4, 8 or 16)	BFM/BH (2, 3 or 4 zones)	DDS (ramp, sinewave or chirp)	FH (phase reset or continuous)	DAC output mode (NRZ, RF, 2RF)	8-bit/12-bit	Gain adjust	A-SINC	Test mode (ramp or flash)
No interpolation (real data)		■	■	■	■	✓	✓	✓	✓	✓
DUC interpolation (4, 8 or 16)	■		✓	✓	✓	✓	✓	✓	✓	■
BFM/BH (2, 3 or 4 zones)	■	✓		■	✓	✓	✓	✓	✓	■
DDS (ramp, sinewave or chirp	■	✓	■		■	✓	✓	✓	✓	■
FH (phase reset or continuous)	■	✓	✓	■		✓	✓	✓	✓	■
DAC output mode (NRZ, RF, 2RF)	✓	✓	✓	✓	✓		✓	✓	✓	✓
8-bit/12-bit	✓	✓	✓	✓	✓	✓		✓	✓	✓
Gain adjust	✓	✓	✓	✓	✓	✓	✓		✓	✓
A-SINC	✓	✓	✓	✓	✓	✓	✓	✓		✓
Test mode (ramp or flash)	✓	■	■	■	■	✓	✓	✓	✓	

9. SERIAL PERIPHERAL INTERFACE (SPI)

The digital interface is a standard SPI with:

- 16 bits for the address A[15] to A[0] including a R/W bit (A[15] = R/W, being A[15] is the MSB);
- 16 bits of data D[15] to D[0] with D[15] the MSB.

5 signals are required:

- RSTN for the SPI reset;
- SCLK for the SPI clock;
- CSN for the Chip Select;
- MISO for the Master In Slave Out SPI Output
- MOSI for the Master Out Slave In SPI Input.

The MOSI sequence should start with one R/W bit (A[15]):

- R/W = 0 is a read instruction
- R/W = 1 is a write instruction

Writing instruction on a 16-bit register (R/W = 1):

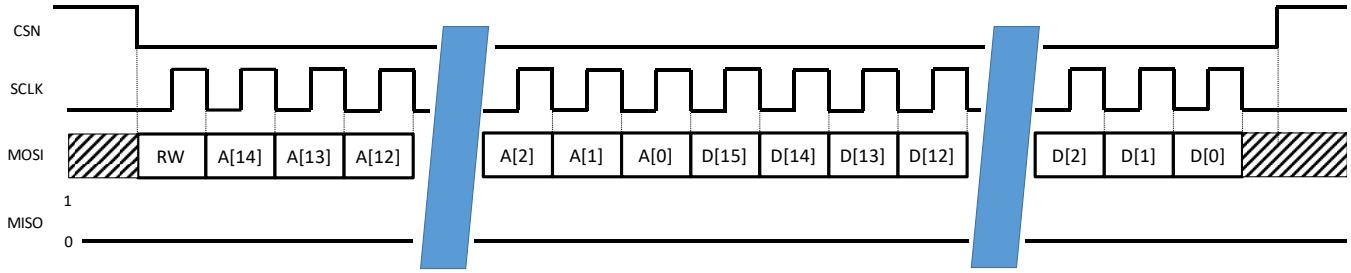


Figure 15 - SPI writing timing

Reading instruction on a 16-bit register (R/W = 0):

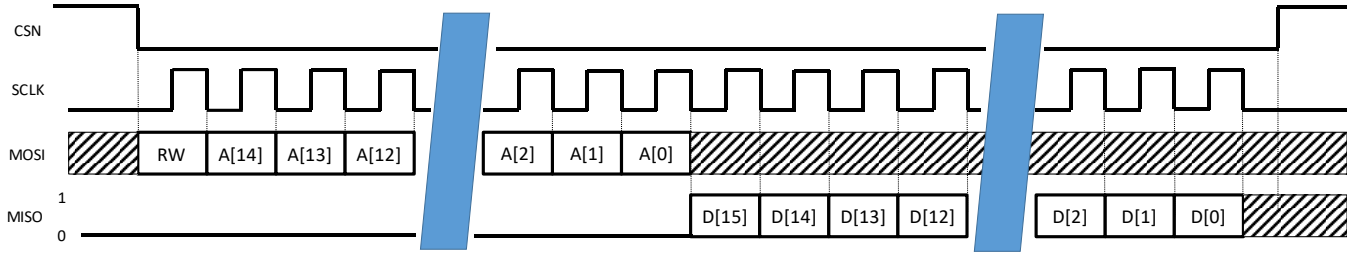


Figure 16 - SPI reading timing

See section Table 13 for SPI timing characteristics (max clock frequency, …)

10. ESISTREAM SERIAL DATA INTERFACE

10.1 Serial link Analog Front End

The serial link receiver can be tuned according to its input data rate and lane length. Cut-off frequency can be set by SPI for each lane (see SERDES_ANA register description Table 173).

10.2 Serial link protocol

The DAC offers a high-speed serial interface to receive data; it has up to 32 high-speed serial lanes (up to 16 per core) running at a ratio of the external clock frequency (fc) depending on interpolation ratio (see interpolation chapter). It uses the protocol ESIstream to optimize efficiency, simplicity and latency.

ESIstream protocol specifications, example designs and simulations available on www.esistream.com.

ESIstream provides an efficient 14b/16b high-speed serial data transmission protocol deploying Current Mode Logic (CML) transceivers. It is license-free and supports in particular serial communication between FPGAs and High-Speed data converters. The protocol initiated by Teledyne-e2v is born from a severe need of the following combination:

- Reduced data overhead on serial links, as low as possible.
- Increased rate of useful data when linking ADCs operating at GSPS speeds with FPGAs on a serial interface.
- Simplified hardware implementation. It uses few logic resources and it is simple enough to be built on RF SiGe technologies.

An ESIstream system comprises at a minimum a transmitter and a receiver.

- A transmitter can be an ADC or an FPGA or an ASIC
- A receiver can be a DAC or an FPGA or an ASIC
- A number of lanes (L ≥ 1) to transmit serial data
- A synchronization signal (sync) to initialize the communication.

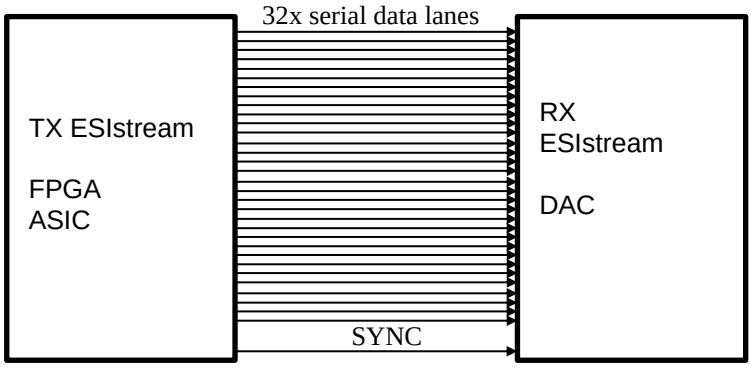


Figure 17: ESIstream system example using the DAC

ESIstream uses 14b/16b encoding giving it a 87.5% data rate efficiency. In other words, the encoding takes 14-bit of raw data, the data word, and adds two bits of protocol overhead. The overhead comprises a Clock Bit (Clk) which toggles between each frame and the Disparity Bit (DB), which ensures that a deterministic DC balance is maintained for each data lane. The data word contains two control bits, CB1 and CB2 respectively the bit 12 and the bit 13 and a DAC sample on bits 0 to 11. The 16-bit ESIstream frame comprises a scrambled version of the data word (sample + control bits) combined with the overhead bits.

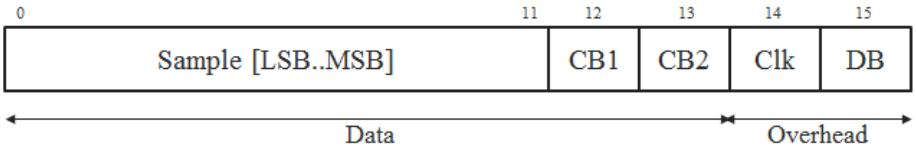


Figure 18: Unscrambled ESIstream frame

To ensure a statistical DC balanced transmission, the data word is first scrambled. The ESIstream transmit encoding system comprises a linear feedback shift register (LFSR) which generates a pseudo random binary sequence (PRBS), based on a Fibonacci polynomial. The PRBS is used to scramble the data word (14 LSB bits).

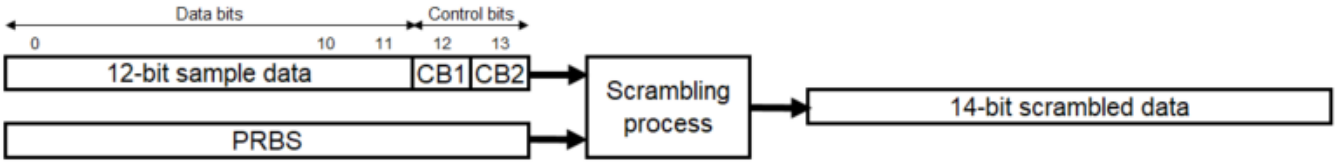


Figure 19: TX 14-bit scrambling process principle

Then the 14-bits data word is encoded. The encoding process comprises concatenation of the clock bit, a disparity processing applied on the 15 LSB bits (data word + clock bit) and concatenation of the disparity bit.

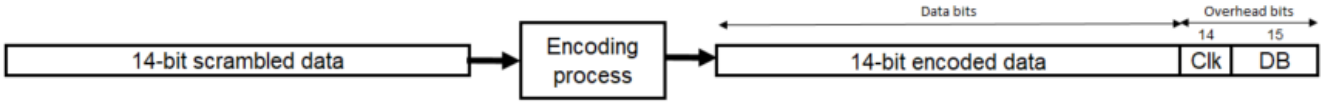


Figure 20: TX 16-bit encoding process principle

The 16-bit frame thus obtained is sent through the high-speed serial link. By default, frames are transmitted LSB first.

During normal operation, the synchronization of the serial links and transmission bit errors can be monitored through the control bit CB2 (bit 13) when parity check is enabled in the DAC using ESI_PARITY_ENA bit of ESISTREAM_CFG register.

CB1 and Clk bit are not used by the DAC

10.2.1 Synchronization

The link must be synchronized to align the frames between the transmitter and the receiver and to synchronize the reception scrambler (DAC) with the transmission scrambler (FPGA or ASIC).

ESIstream starts the link synchronization using a synchronization signal, the SYNC pulse.
On a SYNC pulse, the transmitter sends the synchronization sequence to the receiver. The synchronization sequence is composed of the Frame Alignment Sequence (FAS) and of the PRBS alignment sequence (PAS).

- The FAS, 32 frames alternating between 0xFF00 and 0x00FF, allows aligning all the frames sent between the transmitter and the receiver. As the sequence is already DC balanced, the sequence bypasses the scrambling and disparity processing.
- The PAS, 32 frame containing only the scrambling PRBS of the transmitter, allows synchronizing the descrambler of the receiver with the scrambler of the transmitter. The sequence go through the disparity processing, as the PRBS value will start to impact the running disparity of the transmission.

After the 64 frames of the synchronization sequence, the next frame contains the first valid data of the transmission. For each lane of the serial link, when the receiver receives the first valid data, it stores it and the following ones in an output buffer.

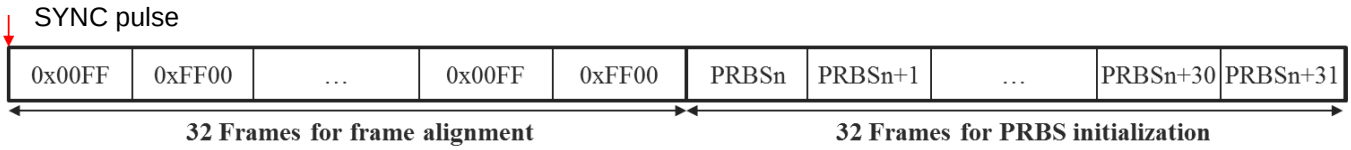


Figure 21: Synchronization sequence

The SYNC pulse must be sent to the receiver and to the transmitter. The receiver must receive the SYNC pulse prior to the ESIstream Synchronization Sequence.

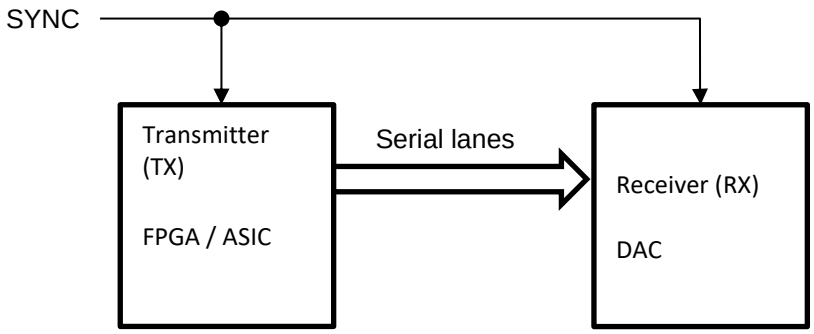


Figure 22: SYNC pulse sequence principle between ESIstream transmitter and receiver

When the transmitter detects a SYNC pulse, it sends the ESIstream synchronization sequence on each serial lanes.

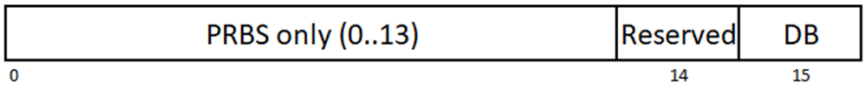


Figure 23: Frame sent for PRBS initialization

The receiver embeds a LFSR based on the same Fibonacci polynomial than the transmitter. The receiver will detect the transition between the FAS and PAS and will use a minimum of two PRBS data frames to initialize its LFSR.
Once initialized, the receiver LFSR is synchronized with the transmitter LFSR and it starts generating the same PRBS values used by the transmitter to scramble the data. Then, the receiver uses the PRBS values to descramble the received frames applying a XOR bitwise operation between PRBS value and received scrambled data word.

After this ESIstream synchronization sequence, the link synchronization is complete.

10.2.2 Scrambling

Applying scrambling ensures a statistical DC balanced transmission. It also statistically ensures that there are enough transitions within the transmitted data stream to ensure the link remains locked at the receive end of the link. It is necessary to comply with these constraints otherwise the eye opening detection module used by the receiver may lose its lock and the data would be corrupted at deserializer output.

The scrambling technique used in ESIstream is an additive scrambling to avoid error propagation in case of a single bit error. It is based on Fibonacci architecture using the following polynomial: X17+X3+1. It has a run length of 217 - 1. Instead of using a shift of one bit per operation, it uses shifts of 14 bits per operation to adapt to the size of the data being scrambled.
The equations to use to generate this PRBS are as follow:

$$LFSR_{n+1}(0) = LFSR_n(14)$$
$$LFSR_{n+1}(1) = LFSR_n(15)$$
$$LFSR_{n+1}(2) = LFSR_n(16)$$
$$LFSR_{n+1}(3) = LFSR_n(0) \text{ xor } LFSR_n(3)$$
$$LFSR_{n+1}(4) = LFSR_n(1) \text{ xor } LFSR_n(4)$$
$$LFSR_{n+1}(5) = LFSR_n(2) \text{ xor } LFSR_n(5)$$
$$LFSR_{n+1}(6) = LFSR_n(3) \text{ xor } LFSR_n(6)$$
$$LFSR_{n+1}(7) = LFSR_n(4) \text{ xor } LFSR_n(7)$$
$$LFSR_{n+1}(8) = LFSR_n(5) \text{ xor } LFSR_n(8)$$
$$LFSR_{n+1}(9) = LFSR_n(6) \text{ xor } LFSR_n(9)$$
$$LFSR_{n+1}(10) = LFSR_n(7) \text{ xor } LFSR_n(10)$$
$$LFSR_{n+1}(11) = LFSR_n(8) \text{ xor } LFSR_n(11)$$
$$LFSR_{n+1}(12) = LFSR_n(9) \text{ xor } LFSR_n(12)$$
$$LFSR_{n+1}(13) = LFSR_n(10) \text{ xor } LFSR_n(13)$$
$$LFSR_{n+1}(14) = LFSR_n(11) \text{ xor } LFSR_n(14)$$
$$LFSR_{n+1}(15) = LFSR_n(12) \text{ xor } LFSR_n(15)$$
$$LFSR_{n+1}(16) = LFSR_n(13) \text{ xor } LFSR_n(16)$$

The PRBS is applied to the data word (or useful data) as follow; the 14 LSB of the PRBS are the bits used to scramble the data.

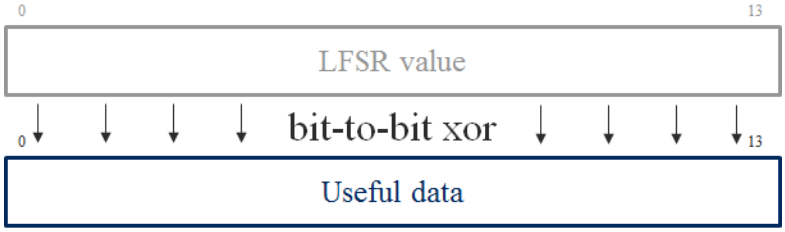


Figure 24: LFSR operation

10.2.3 Encoding

After encoding, a frame contains 16 bits (14 bits of scrambled data and 2 bits of overhead). The first overhead bit is the Clk bit; it toggles at every frame. The other is the Disparity Bit of the 14-bit scrambled data + clock bit. Its objective is to ensure deterministically the advantages brought statistically by the scrambling process.

Figure 25: Frame format after encoding

Even with scrambling, large running disparity can still occur with very low probability and could produce excessive eye shifts. These eye shifts could be balanced by a more complicated equalization stage in the receiver if the running disparity was still limited. However, a PRBS does not bind the running disparity deterministically, thus the data could be corrupted on the reception end and it could eventually cause the eye opening detection module to lose its lock. To prevent this, the disparity bit is implemented.

For each lane and for each frame, transmitter constantly calculates and monitors the running disparity.

- If the running disparity of the transmission does not increase above +/- 15 (+15 and -15 included). In this case, the disparity bit is set to '0' and the 15 bits of data (scrambled data + clk bit) are transmitted as such.
- If the running disparity of the transmission does increase above +/-15 (+15 and -15 excluded). In this case, the 15 bits of data (scrambled data + clk bit) are inverted, using a bit-to-bit not operation, and the disparity bit is set to '1'.

This disparity bit ensures that the longest possible series of '1' or '0' transmitted is of 48 bits (the clk bit reduces this value effectively to 32). The disparity bit also ensures that the running disparity does not exceed +/- 15 (included) which satisfies the DC balance condition.

In normal operating mode, the receiver will check the disparity bit (DB) first.
If DB is high then a not bitwise operation is applied on the received data, then data are descrambled.
If DB is low, data are directly descrambled.

10.3 Serial link implementation

The table below illustrates the way serial lanes are implemented depending on the considered modes (Real or Complex input data and interpolation ratio).
Note that for high output frequencies where performance is reduced (Fout > 17GHz), it is possible to send only 8-bit of data without affecting too much dynamic performance. In that case, the way of sending data is illustrated in the column 8-bit DATA case.

Table 21. Serial lanes implementation depending on modes

	12 BITS DATA SIZE				8 BITS DATA SIZE							
	REAL DATA	COMPLEX DATA			REAL DATA		COMPLEX DATA					
INTERPOLATION	1	4	8	16	1		4		8		16	
SERIAL LANE NUMBER	[11:0]	[11:0]	[11:0]	[11:0]	[11:4] 8 bits	[3:0] 4 bits	[11:4] 8 bits	[3:0] 4 bits	[11:4] 8 bits	[3:0] 4 bits	[11:4] 8 bits	[3:0] 4 bits
ASL0/BSL0	n	special data	special data	special data	n	n+1 (LSB)	special data		special data		special data	
ASL1/BSL1	n+1	n (I)	n (I)	n (I)	n+2	n+1 (MSB)	n (I)	n+1 (I) (LSB)	n (I)	unused	n (I)	unused
ASL2/BSL2	n+2	n (Q)	n (Q)	n (Q)	n+3	n+4 (LSB)	n (Q)	n+1 (Q) (LSB)	n (Q)	n+1 (Q) (LSB)	n (Q)	unused
ASL3/BSL3	n+3	n+1 (I)	n+1 (I)		n+5	n+4 (MSB)	n+2 (I)	n+1 (I) (MSB)	n+1 (I)	n+1 (Q) (MSB)		
ASL4/BSL4	n+4	n+1 (Q)	n+1 (Q)		n+6	n+7 (LSB)	n+2 (Q)	n+1 (Q) (MSB)				
ASL5/BSL5	n+5	n+2 (I)			n+8	n+7 (MSB)	n+3 (I)	unused				
ASL6/BSL6	n+6	n+2 (Q)			n+9	n+10 (LSB)	n+3 (Q)	unused				
ASL7/BSL7	n+7	n+3 (I)			n+11	n+10 (MSB)						
ASL8/BSL8	n+8	n+3 (Q)			n+12	n+13 (LSB)						
ASL9/BSL9	n+9				n+14	n+13 (MSB)						
ASL10/BSL10	n+10				n+15	unused						
ASL11/BSL11	n+11											
ASL12/BSL12	n+12											
ASL13/BSL13	n+13											
ASL14/BSL14	n+14											
ASL15/BSL15	n+15											
DATA and LANE number	16 DATA on 16 LANES	4 DATA on 8 LANES	2 DATA on 4 LANES	1 DATA on 2 LANES	16 DATA on 11 LANES		4 DATA on 6 LANES		2 DATA on 3 LANES		1 DATA on 2 LANES	
NUMBER OF ESISTREAM ENABLE	16	8+1	4+1	2+1	11		6+1		3+1		2+1	

Note:
1. Special data = HSSL0 used for fast programming of frequency hopping
2. Unused HSSLs must remain open (not connected). It is recommended to power down unused HSSLs. Refer to Table 56 and Table 57.
3. HSSLs are designed to support cold sparing (active signal while circuit is powered down)

11. MAIN FUNCTIONALITIES

11.1 Gain adjustment

A 10 bit accuracy gain tuning (5-bit Coarse and 5-bit Fine) is implemented to adjust each DAC output gain individually in the range of ±10% of the analog full-scale. A 5 bit LSB DAC is implemented within the A-SINC function and 5-bit MSB DAC is implemented within the DAC analog core block.

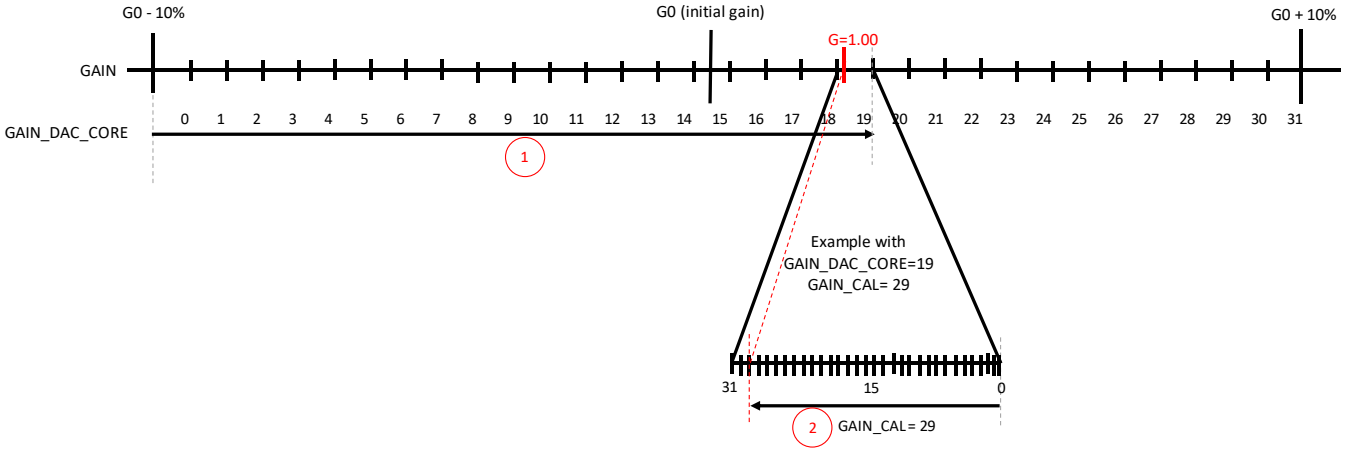


Figure 26: Gain adjustment trough x_GAIN_CAL & GAIN_DAC_CORE

The 5 LSB bit are set by SPI via registers A_ GAIN_CAL and B_GAIN_CAL.
The total gain for core x (x=A or B)

$$G = (1 - \text{x\_SINC\_GAIN\_CAL} \cdot 2^{-12})\text{x}(0.9 + \text{GAIN\_DAC\_CORE}.0.00625)$$

Example with gain attenuation:
For example, if Fout = 10MHz, NRZ mode, no Beam-Forming: If the output differential signal on OUTA has 1.07Vpp swing, this value can be adjusted to 1Vpp by applying a 1/1.07=0.934579 attenuation.
We have to adjust first the MSB part of the gain (analog adjustment). To get near 0.034579, Gain_DAC_CORE must be set to 6 (the highest integer value close to 0.034579/0.00625=5.53), so corresponding attenuation value is 0.00625*6= 0.0375 which is higher than the desired one, that is why it is necessary to use x_GAIN_CAL adjustment.

$$1 - x\_GAIN\_CAL \cdot 2^{-12} = \frac{0.934579}{0.9 + 0.0375} = 0.996884$$

We deduce that: A_ GAIN_CAL= (1-0.996884). 2^{12} ~ 13.

Example with Gain amplification:
To get a 1.073247 Gain value, we have to set: Gain_DAC_CORE = 28**,** A_GAIN_CAL= 7. We obtain: G= 1.07316.

11.2 DAC output modes

Three possible output modes are proposed and can be selected via the SPI

- Classical Non Return to Zero (NRZ) mode
- Radio Frequency (RF) mode
- 2RF mode

The output response in the different modes is represented in the graph below (assuming a 12GHz clock rate in NRZ and RF modes and 24GHz clock rate in 2RF mode) over 5 Nyquist zones.

Ideal equations describing maximum available output power versus analog output frequency in the 3 modes are given hereafter, with X being the normalized output frequency (i.e. Fout/F_C, thus the edges of the Nyquist zones are at X = 0, 1/2, 1, 3/2, 2, …)
In fact, due to limited bandwidth, an extra term must be added to take into account a first order low pass filter with a 25 GHz cut-off frequency.
In the following formula, Pout(X) is expressed in dBm.
NRZ mode:

$$Pout(X) = 20 \cdot log_{10}\left[\frac{sinc(\pi \cdot X)}{0.893}\right]$$

where: sinc(x) = sin(x)/x

RF mode:

$$Pout(X) = 20 \cdot log_{10}\left[\frac{sinc\left(\frac{\pi \cdot X}{2}\right) \cdot sin\left(\frac{\pi \cdot X}{2}\right)}{0.893}\right]$$

where:

2RF mode:

$$Pout(X) = 20 \cdot log_{10}\left[\frac{sinc\left(\frac{\pi \cdot X}{2}\right) \cdot sin\left(\frac{\pi \cdot X}{2}\right) \cdot cos(\pi X)}{0.893}\right]$$

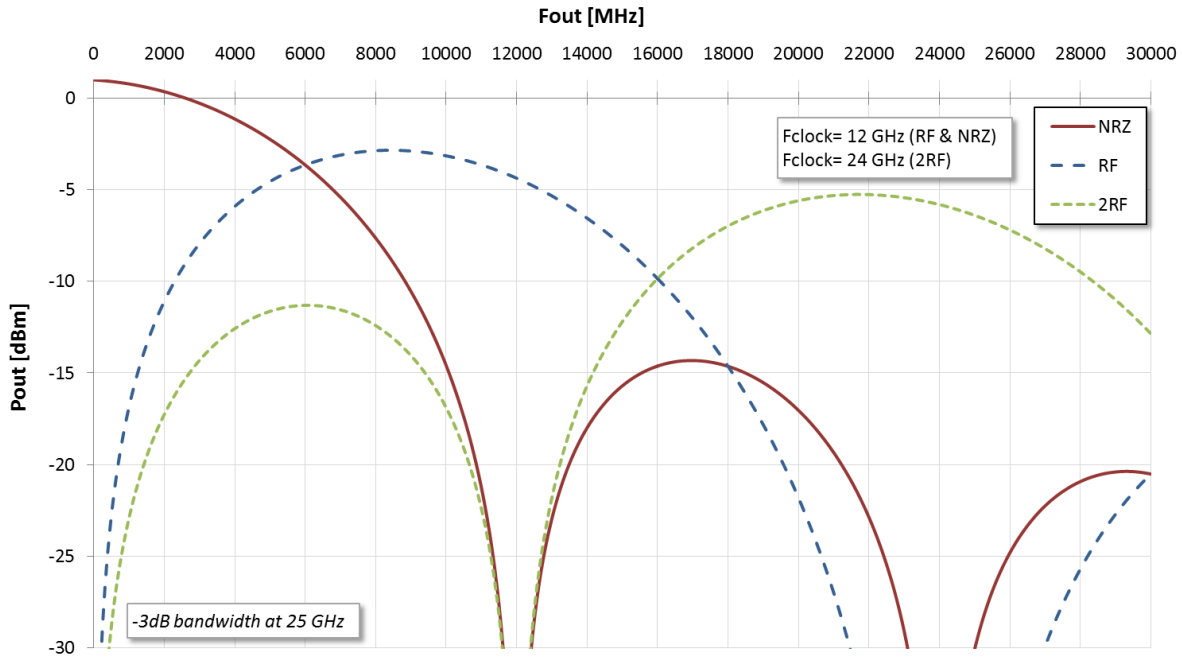


Figure 27 – Max available output power (Pout) vs output frequency (Fout) in the two output modes over four Nyquist zones

- NRZ mode offers max power for 1st operation
- RF mode offers maximum power over 2nd and 3rd Nyquist operation
- 2RF mode offers maximum power over 3rd, 4th and 5th Nyquist operation (6GHz Nyquist zone with 24GHz clock rate)

11.2.1 NRZ output mode

This mode does not allow for operation in the 2nd Nyquist zone because of the sin(x)/x notch.
The advantage is that it gives good results at the beginning of the 1st Nyquist zone; it also removes the parasitic spur at the clock frequency (in differential).
This legacy mode provides the highest output power at the beginning of the 1st Nyquist zone.

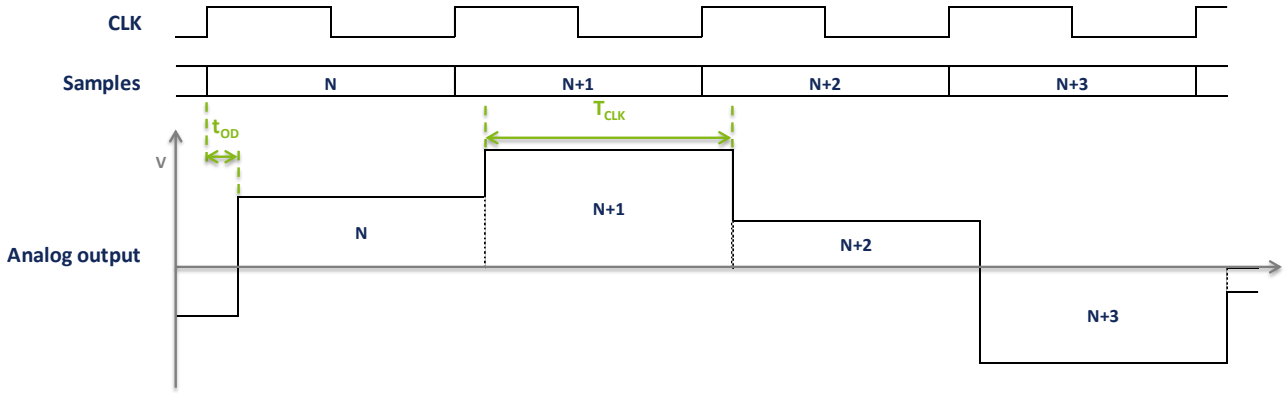


Figure 28 – NRZ mode timing diagram

11.2.2 RF output mode

RF mode is optimal for operation at high output frequency. Unlike NRZ mode, the RF mode presents notches at DC and 2N*Fs, and minimum attenuation close to Fout = Fs. (Fs corresponding to the frequency of the external clock).
Advantages:

- Optimized for operations over the second half of the 2nd Nyquist zone or over the 3rd Nyquist zone;
- Extended dynamic;

Weakness:

- By construction clock spur at Fs.
- Next clock spur pushed to 2.Fs.

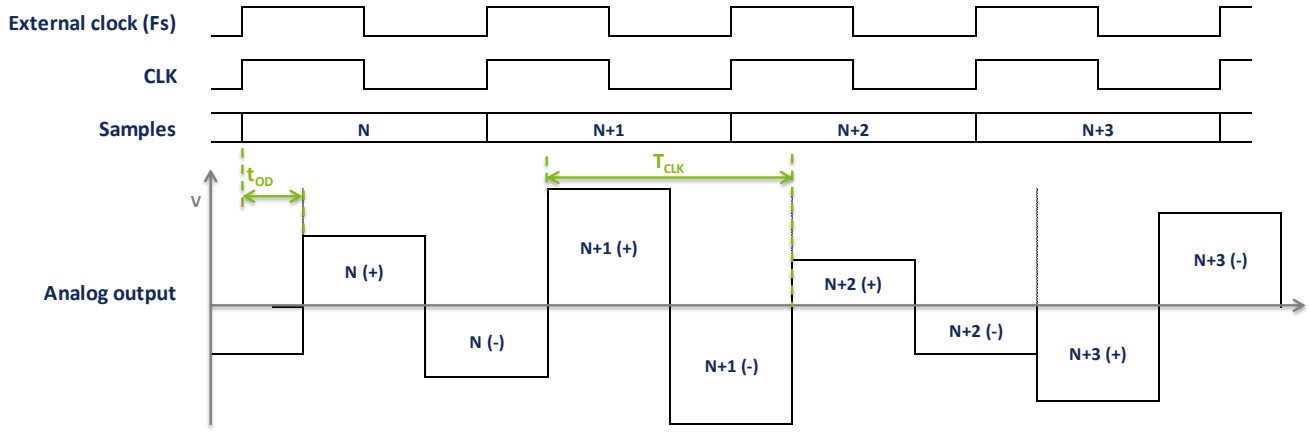


Figure 29 – RF mode timing diagram

11.2.3 2RF output mode

2RF mode is optimal for operation at high output frequency when output power of RF mode is beginning to decrease. The 2RF mode presents notches at DC and (2N+1)*Fc/2 and minimum attenuation close to Fout= Fc. (Fc corresponding to the frequency of the external clock)
Advantages:

- Optimized for operation in K-band (Fout close to Fs) (High Pout, quite flat)

Weakness:

- Requires a clock at twice the speed of NRZ or RF mode
- +130mW in this mode for a Dual DAC

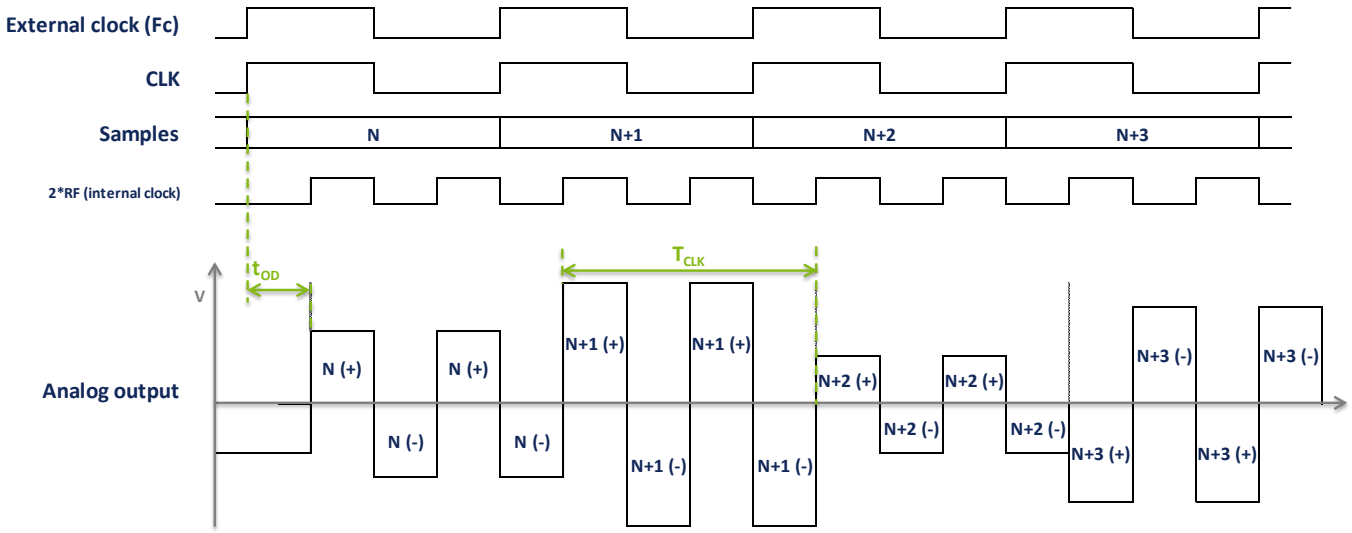


Figure 30 – 2RF mode timing diagram

11.3 Clock out

The DAC can provide to another DAC an image of its reference clock, adding 60 fs rms jitter to the reference clock.

11.4 SSO

The DAC can provide for frequency loop or synchronization a programmable ratio of the input clock to keep this reference close to 375 MHz as needed by the FPGA.

SSO output frequency = Fs/M with M equal to 32, 16, 8 or 4 and Fs the sampling frequency

In NRZ and RF mode:
Fs = Fc
For example, if Fc is 12GHz, the user have to choose the division by 32 to get 375MHz.

In 2RF mode:
Fs=Fc/2
For example, if Fc is 24GHz, the user have to choose the division by 64 to get 375MHz.

11.5 SYNC

The SYNC signal is mandatory in order to have deterministic timing for the 2 cores synchronization and for multiple component time alignment. Thus it is necessary to send a SYNC pulse after power-up so that the DAC timing circuitry starts in a deterministic way. This pulse resets the different dividers on the clock path and ensures that all

the timing circuitry restarts deterministically. It also starts the synchronization sequence of the serial interface. It also resets the test modes to their initial value.

For multiple components, clock tree will be aligned.
In order to get a deterministic alignment, a specific SPI procedure has to be launched.
(this procedure will be detailed later on)

11.6 SYNCO

The SYNC signal can be provided to another DAC for multi DAC synchronization.

11.7 Die temperature monitoring diode

Two pins are provided so that the temperature diode can be probed using standard temperature sensors. Diode C must be connected to GND. A current reference between 100µA and 1 mA is required.

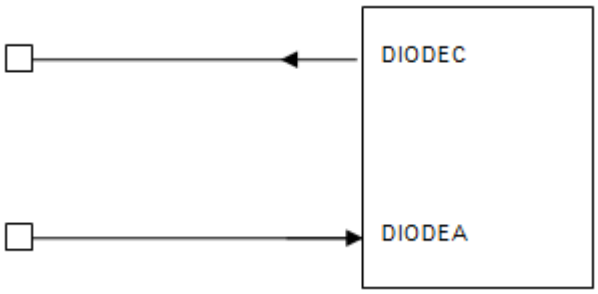


Figure 31: Temperature diode

11.8 DIGITAL processing Functions

11.8.1 Top level description

The digital signal processing implements a programmable anti-sinc filter, a programmable complex mixer, digital up conversion (DUC), beamforming and direct digital synthesis (DDS) as illustrated in Figure 32.

For each DAC, the signal processing path is made of 1 DUC containing:
- 4 interpolations stages
- 1 gain and delay stages for beam forming
- 1 sinc compensation
- 1 frequency hopping table

Frequency hopping, gain and phase stages, interpolation filter and SINC compensation block are controlled through SPI.

The DUC can be configured for interpolation with a factor of 4, 8 or 16. The complex mixer can be programmed with a frequency resolution of 32 bit. The mixer can also be programmed for DDS mode in which it generates either a CW or a chirp pattern, selectable by the user. The beamforming functionality consists of a programmable delay from -8.5 to 7.5 samples with a fractional delay resolution of 7 bit and a programmable gain with a range of ±12.5% and a resolution of 10 bit. The anti-sinc filter intended to compensate for the DAC pulse shape has two programmable coefficients.

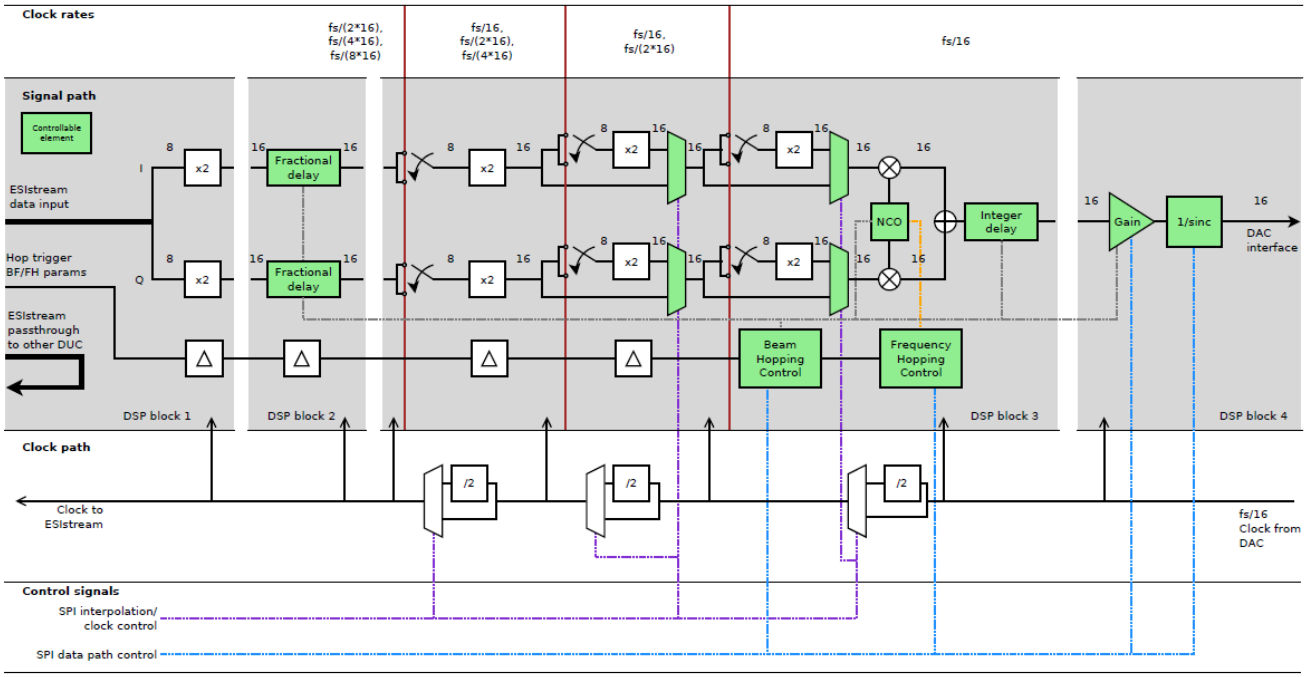


Figure 32 – Signal path with DUC

11.8.2 Interpolation

Flexible interpolation is embedded to minimize serial link data transport and simplify digital baseband processing.

The supported interpolation factors are M={1, 4, 8, 16}.
Each DAC can have different interpolation ratio.

It should be noted that interpolation by 1 (no interpolation) is only supported with real data, i.e. no I/Q.

11.8.2.1 Interpolation stage 1

Each Interpolation stage implements upsampling by 2 followed by a half-band filter. The first interpolation stage filter has been designed with 85% of a Nyquist zone bandwidth and a -70dBc ripple in the stop band. Table 22 lists the coefficients used in the filter.

Table 22. Fixed point coefficients of interpolation stage 1 filter

Index	Coefficient	Index	Coefficient	Index	Coefficient	Index	Coefficient
0	0	16	0	32	16384	48	0
1	0	17	-316	33	10396	49	218
2	0	18	0	34	0	50	0
3	8	19	448	35	-3376	51	-146
4	0	20	0	36	0	52	0
5	-16	21	-628	37	1920	53	96
6	0	22	0	38	0	54	0
7	32	23	882	39	-1264	55	-57
8	0	24	0	40	0	56	0
9	-57	25	-1264	41	882	57	32
10	0	26	0	42	0	58	0
11	96	27	1920	43	-628	59	-16
12	0	28	0	44	0	60	0
13	-146	29	-3376	45	448	61	8
14	0	30	0	46	0		
15	218	31	10396	47	-316		

In the signal path shown in Figure 33, the first interpolation factor is 4 and the fractional filter (Farrow filter described in Figure 34) is after the first interpolation by 2 stage. There are also 2 optional interpolation stages to make the overall interpolation factor 8 or 16. The fractional delay should be in the range $\pm 0.5/f_{dac}$ at the output where : f_{dac} = Fs (NRZ or RF mode) or Fs/2 in 2RF mode case.

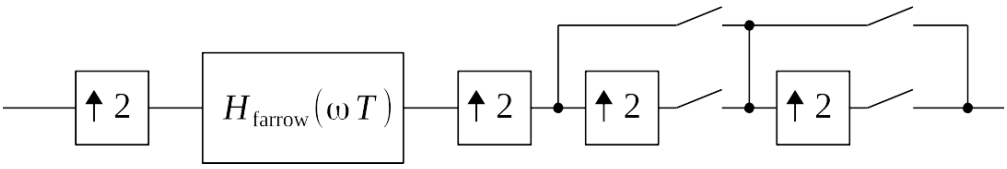
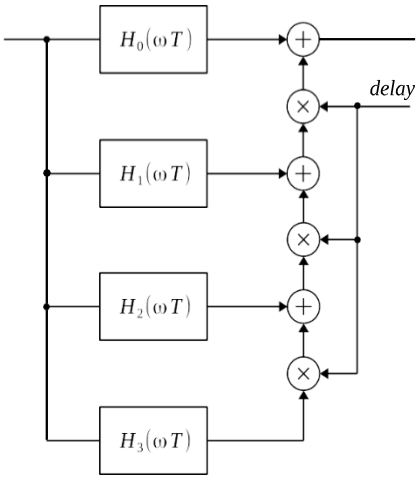


Figure 33 – Signal path before mixer

The Farrow structure is suitable for implementation of such a fractional delay filters. A delay corresponds to exp(−jωTd). The Taylor expansion is:

$$\exp(-j\omega Td) \approx 1 - j\omega Td + \frac{(j\omega Td)^2}{2} - \frac{(j\omega Td)^3}{6} + \frac{(j\omega Td)^4}{24} + \ldots$$

This can be approximated using the structure shown in Figure 34.



Where :
$H_0(\omega T) \approx 1$
$H_1(\omega T) \approx -j\omega T$
$H_2(\omega T) \approx -(\omega T)^2/2$
$H_3(\omega T) \approx j(\omega T)^3/6$

Figure 34 – Farrow filter implementation

Farrow filter is built with 4 sub-filters all with a filter order of 4. The first filter is a pure delay.
Since interpolation changes the sampling rate of the signal out of the Farrow filter the delay scales with the interpolation factor. Therefore the delay parameter must be internally scaled by the interpolation factor as shown in Table 23. First interpolation filter supports a relative signal band of 0.85.

Table 23. Delay parameter scaling vs. interpolation factor (fdac= Fs (NRZ or RF mode) or Fs/2 in 2RF mode).

M	**Delay** t_d/f_{dac}	**Delay** t_d/f_{farrow}
4	±0.5	±0.25
8	±0.5	±0.125
16	±0.5	±0.0625

As the Farrow filter is preceded by interpolation by two, the signal band is 0.85/2 = 0.425. According to the table above, the maximum range of the delay parameter is ±0.25 of a clock period at sampling rate $f_{farrow} = 2f_{dac}/M$.

11.8.2.2 Interpolation stage 2

Interpolation stage 2 implements upsampling by two followed by a half-band filter. The interpolation filter has been designed with 42.5% bandwidth and a -70dBc ripple in the stop band. 0 lists the coefficients used in the filter.

Table 24. Fixed point coefficients of interpolation stage 2 filter

Index	Coefficient	Index	Coefficient	Index	Coefficient	Index	Coefficient
0	0	7	-8	15	1248	23	-4
1	0	8	0	16	2048	24	0
2	0	9	-4	17	1248	25	-8
3	-1	10	0	18	0	26	0
4	0	11	73	19	-288	27	4
5	4	12	0	20	0	28	0
6	0	13	-288	21	73	29	-1
		14	0	22	0		

11.8.2.3 Interpolation stage 3

Interpolation stage 3 implements upsampling by two followed by a half-band filter. The interpolation filter has been designed with 21.25% bandwidth and a -70dBc ripple in the stop band. Table 25 lists the coefficients used in the filter.

Table 25. Fixed point coefficients of interpolation stage 3 filter

Index	Coefficient	Index	Coefficient
0	0	11	17
1	0	12	0
2	0	13	-113
3	0	14	0
4	0	15	608
5	0	16	1024
6	0	17	608
7	0	18	0
8	0	19	-113
9	0	20	0
10	0	21	17

11.8.2.4 Interpolation stage 4

Interpolation stage 4 implements upsampling by two followed by a half-band filter. The interpolation filter has been designed with 10.625% bandwidth and a -70dBc ripple in the stop band. Table 26 lists the coefficients used in the filter.

Table 26. Fixed point coefficients of interpolation stage 4 filter

Index	Coefficient	Index	Coefficient
0	0	10	0
1	0	11	0
2	0	12	0
3	0	13	-1
4	0	14	0
5	0	15	9
6	0	16	16
7	0	17	9
8	0	18	0
9	0	19	-1

11.8.2.5 Interpolation Filters Transfer Function

The transfer function of Interpolation filters are shown in the figures below:

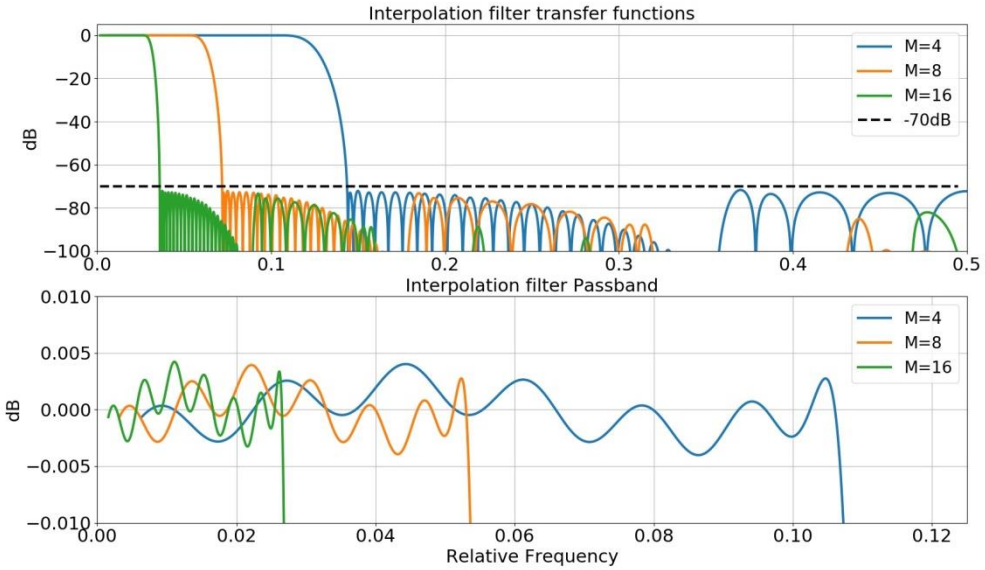


Figure 35 – Interpolation filter for orders 4, 8 and 16 and bandpass behavior for each order.

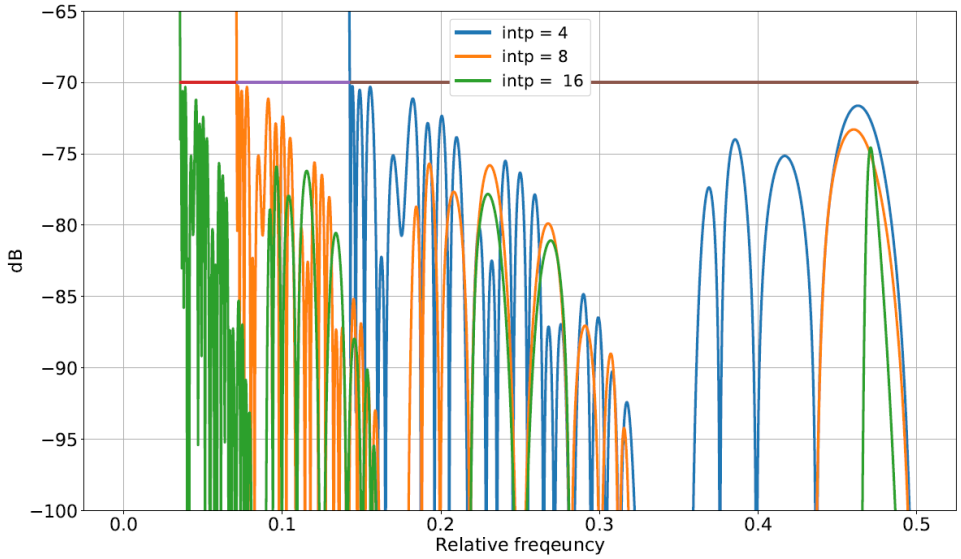


Figure 36 – Interpolation filters, zoom of stopband

Above figure represents interpolation filter frequency response that is translated by DUC. The global transfer function is symmetrical around digital Lo.

11.8.3 NCO

The NCO generates one or more sinusoidal signals. NCO is using a table combined with the CORDIC algorithm. The most significant bits are generated by the table while the least significant bits are generated by the CORDIC. The input to the sine generator is generated by an accumulator (integrator) shown in Figure 37. This signal (acc_out) is always positive and wrap at $2^{n_{acc}}$. This means that the phase of the sinusoid is:

$$ph_{sig} = 2\pi \cdot \text{acc\_out}/2^{n_{acc}}$$

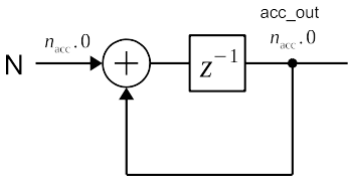


Figure 37 – Phase accumulator

11.8.4 Digital Up Conversion (DUC)

To allow better spectral efficiency, a Digital Up Conversion (DUC) is used. This complex mixer translates baseband I/Q signal to digital LO frequency, thanks to a programmable 32 bit numerically controlled oscillator (NCO), set by SPI. The tuning is done with NCO and allows phase alignment between two DAC outputs.

Digital LO frequency=fdac * $NCOregister/2^{32}$
With fdac = Fs (NRZ or RF mode) or Fs/2 in 2RF mode

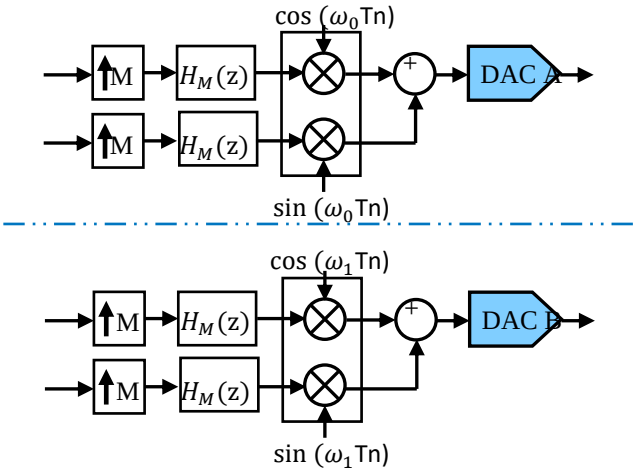


Figure 38 – Digital Up Conversion Block diagram

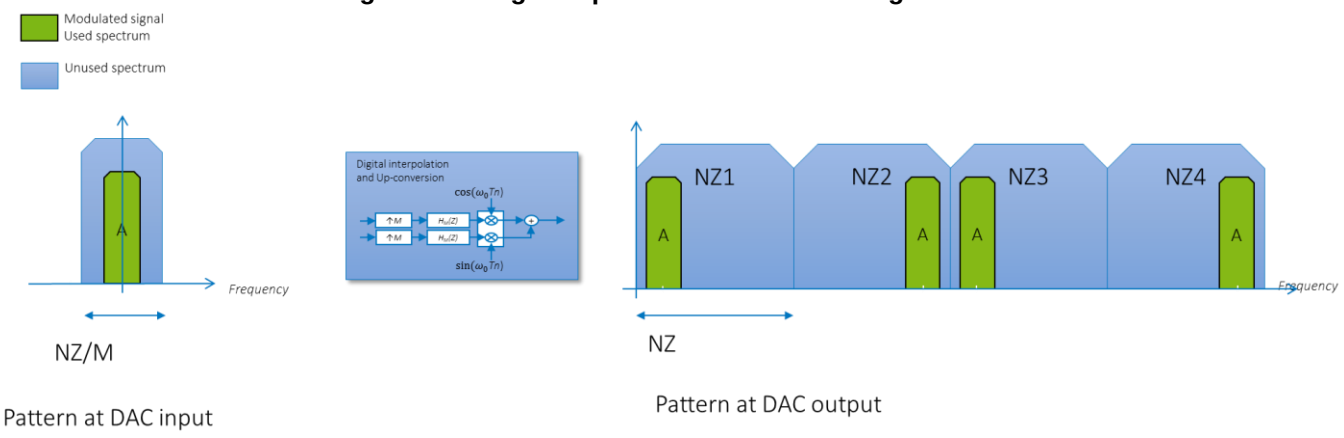


Figure 39 – Digital Up Conversion Principle

Each DAC has its own DUC pattern. Only one NCO frequency is possible for each DAC. This NCO frequency is set by SPI and can be different for each DAC as illustrated on the figure below.

11.8.5 Beamforming and beam-hopping

Instead of setting gain and phase on board, this DAC proposes “Beam Forming” to compensate this parameter digitally as depicted hereafter. The same input data is provided to both DAC cores cutting by 2 the number of required serial lanes but DAC gain/delay control is individual.

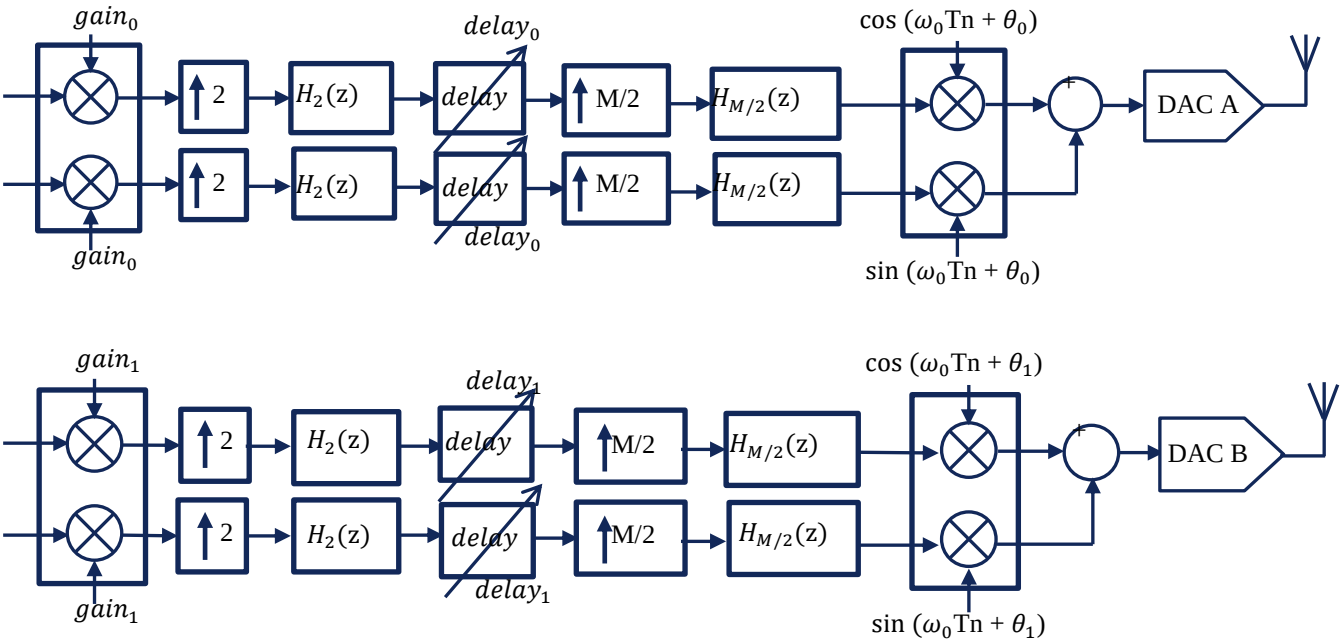


Figure 40 – Beam-forming (Digital Butler Matrix) principle

The DAC integrates a beam hopping which modifies beam-forming parameters (time delay and gain) dynamically when beam-forming is used, allowing new beam characteristics (loop on 2, 3 or 4 locations). SPI is used to program the 4 setting sets for time delay and gain. Input data flux is sent to DAC B only.
An on-board programmable 4-state beam hopping pattern register bank can allow pre compute beam plan.
It is possible to do the loop on only 2 or 3 settings (selection of the number of locations is done via SPI).
The N settings (gain on 10 bit and coarse time delay on 7 bit and fine time delay on 4 bit) are written in SPI registers via 3*N SPI instructions.

In order to switch from setting S to setting S+1, a trigger must be sent in write only register TRIG_BH.

The delay can be implemented as a time delay or a phase shifter as shown in Figure 41. Using time delay is preferred since phase shifters cause squinting, i.e. the direction of the beam will be frequency dependent.

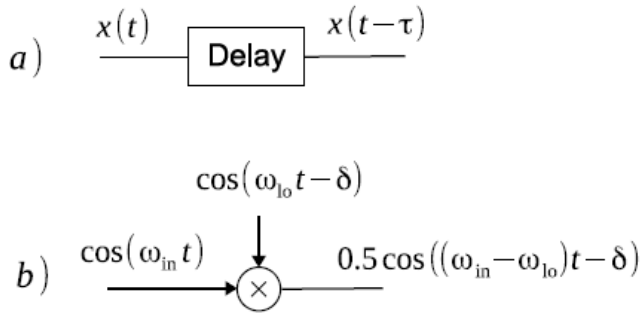


Figure 41 – Time delay a) and phase shifter b)

The delay in the signal path is implemented as a fractional delay filter where the delay can be up to 0.5 clock cycle (it is also possible to add whole clock cycles of delay). The sampling rate of the filter depends on the interpolation factor.

Table 27. Beam-forming/Beam-hopping specifications

	Specification
Gain resolution	10 bit
Gain range	±12.5% of DAC Full Scale
Time delay fine adjustment	7 bit Range: ±0.5*Ts
Time delay coarse adjustment	4 bit (step of Ts) Range: 15 Ts (Ts being the sampling period)

The sampling rate for different interpolation factors is shown in the table below.

Table 28. Delay Filter Sampling Rate vs. Interpolation factor

Interpolation factor	Fs = 1/Ts
4	$f_{dac}/2$
8	$f_{dac}/4$
16	$f_{dac}/8$

With fdac = Fs (NRZ or RF mode) or Fs/2 in 2RF mode
SPI is used to program beamforming parameters (Gain and Time delay) on each DAC Core. Input data flux is sent to DAC B only (HSSLs from DAC A can be powered down).

The gain and time delay settings are written in SPI registers via 3 SPI instructions (1 SPI instruction for Gain and 2 SPI instructions for Time delay). Then one SPI instruction for trigger (TRIG_BH) is needed to activate the programmed settings.

11.8.5.1 Procedure for BEAM-HOPPING or BEAM-FORMING with interpolation by 4

In this mode, 8 serial links on the B side are powered ON
The following SPI instructions must be added before the SYNC signal:

```
WRITE @INTERPOL_MODE                0x 0005
WRITE @FH_HSSL0_ENA                 0x 0000

WRITE @A_HSSL_POWER_ON              0x 0000     (optional, to save power)
WRITE @B_HSSL_POWER_ON              0x 01FE     (optional, to save power)
```

- ⇨ All serial links on core A are powered OFF
- ⇨ BSL0, BSL9, BSL10, BSL11, BSL12, BSL13, BSL14, BSL15 are powered OFF

Then continue with the BEAM HOPPING procedure (refer to 11.8.5.5) or BEAM FORMING procedure (refer to 11.8.5.4)

11.8.5.2 Procedure for BEAM-HOPPING or BEAM-FORMING with interpolation by 8

In this mode, only 4 serial links on the B side are powered ON
The following SPI instructions must be added before the SYNC signal:

```
WRITE @INTERPOL_MODE                0x 000A
WRITE @FH_HSSL0_ENA                 0x 0000

WRITE @A_HSSL_POWER_ON              0x 0000     (optional, to save power)
```


WRITE @B_HSSL_POWER_ON 0x 001E (optional, to save power)
- ⇨ All serial links on core A are power off
- ⇨ BSL0, BSL5, BSL6, BSL7, BSL8, BSL9, BSL10, BSL11, BSL12, BSL13, BSL14, BSL15 are powered OFF

Then continue with the BEAM HOPPING procedure (refer to 11.8.5.5) or BEAM FORMING procedure (refer to 11.8.5.4)

11.8.5.3 Procedure for BEAM-HOPPING or BEAM-FORMING with interpolation by 16

In this mode, only 2 serial links on the B side are powered ON
The following SPI instructions must be added before the SYNC signal:

WRITE @INTERPOL_MODE 0x 000F
WRITE @FH_HSSL0_ENA 0x 0000

WRITE @A_HSSL_POWER_ON 0x 0000 (optional, to save power)
WRITE @B_HSSL_POWER_ON 0x 0006 (optional, to save power)
- ⇨ All serial link core A are power off
- ⇨ BSL0, BSL3, BSL4, BSL5, BSL6, BSL7, BSL8, BSL9, BSL10, BSL11, BSL12, BSL13, BSL14, BSL15 are powered OFF

Then continue with the BEAM FORMING procedure (refer to 11.8.5.4) or BEAM HOPPING procedure (refer to 11.8.5.5).

11.8.5.4 Procedure for BEAM-FORMING

RESET (active at low level, 100 ns min)
WRITE @FH_HSSL0_ENA 0x 0000

WRITE @A_NCO_LSB 0x ---- (16 bits for the NCO[15:0] core A)
WRITE @A_NCO_MSB 0x ---- (16 bits for the NCO[31:16] core A)
WRITE @B_NCO_LSB 0x ---- (16 bits for the NCO[15:0] core B)
WRITE @B_NCO_MSB 0x ---- (16 bits for the NCO[31:16] core B)

WRITE @A_BH_GAIN_ZONE1 0x ----
WRITE @B_BH_GAIN_ZONE1 0x ----
WRITE @A_BH_DELAY_COARSE_ZONE1 0x ----
WRITE @B_BH_DELAY_COARSE_ZONE1 0x ----
WRITE @A_BH_DELAY_FINE_ZONE1 0x ----
WRITE @B_BH_DELAY_FINE_ZONE1 0x ----

WRITE @TRIGGER_ENA 0x 0003
WRITE @BEAM_ENA 0x 0004 (BEAM FORMING mode enable)
WRITE @DUC_LOAD_NCO 0x 0007
WRITE @OTP_LOADING 0x 0000
- ⇨ Wait 200 µs between the end of the RESET and OTP_LOADING instruction
- ⇨ The OTP_LOADING instruction loads OTPs (factory configuration) in the SPI register

SYNC

WRITE @TRIG_BH 0x 0000 (TRIG FOR CORE A & B)
- ⇨ BEAM parameters are taken into account after the TRIG_BH instruction

11.8.5.5 Procedure for BEAM-HOPPING

RESET
WRITE @FH_HSSL0_ENA 0x 0000

WRITE @A_NCO_LSB	0x ----	(16 bits for the NCO[15:0] core A)
WRITE @A_NCO_MSB	0x ----	(16 bits for the NCO[31:16] core A)
WRITE @B_NCO_LSB	0x ----	(16 bits for the NCO[15:0] core B)
WRITE @B_NCO_MSB	0x ----	(16 bits for the NCO[31:16] core B)
WRITE @A_BH_GAIN_ZONE1	0x ----	
WRITE @B_BH_GAIN_ZONE1	0x ----	
WRITE @A_BH_DELAY_COARSE_ZONE1	0x ----	
WRITE @B_BH_DELAY_COARSE_ZONE1	0x ----	
WRITE @A_BH_DELAY_FINE_ZONE1	0x ----	
WRITE @B_BH_DELAY_FINE_ZONE1	0x ----	
WRITE @A_BH_GAIN_ZONE2	0x ----	
WRITE @B_BH_GAIN_ZONE2	0x ----	
WRITE @A_BH_DELAY_COARSE_ZONE2	0x ----	
WRITE @B_BH_DELAY_COARSE_ZONE2	0x ----	
WRITE @A_BH_DELAY_FINE_ZONE2	0x ----	
WRITE @B_BH_DELAY_FINE_ZONE2	0x ----	
WRITE @A_BH_GAIN_ZONE3	0x ----	
WRITE @B_BH_GAIN_ZONE3	0x ----	
WRITE @A_BH_DELAY_COARSE_ZONE3	0x ----	
WRITE @B_BH_DELAY_COARSE_ZONE3	0x ----	
WRITE @A_BH_DELAY_FINE_ZONE3	0x ----	
WRITE @B_BH_DELAY_FINE_ZONE3	0x ----	
WRITE @A_BH_GAIN_ZONE4	0x ----	
WRITE @B_BH_GAIN_ZONE4	0x ----	
WRITE @A_BH_DELAY_COARSE_ZONE4	0x ----	
WRITE @B_BH_DELAY_COARSE_ZONE4	0x ----	
WRITE @A_BH_DELAY_FINE_ZONE4	0x ----	
WRITE @B_BH_DELAY_FINE_ZONE4	0x ----	
WRITE @TRIGGER_ENA	0x 0003	
WRITE @BEAM_ENA	0x 0007	
⇨ BEAM HOPPING mode enable with 4 zones		
⇨ WRITE @BEAM_ENA 0006 for 3 zones		
⇨ WRITE @BEAM_ENA 0005 for 2 zones		
WRITE @DUC_LOAD_NCO	0x 0007	
WRITE @OTP_LOADING	0x 0000	

SYNC

WRITE @TRIG_BH	0x 0000	(TRIG FOR CORE A & B)
WAIT (parameters zone 1 are applied until next TRIG_BH)		
WRITE @TRIG_BH	0x 0000	(TRIG FOR CORE A & B)
WAIT (parameters zone 2 are applied until next TRIG_BH)		
WRITE @TRIG_BH	0x 0000	(TRIG FOR CORE A & B)
WAIT (parameters zone 3 are applied until next TRIG_BH)		
WRITE @TRIG_BH	0x 0000	(TRIG FOR CORE A & B)
WAIT (parameters zone 4 are applied until next TRIG_BH)		
WRITE @TRIG_BH	0x 0000	(TRIG FOR CORE A & B)
WAIT (parameters zone 1 are applied until next TRIG_BH)		
WRITE @TRIG_BH	0x 0000	(TRIG FOR CORE A & B)
WAIT (parameters zone 2 are applied until next TRIG_BH)		

And so on …

Note:
It is possible to switch only core A BEAM parameters or only core B BEAM parameters.
WRITE @A_TRIG_BH 0x 0000 ➔ switch beam parameters from zone n to zone n+1 for core A only
WRITE @B_TRIG_BH 0x 0000 ➔ switch beam parameters from zone n to zone n+1 for core B only

Function	Associated SPI registers	Description
BEAM HOPPING	A BH GAIN ZONE1	Refer to Table 132
	A BH DELAY COARSE ZONE1	Refer to Table 133
	A BH DELAY FINE ZONE1	Refer to Table 134
	A BH GAIN ZONE2	Refer to Table 135
	A BH DELAY COARSE ZONE2	Refer to Table 136
	A BH DELAY FINE ZONE2	Refer to Table 137
	A BH GAIN ZONE3	Refer to Table 138
	A BH DELAY COARSE ZONE3	Refer to Table 139
	A BH DELAY FINE ZONE3	Refer to Table 140
	A BH GAIN ZONE4	Refer to Table 141
	A BH DELAY COARSE ZONE4	Refer to Table 142
	A BH DELAY FINE ZONE4	Refer to Table 143
	B BH GAIN ZONE1	Refer to Table 145
	B BH DELAY COARSE ZONE1	Refer to Table 146
	B BH DELAY FINE ZONE1	Refer to Table 147
	B BH GAIN ZONE2	Refer to Table 148
	B BH DELAY COARSE ZONE2	Refer to Table 149
	B BH DELAY FINE ZONE2	Refer to Table 150
	B BH GAIN ZONE3	Refer to Table 151
	B BH DELAY COARSE ZONE3	Refer to Table 152
	B BH DELAY FINE ZONE3	Refer to Table 153
	B BH GAIN ZONE4	Refer to Table 154
	B BH DELAY COARSE ZONE4	Refer to Table 155
	B BH DELAY FINE ZONE4	Refer to Table 156
	TRIGGER ENA	Refer to Table 44
	BEAM ENA	Refer to Table 42
	A BH CLEAR PHASE	Refer to Table 131
	B BH CLEAR PHASE	Refer to Table 144
	A TRIG BH	Refer to Table 54
	B TRIG BH	Refer to Table 55
	FH HSSL0 ENA (must be set to 0)	Refer to Table 45
	TRIG BH	Refer to Table 53

	A_HSSL_POWER_ON	Refer to Table 56
	B_HSSL_POWER_ON	Refer to Table 57

Function	Associated SPI registers	Description
BEAM FORMING	A_BH_GAIN_ZONE1	Refer to Table 132
	A_BH_DELAY_COARSE_ZONE1	Refer to Table 133
	A_BH_DELAY_FINE_ZONE1	Refer to Table 134
	B_BH_GAIN_ZONE1	Refer to Table 145
	B_BH_DELAY_COARSE_ZONE1	Refer to Table 146
	B_BH_DELAY_FINE_ZONE1	Refer to Table 147
	TRIGGER_ENA	Refer to Table 44
	BEAM_ENA	Refer to Table 42
	A_BEAMHOP_CLEAR_PHASE_ON_HO	Refer to Table 131
	B_BEAMHOP_CLEAR_PHASE_ON_HO	Refer to Table 144
	A_TRIG_BH	Refer to Table 54
	B_TRIG_BH	Refer to Table 55
	FH_HSSL0_ENA must be set to 0	Refer to Table 45
	TRIG_BH	Refer to Table 53
	A_HSSL_POWER_ON	Refer to Table 56
	B_HSSL_POWER_ON	Refer to Table 57

11.8.6 Digital Direct Synthesis (DDS) & Chirp mode

11.8.6.1 DDS mode

The mixer can also be programmed for DDS mode in which it generates either a CW or a chirp pattern or a ramp, selectable by the user.

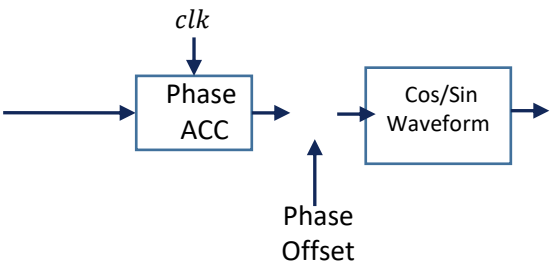


Figure 42 shows a diagram of the programmable complex mixer. In DDS/chirp mode the normal input signal is disconnected and replaced by a constant amplitude.
The NCO is used to generate sine wave pattern. SPI is used to program frequency, phase, offset and amplitude parameters. Refreshing time is 6 SPI instructions @ 100MHz.
The NCO value is used to select the frequency of the sinewave.

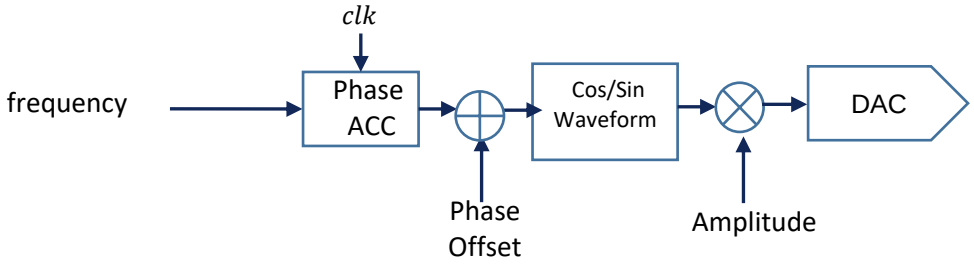


Figure 42 – Direct Digital Synthesis Principle

The DDS settings are programmed in writing the following registers:

- Registers A_NCO_LSB, A_NCO_MSB for NCO frequency (B_NCO_LSB and B_NCO_MSB for core B)
- Register A_DDS_AMPLITUDE for DDS amplitude (B_DDS_AMPLITUDE for core B)
- Registers A_PHASE_OFFSET_LSB and A_PHASE_OFFSET_MSB for DDS phase offset (B_PHASE_OFFSET_LSB and B_PHASE_OFFSET_MSB for core B)
- Then one SPI instruction for trigger is needed to activate the setting (write in A_ TRIG_FH_CHIRP or B_ TRIG_FH_CHIRP register or TRIG_FH_CHIRP to trig A & B core simultaneously).

Note: it is possible to replace the sinewave by a ramp when A_DDS_RAMP_MODE or B_DDS_RAMP_MODE are set to 1.

11.8.6.1.1 Procedure DDS mode core B

RESET (active at low level, 100 ns min)		(mandatory)
WRITE @B_HSSL_POWER_ON	0x 0000	(optional, to save power)
WRITE @INTERPOL_MODE	0b 11--	(low power mode)
WRITE @B_DDS AMPLITUDE	0x ----	
WRITE @B_NCO_LSB	0x ----	(16 bits for the NCO[15: 0])
WRITE @B_NCO_MSB	0x ----	(16 bits for the NCO[31:16])
WRITE @B_PHASE_OFFSET_LSB	0x ----	
WRITE @B_PHASE_OFFSET_MSB	0x ----	
WRITE @B_CHIRP_RESET_TO_ZERO	0x 0000	(mandatory)
WRITE @DDS_ENA	0b 001---	
WRITE @DUC_LOAD_NCO	0x 0007	
WRITE @OTP_LOADING	0x 0000	
SYNC		

Note: If a second SYNC is sent, a new sinus will start.
Note: if NCO or DDS_AMPLITUDE parameters are updated; they will not be taken into account automatically. They will be taken into account on the next SYNC signal.

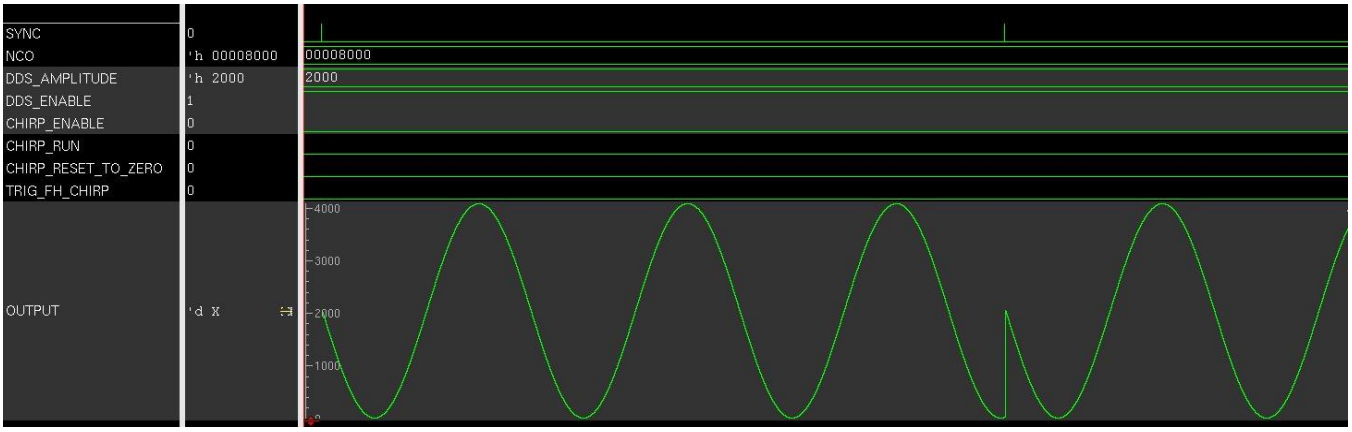


Figure 43 – DDS mode

11.8.6.1.2 Procedure DDS mode core A

RESET (active at low level, 100 ns min)

WRITE @A_HSSL_POWER_ON	0x 0000	(optional, to save power)
WRITE @INTERPOL_MODE	0b --11	(for low power mode)
WRITE @A_DDS AMPLITUDE	0x ----	
WRITE @A_NCO_LSB	0x ----	(16 bits for the NCO[15:0])
WRITE @A_NCO_MSB	0x ----	(16 bits for the NCO[31:16])
WRITE @A_ CHIRP_RESET_TO_ZERO	0x 0000	(mandatory)
WRITE @DDS_ENA	0b ---001	
WRITE @DUC_LOAD_NCO	0x 0007	
WRITE @OTP_LOADING	0x 0000	

SYNC

11.8.6.1.3 Procedure DDS mode core B + update NCO and amplitude parameters

RESET (active at low level, 100 ns min)

WRITE @B_HSSL_POWER_ON	0x 0000	(optional, to save power)
WRITE @INTERPOL_MODE	0b 11--	(optional, to save power)
WRITE @B_DDS AMPLITUDE	0x ----	
WRITE @B_NCO_LSB	0x ----	(16 bit for the NCO[15:0])
WRITE @B_NCO_MSB	0x ----	(16 bit for the NCO[31:16])
WRITE @B_ CHIRP_RESET_TO_ZERO	0x 0000	(mandatory)
WRITE @DDS_ENA	0b 001---	
WRITE @TRIGGER_ENA	0b 1-	
WRITE @DUC_LOAD_NCO	0x 0007	
WRITE @OTP_LOADING	0x 0000	

SYNC

WRITE @B_DDS AMPLITUDE	0x ----	
WRITE @B_NCO_LSB	0x ----	
WRITE @B_NCO_MSB	0x ----	
WRITE @B_TRIG_FH_CHIRP	0x 0000	(new parameters are taken into account)

11.8.6.1.4 Procedure DDS mode core A + update NCO and amplitude parameters

RESET (active at low level, 100 ns min)

WRITE @A_HSSL_POWER_ON	0x 0000	(optional, to save power)
WRITE @INTERPOL_MODE	0b --11	(optional, to save power)
WRITE @A_DDS AMPLITUDE	0x ----	
WRITE @A_NCO_LSB	0x ----	(16 bit for the NCO[15:0])
WRITE @A_NCO_MSB	0x ----	(16 bit for the NCO[31:16])
WRITE @A_ CHIRP_RESET_TO_ZERO	0x 0000	(mandatory)
WRITE @DDS_ENA	0b ---001	
WRITE @TRIGGER_ENA	0b -1	
WRITE @DUC_LOAD_NCO	0x 0007	
WRITE @OTP_LOADING	0x 0000	

SYNC

WRITE @A_DDS AMPLITUDE	0x ----	
WRITE @A_NCO_LSB	0x ----	
WRITE @A_NCO_MSB	0x ----	
WRITE @A_TRIG_FH_CHIRP	0x 0000	

11.8.6.1.5 Procedure DDS mode core A and B + update NCO and amplitude parameters

Replace @A_TRIG_FH_CHIRP and @B_TRIG_FH_CHIRP by @TRIG_FH_CHIRP

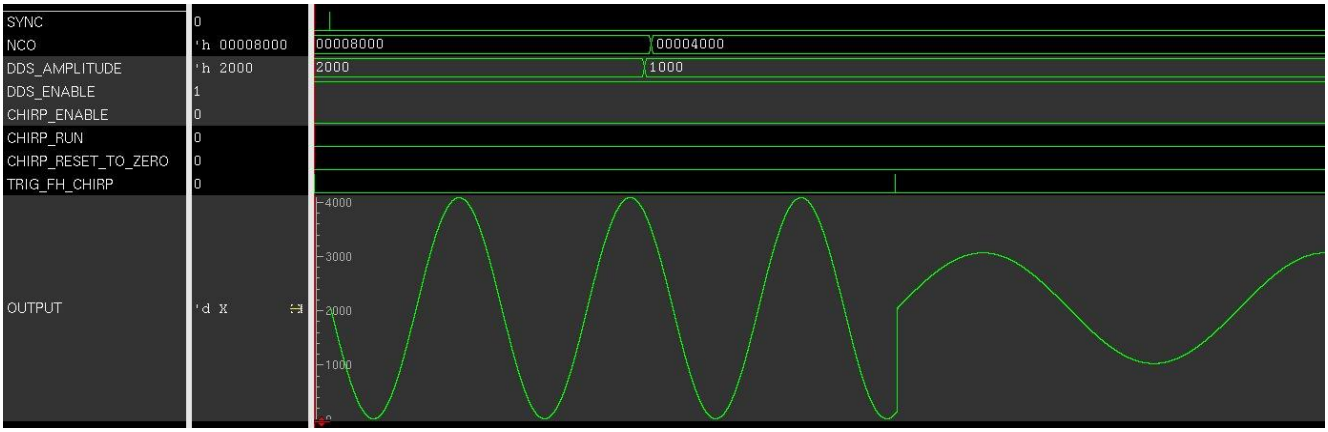


Figure 44 – DDS mode + NCO update

11.8.6.2 Chirp mode

The DDS can alternatively be programmed to generate a frequency sweep with a settable range and rate.. The frequency sweep can either be repeated continuously or generated only once in one-shot mode. Triggering is issued either with an SPI write (write in A_TRIG_FH_CHIRP or B_ TRIG_FH_CHIRP register or TRIG_FH_CHIRP to trig A & B core simultaneously).

After setting up the frequency start, stop and step parameters a trigger starts the generation of a synthesized sine wave pattern at the set starting frequency. Every 16th sample the frequency is increased using the set step size until the frequency reaches the set stop frequency.

$$Chirp\ sweep\ rate\ = \frac{Chirp\ stop\ frequency - Chirp\ start\ frequency}{Chirp\ duration}$$

The Chirp sweep rate (Hz/s) is settable from $Fs^2 / 2^{36}$ to $Fs^2 / 2^5$.

Frequency words calculation:

$$\text{Chirp step frequency word } = integer(\frac{2^{36}}{(fs)^2} sweep\ rate - 1)$$

$$Chirp\ start\ frequency\ word = integer(2^{32}.\frac{fstart}{fs})$$

$$Chirp\ stop\ frequency\ word = integer(2^{32}.\frac{fstop}{fs})$$

With:

Chirp step frequency word for core A = A_CHIRP_STEP_FREQ_MSB & A_CHIRP_STEP_FREQ_LSB
Chirp start frequency word for core A = A_CHIRP_MIN_FREQ_MSB & A_CHIRP_MIN_FREQ_LSB
Chirp stop frequency word for core A = A_CHIRP_MAX_FREQ_MSB & A_CHIRP_MAX_FREQ_LSB

Chirp step frequency word for core B = B_CHIRP_STEP_FREQ_MSB & B_CHIRP_STEP_FREQ_LSB
Chirp start frequency word for core B = B_CHIRP_MIN_FREQ_MSB & B_CHIRP_MIN_FREQ_LSB
Chirp stop frequency word for core B = B_CHIRP_MAX_FREQ_MSB & B_CHIRP_MAX_FREQ_LSB

Note: Highest sweep rates are not usable since they go through the whole Nyquist band in 16 clock cycles.
Start and stop frequencies must remain within the same Nyquist Zone.

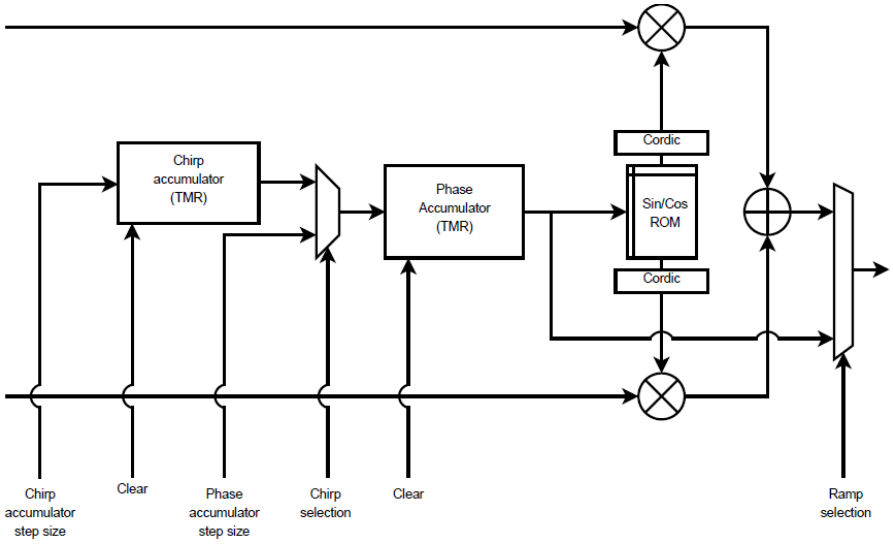


Figure 45 – Complex mixer configuration for Chirp function

The amplitude of the frequency sweep is controlled using the DDS amplitude parameter.

11.8.6.2.1 Procedure CHIRP triggered mode core A

```
RESET
WRITE @INTERPOL_MODE                0b --11
WRITE @A_DDS AMPLITUDE              0x ----
WRITE @A_CHIRP_MIN_FREQ_LSB         0x ----
WRITE @A_CHIRP_MIN_FREQ_MSB         0x ----
WRITE @A_CHIRP_MAX_FREQ_LSB         0x ----
WRITE @A_CHIRP_MAX_FREQ_MSB         0x ----
WRITE @A_CHIRP_STEP_FREQ_LSB        0x ----
WRITE @A_CHIRP_STEP_FREQ_MSB        0x ----
WRITE @A_CHIRP_REPEAT               0x 0000     (just one chirp , no repetition)
WRITE @A_CHIRP_RESET_TO_ZERO        0x 0001     (return to zero after chir)
WRITE @DDS_ENA                      0b ---111
WRITE @DUC_LOAD_NCO                 0x 0007
WRITE @OTP_LOADING                  0x 0000
WRITE @TRIGGER_ENA                  0b -1              (ENABLE TRIG)
SYNC
WAIT
WRITE  @A_TRIG_FH_CHIRP             0x 0000     (TRIG 1)
WAIT
WRITE  @A_TRIG_FH_CHIRP             0x 0000     (TRIG  2)
WAIT
```

11.8.6.2.2 Procedure CHIRP triggered mode core B

```
RESET
WRITE @INTERPOL_MODE                0b 11--
WRITE @B_DDS AMPLITUDE              0x ----
WRITE @B_CHIRP_MIN_FREQ_LSB         0x ----
WRITE @B_CHIRP_MIN_FREQ_MSB         0x ----
WRITE @B_CHIRP_MAX_FREQ_LSB         0x ----
WRITE @B_CHIRP_MAX_FREQ_MSB         0x ----
WRITE @B_CHIRP_STEP_FREQ_LSB        0x ----
WRITE @B_CHIRP_STEP_FREQ_MSB        0x ----
WRITE @B_CHIRP_REPEAT               0x 0000
WRITE @B_CHIRP_RESET_TO_ZERO        0x 0001
WRITE @DDS_ENA                      0b 111---
WRITE @TRIGGER_ENA                  0b 1-
WRITE @DUC_LOAD_NCO                 0x 0007
```

```
WRITE @OTP_LOADING                0x 0000
SYNC
WAIT

WRITE  @B_TRIG_FH_CHIRP           0x 0000      (TRIG 1)
WAIT

WRITE  @B_TRIG_FH_CHIRP           0x 0000      (TRIG 2)
WAIT
```

11.8.6.2.3 Procedure CHIRP triggered mode core A & B

Replace @A_TRIG_FH_CHIRP and @B_TRIG_FH_CHIRP by @TRIG_FH_CHIRP

With just one TRIG (TRIG 1) for one CHIRP:

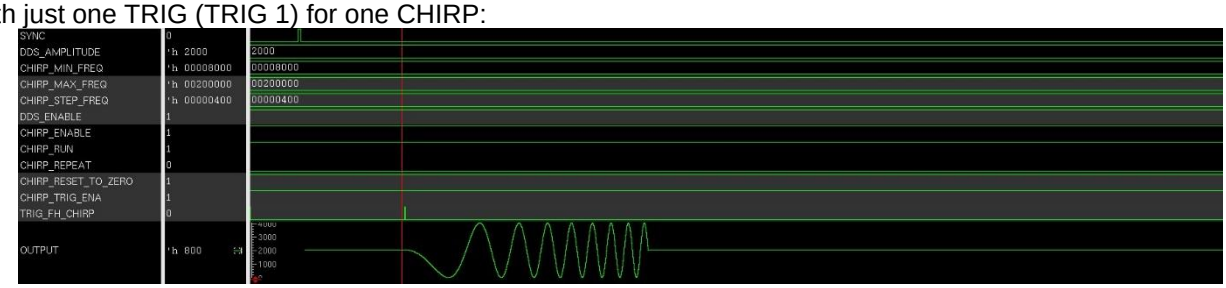


Figure 46 – Chirp mode – Single pattern

With two TRIG (TRIG 1 and TRIG 2) for two CHIRP:

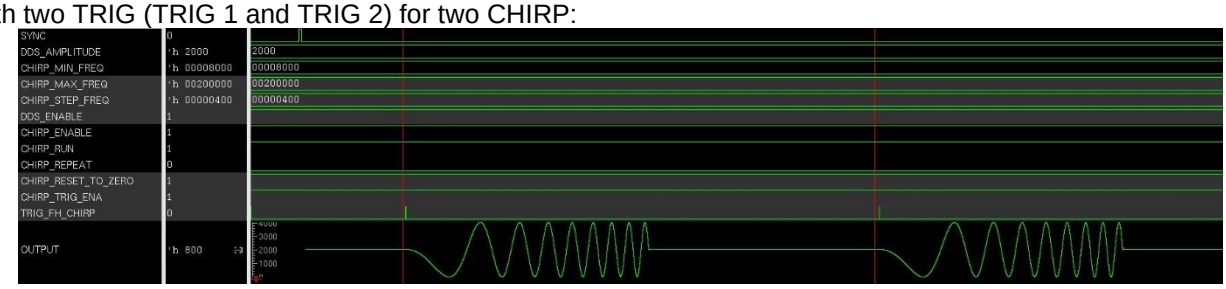


Figure 47 – Chirp mode – Several patterns

11.8.6.2.4 Procedure CHIRP mode with automatic repeat

Replace “WRITE @A_CHIRP_REPEAT 0000” by “WRITE @A_CHIRP_REPEAT 0001” for CORE A or “WRITE @B_CHIRP_REPEAT 0000” by “WRITE @B_CHIRP_REPEAT 0001” for CORE B.

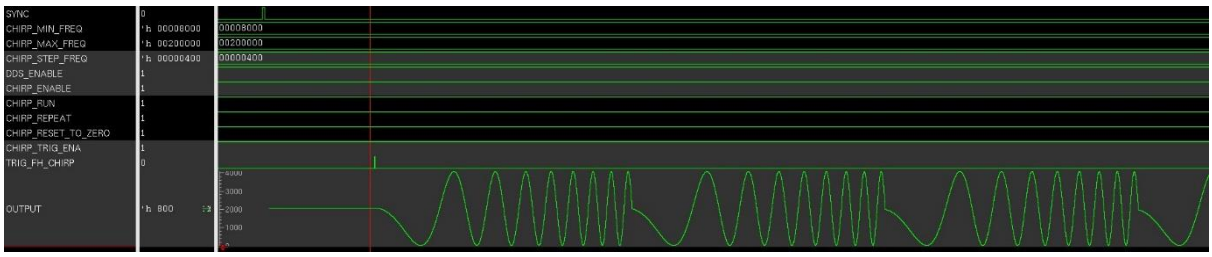


Figure 48 – Chirp mode – Automatic repeat pattern

Function	Associated SPI registers	Description
DDS	A_DDS AMPLITUDE	Refer to Table 129
	B DDS AMPLITUDE	Refer to Table 130
	A NCO LSB	Refer to Table 117
	B NCO LSB	Refer to Table 119
	A NCO MSB	Refer to Table 118

	A PHASE OFFSET LSB	Refer to Table 123
	A PHASE OFFSET MSB	Refer to Table 124
	B PHASE OFFSET LSB	Refer to Table 127
	B PHASE OFFSET MSB	Refer to Table 128
	B NCO MSB	Refer to Table 120
	DDS ENA	Refer to Table 43
	A TRIG FH CHIRP	Refer to Table 51
	B TRIG FH CHIRP	Refer to Table 52
	TRIG FH CHIRP	Refer to Table 50
	A_ CHIRP_RESET_TO_ZERO must be set to 0	Refer to Table 108
	B_ CHIRP_RESET_TO_ZERO must be set to 0	Refer to Table 116
	FH_HSSL0_ENA must be set to 0	Refer to Table 45
	TRIGGER ENA	Refer to Table 44
	A HSSL POWER ON	Refer to Table 56
	B HSSL POWER ON	Refer to Table 57

Function	Associated SPI registers	Description
DDS CHIRP	A DDS AMPLITUDE	Refer to Table 129
	B DDS AMPLITUDE	Refer to Table 130
	A NCO LSB	Refer to Table 117
	B NCO LSB	Refer to Table 119
	A NCO MSB	Refer to Table 118
	B NCO MSB	Refer to Table 120
	A CHIRP RESET TO ZERO	Refer to Table 108
	B CHIRP RESET TO ZERO	Refer to Table 116
	DDS ENA	Refer to Table 43
	A CHIRP MIN FREO LSB	Refer to Table 101
	A CHIRP MIN FREO MSB	Refer to Table 102
	A CHIRP MAX FREO LSB	Refer to Table 103
	A CHIRP MAX FREO MSB	Refer to Table 104
	A CHIRP STEP FREO LSB	Refer to Table 105
	A CHIRP STEP FREO MSB	Refer to Table 106
	B CHIRP MIN FREO LSB	Refer to Table 109
	B CHIRP MIN FREO MSB	Refer to Table 110
	B CHIRP MAX FREO LSB	Refer to Table 111

	B_CHIRP_MAX_FREQ_MSB	Refer to Table 112
	B_CHIRP_STEP_FREQ_LSB	Refer to Table 113
	B_CHIRP_STEP_FREQ_MSB	Refer to Table 114
	A_CHIRP_REPEAT	Refer to Table 107
	B_CHIRP_REPEAT	Refer to Table 115
	FH_HSSL0_ENA must be set to 0	Refer to Table 45
	A_TRIG_FH_CHIRP	Refer to Table 51
	B_TRIG_FH_CHIRP	Refer to Table 52
	TRIG_FH_CHIRP	Refer to Table 50
	TRIGGER_ENA	Refer to Table 44

11.8.7 Frequency hopping (with DUC)

The DAC integrates a frequency hopping with ultra-fast hopping rate. This feature is only possible with interpolation by 4, 8 or 16. Serial link can be used for a fast transfer of frequency parameters. ASL0 and BSL0 (Lane 0) are used for this functionality. SPI can also be used but in that case parameter change is not applied at a deterministic instant.

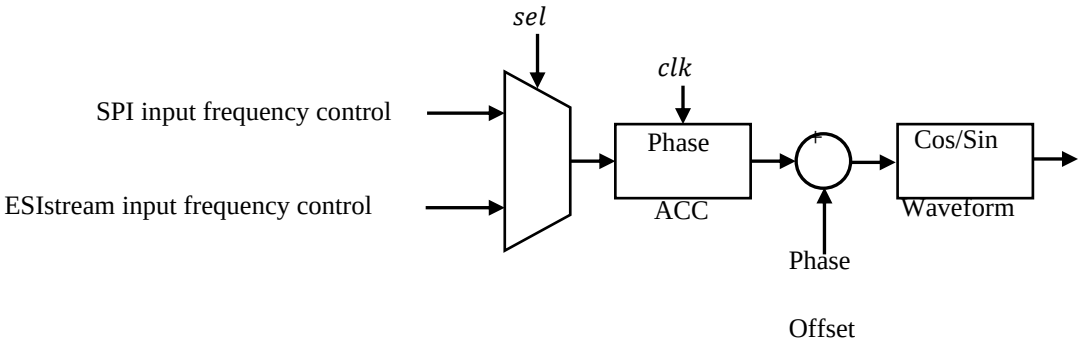


Figure 49 – Frequency Hopping Principle

11.8.7.1 Frequency Hopping Programming via ASL0 and/or BSL0

To activate the new frequency setting, two consecutive trigger frames are mandatory. Trigger can be sent at any instant. A new setting can be reprogrammed at any instant. It will be taken into account once two consecutive trigger (TRIG) frames will be sent.

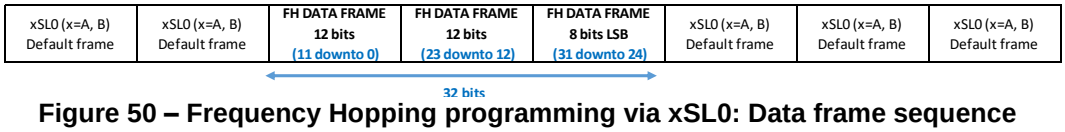


Figure 50 – Frequency Hopping programming via xSL0: Data frame sequence

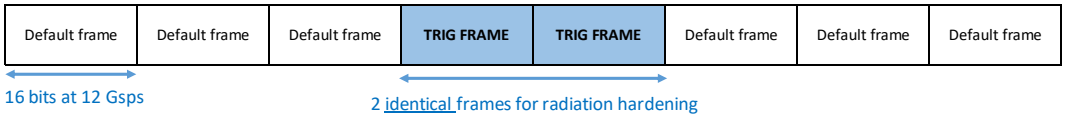


Figure 51 – Frequency Hopping programming via xSL0: TRIG sequence

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FH DATA FRAME	DC	T	Parity	1	D	D	D	D	D	D	D	D	D	D	D	D

Figure 52 – Frequency Hopping via xSL0: data frame

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFAULT FRAME	DC	T	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 53 – Frequency Hopping via xSL0: default frame

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIG FRAME	DC	T	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 54 – Frequency Hopping via xSL0: TRIG frame

FH SEQUENCE example 1	xSL0 (x=A, B) Default frame	xSL0 (x=A, B) Default frame	FH DATA FRAME 12 bits (11 downto 0)	FH DATA FRAME 12 bits (23 downto 12)	FH DATA FRAME 8 bits LSB (31 downto 24)	TRIG FRAME for FH	TRIG FRAME for FH	xSL0 (x=A, B) Default frame	xSL0 (x=A, B) Default frame	xSL0 (x=A, B) Default frame
FH SEQUENCE example 2	xSL0 (x=A, B) Default frame	xSL0 (x=A, B) Default frame	FH DATA FRAME 12 bits (11 downto 0)	FH DATA FRAME 12 bits (23 downto 12)	FH DATA FRAME 8 bits LSB (31 downto 24)	xSL0 (x=A, B) Default frame	TRIG FRAME for FH	TRIG FRAME for FH	xSL0 (x=A, B) Default frame	xSL0 (x=A, B) Default frame

x times

Figure 55 – Examples of frequency hopping programming via xSL0

11.8.7.2 Frequency Hopping programming via SPI:

The frequency setting is written in SPI registers via 2 SPI instructions (A_NCO_LSB and A_NCO_MSB for core A and B_NCO_LSB and B_NCO_MSB for core B). Triggering is issued with an SPI write (write in A_ TRIG_FH_CHIRP or B_ TRIG_FH_CHIRP register or TRIG_FH_CHIRP to trig A & B cores simultaneously).

When switching from one frequency to the following frequency, two possibilities can be selected via SPI (via registers A_FH_CLEAR_PHASE and B_FH_CLEAR_PHASE):

- resetting the phase (default configuration) or
- maintaining the current phase when switching

These 2 possibilities are described in the two below figures. In each plot there are three frequencies, we jump from first to second, to third and then back to the first frequency.
In 'phase continuous' mode, we keep the same phase in the accumulator between the different frequencies. It can be observed that when the frequency changes the first sample of the new frequency starts at the level where the previous frequency ended up.

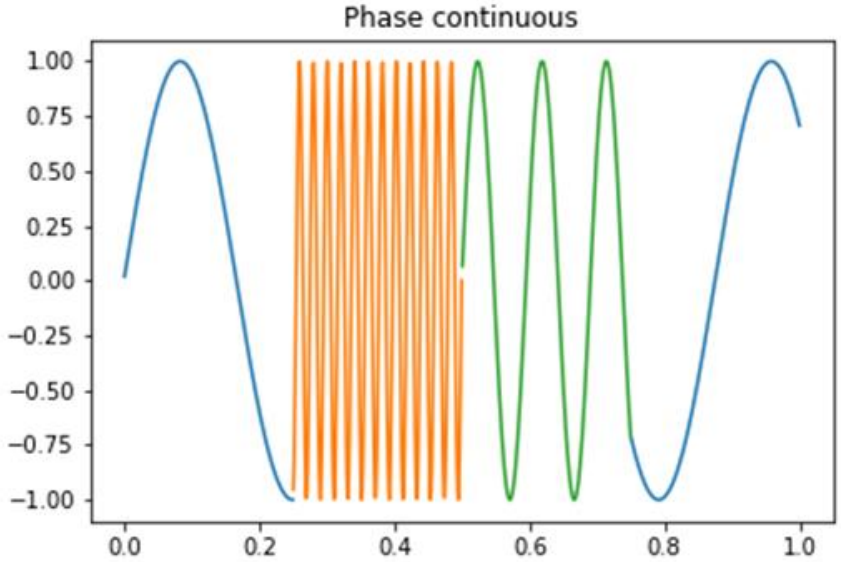


Figure 56 – Example of frequency hopping in phase continuous mode

In 'phase reset' mode, the phase is reset whenever the frequency changes.

It can be observed below that the first sample of each new frequency starts at the reset level (mid-scale).

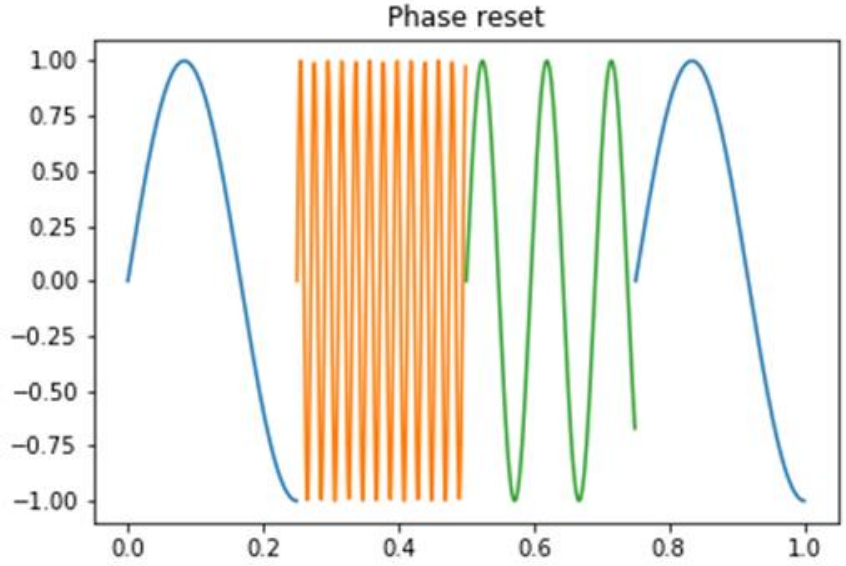


Figure 57 – Example of frequency hopping in phase reset mode

11.8.7.3 Procedure for core A with SPI

RESET (active at low level, 100 ns min)
WRITE @TRIGGER_ENA 0b -1
WRITE @A_NCO_LSB 0x ---- (NCO [15:0])
WRITE @A_NCO_MSB 0x ---- (NCO [31:16])
WRITE @A_FH_ROT_MIXER 0x ----
WRITE @A_PHASE_OFFSET_LSB 0x ----
WRITE @A_PHASE_OFFSET_MSB 0x ----
WRITE @A_FH_CLEAR_PHASE 0x ----
SYNC
WRITE @A_TRIG_FH_CHIRP (NCO above parameters are taken into account)
WAIT

WRITE @A_NCO_LSB 0x ----
WRITE @A_NCO_MSB 0x ----
WRITE @A_TRIG_FH_CHIRP
WAIT

WRITE @A_NCO_LSB 0x ----
WRITE @A_NCO_MSB 0x ----
WRITE @A_TRIG_FH_CHIRP
And so on …

11.8.7.4 Procedure for core B with SPI

RESET
WRITE @TRIGGER_ENA 0b 1-
WRITE @B_NCO_LSB 0x ---- (NCO [15:0])
WRITE @B_NCO_MSB 0x ---- (NCO [31:16])
WRITE @B_FH_ROT_MIXER 0x ----
WRITE @B_PHASE_OFFSET_LSB 0x ----
WRITE @B_PHASE_OFFSET_MSB 0x ----
WRITE @B_FH_CLEAR_PHASE 0x ----

SYNC
WRITE @B_TRIG_FH_CHIRP
WAIT


```
WRITE @B_NCO_LSB                0x ----
WRITE @B_NCO_MSB                0x ----
WRITE @B_TRIG_FH_CHIRP          0x 0000
WAIT

WRITE @B_NCO_LSB                0x ----
WRITE @B_NCO_MSB                0x ----
WRITE @B_TRIG_FH_CHIRP          0x 0000
WAIT
And so on …
```

11.8.7.5 Procedure for core A & B with SPI

```
RESET
WRITE @TRIGGER_ENA              0b 11

WRITE @A_NCO_LSB                0x ----
WRITE @A_NCO_MSB                0x ----
WRITE @A_FH_ROT_MIXER           0x ----
WRITE @A_ PHASE_OFFSET_LSB      0x ----
WRITE @A_ PHASE_OFFSET_MSB      0x ----
WRITE @A_FH_CLEAR_PHASE         0x ----

WRITE @B_NCO_LSB                0x ----
WRITE @B_NCO_MSB                0x ----
WRITE @B_FH_ROT_MIXER           0x ----
WRITE @B_PHASE_OFFSET_LSB       0x ----
WRITE @B_PHASE_OFFSET_MSB       0x ----
WRITE @B_FH_CLEAR_PHASE         0x ----

SYNC
WRITE @TRIG_FH_CHIRP            0x 0000
WAIT

WRITE @A_NCO_LSB                0x ----
WRITE @A_NCO_MSB                0x ----
WRITE @B_NCO_LSB                0x ----
WRITE @B_NCO_MSB                0x ----
WRITE @_TRIG_FH_CHIRP           0x 0000
WAIT

WRITE @B_NCO_LSB                0x ----
WRITE @B_NCO_MSB                0x ----
WRITE @B_TRIG_FH_CHIRP          0x 0000
WAIT

WRITE @A_NCO_LSB                0x ----
WRITE @A_NCO_MSB                0x ----
WRITE @A_TRIG_FH_CHIRP          0x 0000
WAIT

And so on …
```

Note: for all above procedures, @FH_HSSL0_ENA register must be set to 0 (default value)

11.8.7.6 Procedure by Serial Link

11.8.7.6.1 Procedure for core A & B with HSSL0

```
RESET
WRITE @TRIGGER_ENA              0x 0003
```


WRITE @FH_HSSL0_ENA 0x 0001
SYNC
ASL0 and BSL0: NCO value and TRIG instruction are programmed by serial link.

11.8.7.6.2 Procedure for core A with HSSL0

RESET
WRITE @TRIGGER_ENA 0x 0001
WRITE @FH_HSSL0_ENA 0x 0001
SYNC
ASL0: NCO value and TRIG instruction are programmed by serial link.

11.8.7.6.3 Procedure for core B with HSSL0

RESET
WRITE @TRIGGER_ENA 0x 0002
WRITE @FH_HSSL0_ENA 0x 0001
SYNC
BSL0: NCO value and TRIG instruction are programmed by serial link.

Note: serial link number 0 must be activated by register @A_HSSL_POWER_ON[0]=1 and/or @B_HSSL_POWER_ON[0]=1

Table 29. Summary of registers used for frequency hopping feature

Function	Associated SPI registers	Description
Frequency hopping by SPI	A_NCO_LSB	Refer to Table 117
	B_NCO_LSB	Refer to Table 119
	A_NCO_MSB	Refer to Table 118
	B_NCO_MSB	Refer to Table 120
	A_TRIG_FH_CHIRP	Refer to Table 51
	A_FH_CLEAR_PHASE	Refer to Table 121
	B_TRIG_FH_CHIRP	Refer to Table 52
	B_FH_CLEAR_PHASE	Refer to Table 125
	TRIG_FH_CHIRP	Refer to Table 50
	TRIGGER_ENA	Refer to Table 44
	FH_HSSL0_ENA	Refer to Table 45

Function	Associated SPI registers	Description
Frequency hopping by ASL0 /BSL0	A_NCO_LSB	Refer to Table 117
	B_NCO_LSB	Refer to Table 119
	A_NCO_MSB	Refer to Table 118
	B_NCO_MSB	Refer to Table 120
	TRIGGER_ENA	Refer to Table 44
	FH_HSSL0_ENA	Refer to Table 45
	A_HSSL_POWER_ON	Refer to Table 56

	B HSSL POWER ON	Refer to Table 57

11.8.8 SINC compensation

DAC response is close to SINC response, leading to gain variation over Nyquist. A 3 tap symmetrical FIR with 2 settable 8-bit FIR coefficients set by SPI or by One Time Programmable fuse (OTP) is implemented. This "anti-sinc filter" is programmable and can be used to improve the band flatness. Since the sinc transfer function depends on external components, especially in higher Nyquist Zones, it is recommended to have a coefficients set by Nyquist zone. So, the anti-sinc filter is programmable.

To keep hardware cost low the filter is a symmetric 2nd order filter. This means that the filter is not able to accurately cancel all the ripple but only the overall slope. It also does not work well for steep slopes.
The equation of the filter is: y[n] = *b*.x[n] + *a*.x[n-1] + *b*.x[n-2], coefficients *a* and *b* are set using the SPI registers.

a corresponds to Coefficient 1 for channel A (A_ASINC_COEFF_1), respectively channel B (B_ASINC_COEFF_1);
b corresponds to Coefficient 2 for channel A (A_ASINC_COEFF_2), resp. channel B (B_ASINC_COEFF_2);
x_ASINC_COEFF_1 has 9 bits of which 7 are fractional;
x_ASINC_COEFF_2 has 8 bits of which 7 are fractional.
(see Table 81, Table 82, Table 83, Table 84 for details on x_ASINC_COEFF SPI resgisters)

Below is the remaining error after anti-sinc compensation applied to theoretical DAC transfer function for different output modes depending on Nyquist Zone.

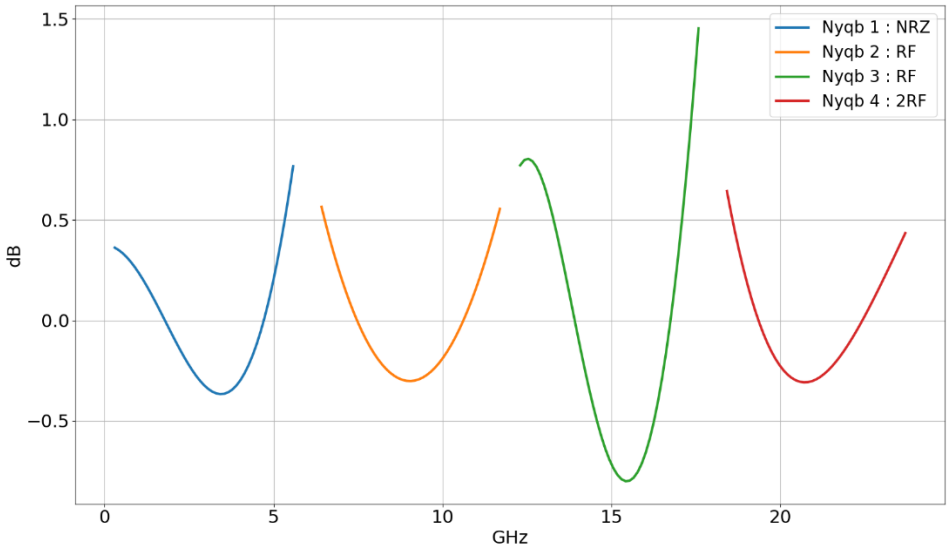


Figure 58 - Remaining error after anti-sinc compensation (Fs = 12 GSps)

The Anti-sinc filter is preceded by a gain block. The gain is used for both beam-forming / beam-hopping (see section 11.8.5) and gain calibration.
The Anti_sinc gain (10 bit) is set by SPI.

- If beam-forming/beam-hopping is not used, gain is set by registers A_ASINC_GAIN and B_ASINC_GAIN.
  The total gain for core A is $G = 1 - \text{A\_ASINC\_GAIN}.\,2^{-12}$
  The total gain for core B is $G = 1 - \text{B\_ASINC\_GAIN}.\,2^{-12}$

- If beam-forming/beam-hopping is used, gain is set by registers A_BH_GAIN_ZONEx (x=1,2,3 and 4) and B_BH_GAIN_ZONEx (x=1,2,3 and 4)

The total gain for core A is $G = 1 - \text{A\_BH\_GAIN\_ZONEx}.\,2^{-12}$
The total gain for core B is $G = 1 - \text{B\_BH\_GAIN\_ZONEx}.\,2^{-12}$
With x=1, 2, 3 and 4

It means that it is only possible to attenuate the signal. To get a gain value higher than 1, there are two possibilities:

Use the gain adjustment feature described in section 11.1.
If Gain adjustment of section 11.1 is not sufficient, the PLUS10_PERCENT_DAC_CORE bit can be used: this bit increases the DAC gain by 10 percent.
Gain expression is (in case we enabled the beam-forming/beam-hopping) :

$$G = (1 + \mathbf{PLUS10\_PERCENT\_DAC\_CORE}) \mathbf{x} (1 - \mathbf{A\_BH\_GAIN\_ZONE} \mathbf{x} . 2^{-12})$$

We can notice that setting BH_GAIN_ZONE and/or ASINC_GAIN at mid-point (511 value) gives a gain adjustment range of ±12.5%.

11.8.9 Digital and HSSLs power down

In order to minimize leakage in power down, it is recommended to ground appropriated digital and I/Os power supplies DUC and interpolation is not used. Each DAC core has its own I/Os and digital power supply in order to allow single DAC core operation.

Procedure for interpolation by 4 (8 serial links on the A and B side)
The following SPI instructions must be added before the SYNC signal:

WRITE @INTERPOL_MODE 0x 0005
WRITE @A_HSSL_POWER_ON 0x 01FE
WRITE @B_HSSL_POWER_ON 0x 01FE

- ⇨ ASL0, ASL9, ASL10, ASL11, ASL12, ASL13, ASL14, ASL15 are powered OFF
- ⇨ BSL0, BSL9, BSL10, BSL11, BSL12, BSL13, BSL14, BSL15 are powered OFF

Procedure for interpolation by 8 (4 serial links on the A and B side)
The following SPI instructions must be added before the SYNC signal:

WRITE @INTERPOL_MODE 0x 000A
WRITE @A_HSSL_POWER_ON 0x 001E
WRITE @B_HSSL_POWER_ON 0x 001E

- ⇨ ASL1, ASL2, ASL3, ASL4, are powered ON, all others serial links are powered OFF
- ⇨ BSL1, BSL2, BSL3, BSL4, are powered ON, all others serial links are powered OFF

Procedure for interpolation by 16 (2 serial links on the A and B side)
The following SPI instructions must be added before the SYNC signal:

WRITE @INTERPOL_MODE 0x 000F
WRITE @A_HSSL_POWER_ON 0x 0006
WRITE @B_HSSL_POWER_ON 0x 0006

- ⇨ ASL1, ASL2 are powered ON, all others serial links are powered OFF
- ⇨ BSL1, BSL2 are powered ON, all others serial links are powered OFF

Procedure for no interpolation (16 serial links on the A and B side)
The following SPI instructions must be added before the SYNC signal:

WRITE @INTERPOL_MODE 0x 0000
WRITE @A_HSSL_POWER_ON 0x FFFF
WRITE @B_HSSL_POWER_ON 0x FFFF

- ⇨ 32 serial links are powered ON.

Note: it is possible to use different interpolation modes between core A and B.

Function	Associated SPI registers	Description
Interpolation	INTERPOL_MODE	Refer to Table 39
	A_HSSL_POWER_ON	Refer to Table 56

	B_HSSL_POWER_ON	Refer to Table 57

11.8.10 Test mode

Several modes on the DAC output are offered to help validate the interface with the DAC.

11.8.10.1 Ramp test mode

In ramp test mode, the pattern on the DAC is a 12 bit ramp on each channel. The ramp value is reset to 0x000 when a pulse is sent on the SYNC input. User can additionally get a tunable sawtooth pattern by muxing out the phase accumulator value from the NCO to the output.

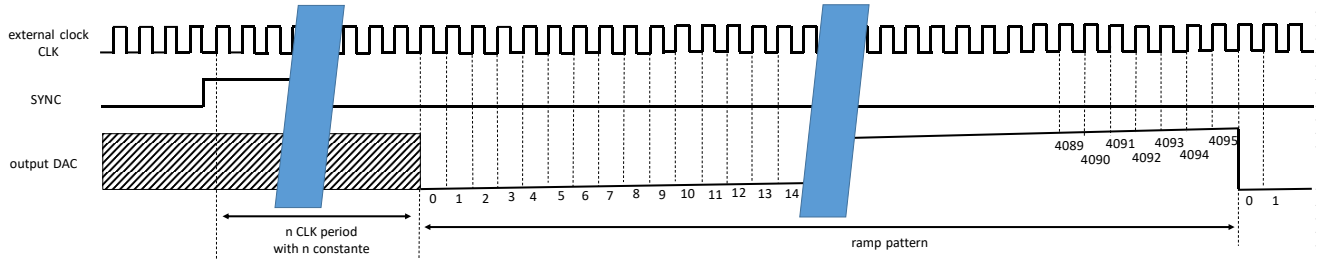


Figure 59: Ramp test mode timing diagram

11.8.10.2 Flash test mode

The flash mode is a repeating pattern in a loop. It can be useful to align different DACs. The flash pattern consists of one data at maximum value followed by 15 data at minimum value.

See below the timing diagram for the DAC output when in flash mode.

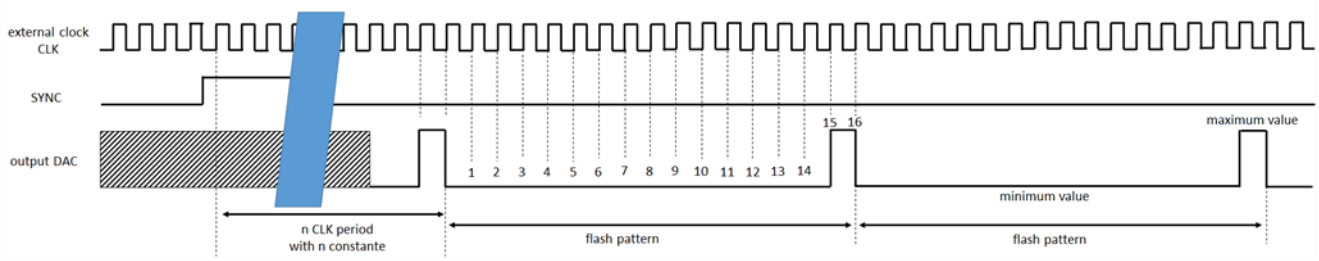


Figure 60: Flash test mode timing diagram

Note: it is possible to double the size of the maximum value by using the bit FLASH_PATTERN_CFG of the TEST_MODE_CFG register , flash pattern becomes two data at maximum value followed by 14 data at minimum value.

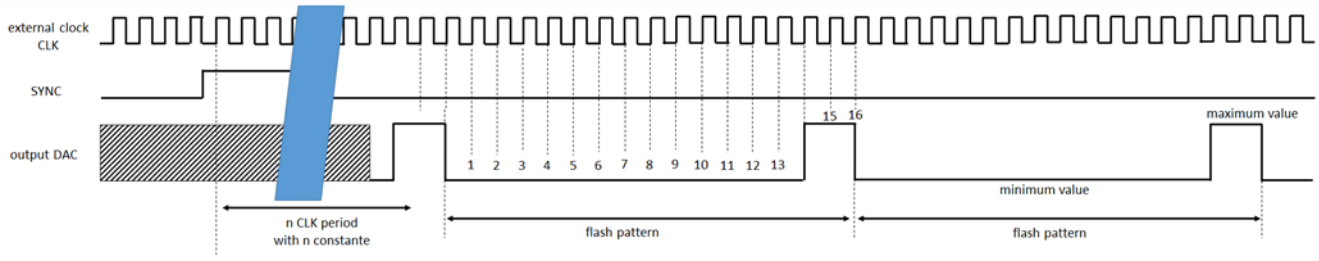


Figure 61: Flash test mode timing diagram (double size maximum value)

11.8.10.3 Constante value mode

The DAC output is fixed to a constant. This constant is programmed by SPI.

12. DETAILED DESCRIPTION OF REGISTERS

12.1 Start-up Sequence

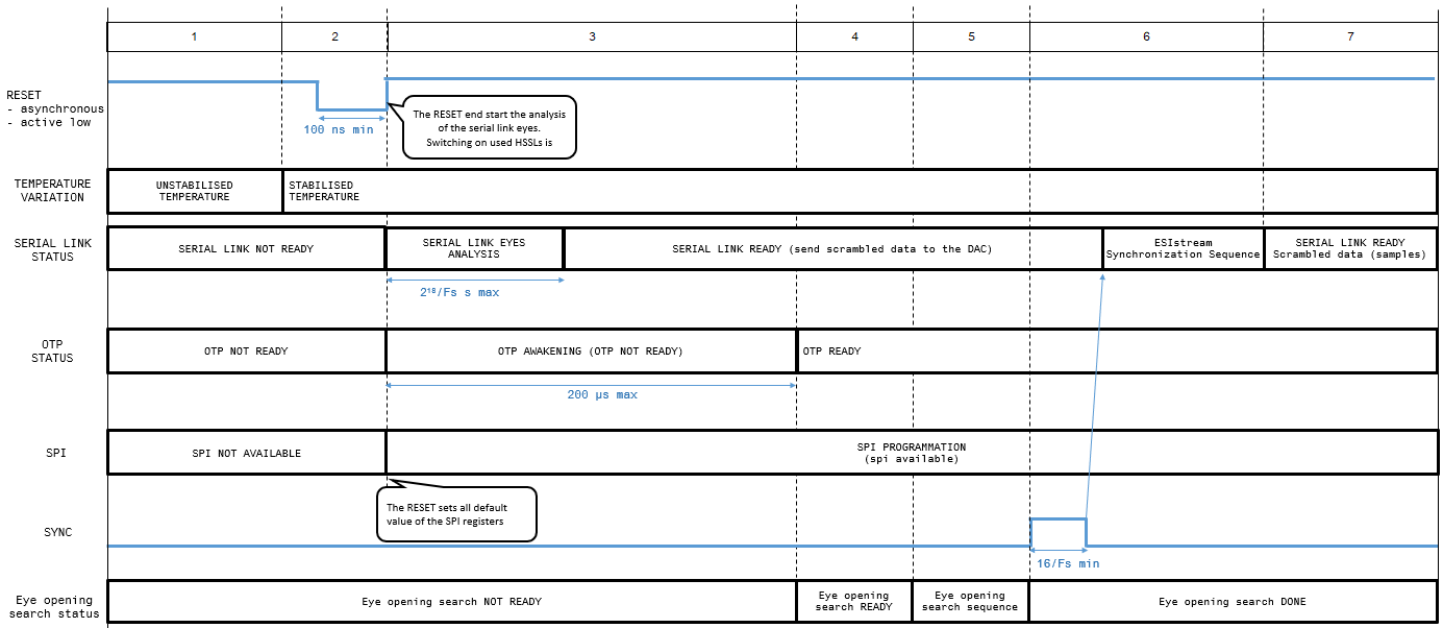


Figure 62: Start-up sequence

Notes:

1. The external clock CLK must be provided before the RSTN pulse. The external clock CLK can start before or after the power-up.
2. After the temperature stabilization the reset can be sent. The reset is an asynchronous active low signal on RSTN pin. The reset sets all SPI registers to their default value.
3. The reset starts the OTPs wake up (after the wake up, the factory configuration is ready). The wake-up status is accessible by SPI: refer to Table 34.
4. At this point, the DAC is ready to receive the SPI “OTP LOAD” instruction (optional). After receiving the SPI “OTP LOAD” instruction, the OTPS are loaded into SPI registers. There must be at least 200 µs between the RSTN pulse rising edge and this SPI “OTP LOAD ”instruction; refer to Table 33.
5. The eye-opening search sequence must be sent
    i. After the OTPs wake up.
    ii. When the FPGA transceivers PLLs are locked.
    When using the SSO as FPGA transceivers clock reference, the SSO must be enabled using the DAC register 0x0006 bit 3. By default, the SSO is disabled.
    iii. When the FPGA is sending scrambled data to the DAC.

    DIG_IN[0:3] and DIG_MODE[0:1] pins must be connected to the FPGA.
    DIG_MODE[0:1] must be set to “00” before releasing DAC reset.

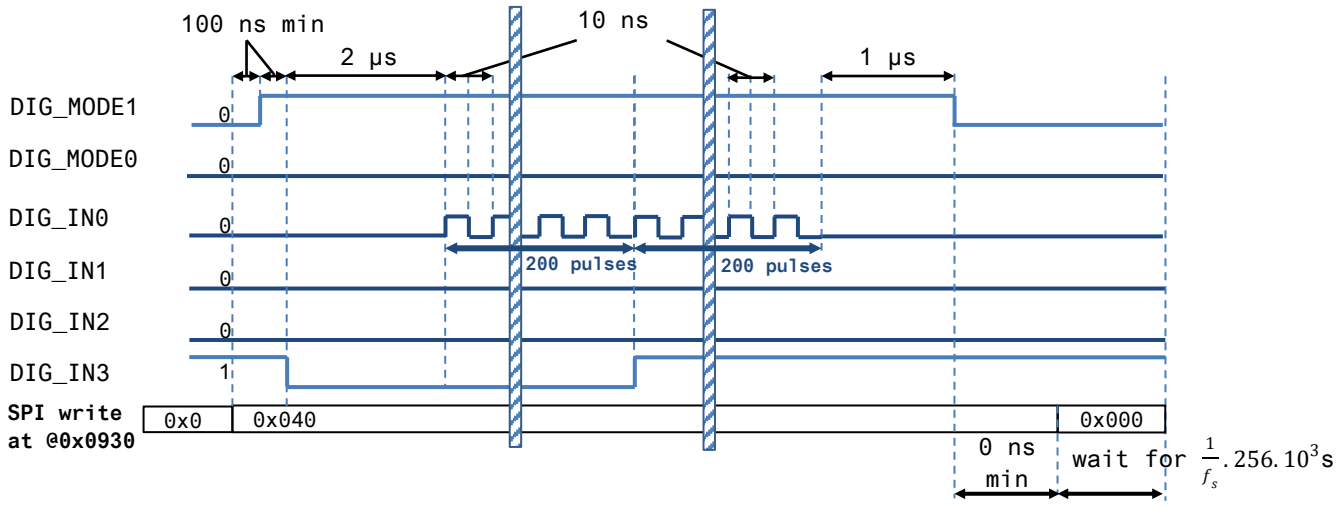


Figure 63: Eye-opening search sequence

6. The SYNC signal must be sent after the OTPs wake up. A pulse at high level (SYNC signal) is applied onto the SYNC input.

As long as the SYNC signal is high, it resets the internal clocks of the DAC. With the exception of the internal clocks used by serial link receivers and ESIstream decoders.
ESIstream decoders are ready to receive the ESIstream Synchronization Sequence (ESS) after receiving the SYNC pulse.. On the other end of the serial link, the ESIstream encoder (transmitter) must start to send the ESS after the falling edge of the SYNC pulse sent to the DAC.

7. The EXTRA_SEE_PROTECT register is optional, this register must not be activated before the SYNC signal. If EXTRA_SEE_PROTECT is activated after the SYNC, the input SYNC is disable and an unwanted SYNC signal will have no effect.

During SERIAL LINK READY and SERIAL LINK NOT

HSSLs that are used in the application should not be stucked at 0 or 1 level, a switching on the wire of HSSL at the operating frequency (12 Gbps maximum) is needed. The switching can be a simple toggle. HSSLs that are not used in the application remain not connected.

Default value for digital pin : CSN=1 , RSTN=1 , SCLK=0, MOSI=0

12.2 Register summary

Table 30. Register Summary

Address	Type	Default Value (Hex)	Register name	Short description	Section
0x0001	R	-	CHIP_ID	Chip identification	Refer to Table 31
0x0002	R	-	SERIAL_NUMBER	Part serialization	Refer to Table 32
0x0003	W	-	OTP_LOADING	Load factory configuration	Refer to Table 33
0x0004	R	-	OTP_STATUS	Check if factory configuration was successfully loaded	Refer to Table 34
0x0005	RW	0	EXTRA_SEE_PROTECT	optional	Refer to Table 35
0x0006	RW	0	SSO_CFG	SSO Clock configuration	Refer to Table 36

Address	Type	Default Value (Hex)	Register name	Short description	Section
0x0007	RW	0	CLKOUT_CFG	CLK output configuration	Refer to Table 37
0x0008	RW	0	SYNCOUT_CFG	SYNC output configuration	Refer to Table 38
0x0009	RW	0	INTERPOL_MODE	Interpolation by 4/8/16 selection	Refer to Table 39
0x000B	RW	7	ESISTREAM_CFG	Configuration of ESIstream frame	Refer to Table 40
0x000C	RW	0	TEST_MODE_CFG	Ramp, flash, constant output value	Refer to Table 41
0x000D	RW	0	BEAM_ENA	Beam-Forming and Beam-Hopping enable	Refer to Table 42
0x000E	RW	0	DDS_ENA	Sinewave, Ramp or chirp generator	Refer to Table 43
0x000F	RW	0	TRIGGER_ENA	Trigger	Refer to Table 44
0x0010	RW	0	FH_HSSL0_ENA	NCO programmation by HSSL0	Refer to Table 45
0x0011	RW	0	OUTPUT_CFG	NRZ, RF, 2RF mode	Refer to Table 46
0x0012	RW	0	ASINC_ENA	Anti-sinc compensation enable	Refer to Table 47
0x0014	RW	1	DUAL_CORE_ENA	Link of Core A & B	Refer to Table 48
0x0015	RW	0	DATA_SIGNED_ENA	Signed or unsigned ESIstream format	Refer to Table 49
0x0017	W	-	TRIG_FH_CHIRP	Trigger	Refer to Table 50
0x0018	W	-	A_TRIG_FH_CHIRP	Trigger	Refer to Table 51
0x0019	W	-	B_TRIG_FH_CHIRP	Trigger	Refer to Table 52
0x001A	W	-	TRIG_BH	Trigger	Refer to Table 53
0x001B	W	-	A_TRIG_BH	Trigger	Refer to Table 54
0x001C	W	-	B_TRIG_BH	Trigger	Refer to Table 55
0x0020	RW	FFFF	A_HSSL_POWER_ON	Core A Serial link power ON	Refer to Table 56
0x0021	RW	FFFF	B_HSSL_POWER_ON	Core B Serial link power ON	Refer to Table 57
0x0022	RW	0	FLAG_OUTPUT_CFG	Selection of different output flags on DIG_OUTx (parity, HSSL status, …) pins	Refer to 0
0x0023	RW	1	POWER_ISOLATION	Power isolation of data path from Core A to Core B when Core A is powered OFF	Refer to Table 59
0x0025	RW	0	DUC_LOAD_NCO	Load NCO	Refer to Table 60

Address	Type	Default Value (Hex)	Register name	Short description	Section
0x0100	R	-	A_HSSL_STATUS_EYE_DRIFT_1	Serial link status	Refer to Table 61
0x0101	R	-	A_HSSL_STATUS_EYE_DRIFT_2	Serial link status	Refer to Table 62
0x0102	R	-	A_HSSL_STATUS_EYE_OPENING_1	Serial link status	Refer to 0
0x0103	R	-	A_HSSL_STATUS_EYE_OPENING_2	Serial link status	Refer to Table 64
0x0104	R	-	A_HSSL_STATUS_EYE_OPENING_3	Serial link status	Refer to Table 65
0x0105	R	-	A_HSSL_STATUS_EYE_OPENING_4	Serial link status	Refer to 0
0x0106	R	-	B_HSSL_STATUS_EYE_DRIFT_1	Serial link status	Refer to Table 67
0x0107	R	-	B_HSSL_STATUS_EYE_DRIFT_2	Serial link status	Refer to Table 68
0x0108	R	-	B_HSSL_STATUS_EYE_OPENING_1	Serial link status	Refer to Table 69
0x0109	R	-	B_HSSL_STATUS_EYE_OPENING_2	Serial link status	Refer to 0
0x010A	R	-	B_HSSL_STATUS_EYE_OPENING_3	Serial link status	Refer to Table 71
0x010B	R	-	B_HSSL_STATUS_EYE_OPENING_4	Serial link status	Refer to Table 72
0x0201	RW	0	A_ASINC_GAIN	Anti-Sinc compensation	Refer to Table 73
0x0202	RW	0	A_GAIN_CAL	Gain adjustment	Refer to Table 75
0x0203	R	-	A_ASINC_OVERFLOW	Anti-Sinc filter overflow	Refer to Table 77
0x0204	W	-	A_ASINC_OVERFLOW_CLEAR	Anti-Sinc filter overflow	Refer to 0
0x0205	RW	0080	A_ASINC_COEFF_1	Anti-sinc coefficient	Refer to Table 81
0x0206	RW	0	A_ASINC_COEFF_2	Anti-sinc coefficient	Refer to Table 82
0x0210	R	-	A_DUC_OVERFLOW	Digital Up Converter overflow	Refer to Table 85
0x0211	W	-	A_DUC_INTERPOL1_OVER_CLEAR	Overflow clear	Refer to Table 87
0x0213	W	-	A_DUC_INTERPOL2_OVER_CLEAR	Overflow clear	Refer to Table 89
0x0215	W	-	A_DUC_INTERPOL3_OVER_CLEAR	Overflow clear	Refer to Table 91
0x0217	W	-	A_DUC_INTERPOL4_OVER_CLEAR	Overflow clear	Refer to Table 93
0x0219	W	-	A_DUC_MIXER_OVER_CLEAR	Overflow clear	Refer to Table 95
0x021B	W	-	A_DUC_FDELAY_OVER_CLEAR	Overflow clear	Refer to Table 97
0x0220	RW	0	A_DUC_IIR_ROUNDING_ENA	Improve NCO rounding noise	Refer to Table 99
0x0230	RW	0	A_CHIRP_MIN_FREQ_LSB	DDS chirp mode	Refer to Table 101
0x0231	RW	0	A_CHIRP_MIN_FREQ_MSB	DDS chirp mode	Refer to Table 102
0x0232	RW	0	A_CHIRP_MAX_FREQ_LSB	DDS chirp mode	Refer to Table 103
0x0233	RW	0	A_CHIRP_MAX_FREQ_MSB	DDS chirp mode	Refer to Table 104
0x0234	RW	0	A_CHIRP_STEP_FREQ_LSB	DDS chirp mode	Refer to Table 105
0x0235	RW	0	A_CHIRP_STEP_FREQ_MSB	DDS chirp mode	Refer to Table 106

Address	Type	Default Value (Hex)	Register name	Short description	Section
0x0237	RW	1	A_CHIRP_REPEAT	DDS chirp mode	Refer to Table 107
0x0238	RW	1	A_CHIRP_RESET_TO_ZERO	DDS chirp mode	Refer to Table 108
0x0241	RW	0	A_NCO_LSB	NCO	Refer to Table 117
0x0242	RW	0	A_NCO_MSB	NCO	Refer to Table 118
0x0243	RW	1	A_FH_CLEAR_PHASE	FREQUENCY HOPPING	Refer to Table 121
0x0244	RW	0	A_FH_ROT_MIXER	FREQUENCY HOPPING	Refer to Table 122
0x0245	RW	0	A_PHASE_OFFSET_LSB	FREQUENCY HOPPING	Refer to Table 123
0x0246	RW	0	A_PHASE_OFFSET_MSB	FREQUENCY HOPPING	Refer to Table 124
0x0250	RW	0	A_DDS_AMPLITUDE	DDS chirp mode	Refer to Table 129
0x0260	RW	1	A_BH_CLEAR_PHASE	BEAM FORMING	Refer to Table 131
0x0261	RW	0	A_BH_GAIN_ZONE1	BEAM FORMING	Refer to Table 132
0x0262	RW	8	A_BH_DELAY_COARSE_ZONE1	BEAM FORMING	Refer to Table 133
0x0263	RW	0	A_BH_DELAY_FINE_ZONE1	BEAM FORMING	Refer to Table 134
0x0264	RW	0	A_BH_GAIN_ZONE2	BEAM HOPPING	Refer to Table 135
0x0265	RW	8	A_BH_DELAY_COARSE_ZONE2	BEAM HOPPING	Refer to Table 136
0x0266	RW	0	A_BH_DELAY_FINE_ZONE2	BEAM HOPPING	Refer to Table 137
0x0267	RW	0	A_BH_GAIN_ZONE3	BEAM HOPPING	Refer to Table 138
0x0268	RW	8	A_BH_DELAY_COARSE_ZONE3	BEAM HOPPING	Refer to Table 139
0x0269	RW	0	A_BH_DELAY_FINE_ZONE3	BEAM HOPPING	Refer to Table 140
0x026A	RW	0	A_BH_GAIN_ZONE4	BEAM HOPPING	Refer to Table 141
0x026B	RW	8	A_BH_DELAY_COARSE_ZONE4	BEAM HOPPING	Refer to Table 142
0x026C	RW	0	A_BH_DELAY_FINE_ZONE4	BEAM HOPPING	Refer to Table 143
0x0270	RW	78	A_LOOP_CFG	Internal Manual Loop Delay timing adjustment	Refer to Table 162
0x0280	RW	0AFF	A_HSSL_POL	HSSL polarity on Core A	Refer to Table 157
0x0301	RW	0	B_ASINC_GAIN	Anti-Sinc compensation	Refer to 0
0x0302	RW	0	B_GAIN_CAL	Gain adjustment	Refer to Table 76
0x0303	R	-	B_ASINC_OVERFLOW	Anti-Sinc filter overflow	Refer to Table 78
0x0304	W	-	B_ASINC_OVERFLOW_CLEAR	Anti-Sinc filter overflow	Refer to Table 80
0x0305	RW	0080	B_ASINC_COEFF_1	Anti-sinc coefficient	Refer to Table 83
0x0306	RW	0	B_ASINC_COEFF_2	Anti-sinc coefficient	Refer to Table 84
0x0310	R	-	B_DUC_OVERFLOW	Digital Up Converter overflow	Refer to Table 86
0x0311	W	-	B_DUC_INTERPOL1_OVER_CLEAR	Overflow clear	Refer to Table 88

Address	Type	Default Value (Hex)	Register name	Short description	Section
0x0313	W	-	B_DUC_INTERPOL2_OVER_CLEAR	Overflow clear	Refer to Table 90
0x0315	W	-	B_DUC_INTERPOL3_OVER_CLEAR	Overflow clear	Refer to Table 92
0x0317	W	-	B_DUC_INTERPOL4_OVER_CLEAR	Overflow clear	Refer to Table 94
0x0319	W	-	B_DUC_MIXER_OVER_CLEAR	Overflow clear	Refer to 0
0x031B	W	-	B_DUC_FDELAY_OVER_CLEAR	Overflow clear	Refer to Table 98
0x0320	RW	0	B_DUC_IIR_ROUNDING_ENA	DDS chirp mode	Refer to Table 100
0x0330	RW	0	B_CHIRP_MIN_FREQ_LSB	DDS chirp mode	Refer to Table 109
0x0331	RW	0	B_CHIRP_MIN_FREQ_MSB	DDS chirp mode	Refer to Table 110
0x0332	RW	0	B_CHIRP_MAX_FREQ_LSB	DDS chirp mode	Refer to Table 111
0x0333	RW	0	B_CHIRP_MAX_FREQ_MSB	DDS chirp mode	Refer to Table 112
0x0334	RW	0	B_CHIRP_STEP_FREQ_LSB	DDS chirp mode	Refer to Table 113
0x0335	RW	0	B_CHIRP_STEP_FREQ_MSB	DDS chirp mode	Refer to Table 114
0x0337	RW	1	B_CHIRP_REPEAT	DDS chirp mode	Refer to Table 115
0x0338	RW	1	B_CHIRP_RESET_TO_ZERO	DDS chirp mode	Refer to Table 116
0x0341	RW	0	B_NCO_LSB	NCO	Refer to Table 119
0x0342	RW	0	B_NCO_MSB	NCO	Refer to Table 120
0x0343	RW	1	B_FH_CLEAR_PHASE	FREQUENCY HOPPING	Refer to Table 125
0x0344	RW	0	B_FH_ROT_MIXER	FREQUENCY HOPPING	Refer to Table 126
0x0345	RW	0	B_PHASE_OFFSET_LSB	FREQUENCY HOPPING	Refer to Table 127
0x0346	RW	0	B_PHASE_OFFSET_MSB	FREQUENCY HOPPING	Refer to Table 128
0x0350	RW	0	B_DDS_AMPLITUDE	DDS chirp mode	Refer to Table 130
0x0360	RW	1	B_BH_CLEAR_PHASE	BEAM FORMING	Refer to Table 144
0x0361	RW	0	B_BH_GAIN_ZONE1	BEAM FORMING	Refer to Table 145
0x0362	RW	8	B_BH_DELAY_COARSE_ZONE1	BEAM FORMING	Refer to Table 146
0x0363	RW	0	B_BH_DELAY_FINE_ZONE1	BEAM FORMING	Refer to Table 147
0x0364	RW	0	B_BH_GAIN_ZONE2	BEAM HOPPING	Refer to Table 148
0x0365	RW	8	B_BH_DELAY_COARSE_ZONE2	BEAM HOPPING	Refer to Table 149
0x0366	RW	0	B_BH_DELAY_FINE_ZONE2	BEAM HOPPING	Refer to Table 150
0x0367	RW	0	B_BH_GAIN_ZONE3	BEAM HOPPING	Refer to Table 151
0x0368	RW	8	B_BH_DELAY_COARSE_ZONE3	BEAM HOPPING	Refer to Table 152
0x0369	RW	0	B_BH_DELAY_FINE_ZONE3	BEAM HOPPING	Refer to Table 153
0x036A	RW	0	B_BH_GAIN_ZONE4	BEAM HOPPING	Refer to Table 154
0x036B	RW	8	B_BH_DELAY_COARSE_ZONE4	BEAM HOPPING	Refer to Table 155

Address	Type	Default Value (Hex)	Register name	Short description	Section
0x036C	RW	0	B_BH_DELAY_FINE_ZONE4	BEAM HOPPING	Refer to Table 156
0x0370	RW	78	B_LOOP_CFG	Internal Manual Loop Delay timing adjustment	Refer to Table 163
0x0380	RW	0AFF	B_HSSL_POL	HSSL polarity on Core B	Refer to Table 158
0x0400	RW	0	PLUS10_PERCENT_DAC_CORE	+10% on DAC Gain	Refer to Table 159
0x0402	RW	3	POWER_ON_CORE_ANA	Power on/off CORE_ANA	Refer to Table 160
0x0406	RW	3	POWER_ON_MUX21	Power on/off MUX21	Refer to Table 161
0x0407	RW	820	SDA_MUX21	MUX21 sampling delay adjustment	Refer to Table 164
0x0500	R	-	SYNC_FLAG	SYNC forbidden area detection	Refer to Table 165
0x0501	RW	0	SYNC_FLAG_RST	Reset of SYNC_FLAG	Refer to Table 166
0x0502	RW	0	SYNC_CFG	SYNC programmable shift	Refer to Table 167
0x0503	RW	0	SHIFT_BUFFER	Multi-DAC synchronization	Refer to Table 168
0x0504	RW	0	BUFFER_CFG	Multi-DAC synchronization	Refer to Table 169
0x0505	RW	4343	MAX_LATENCY_FIRST_DATA	Multi-DAC synchronization	Refer to Table 170
0x0506	R	-	LATENCY_FIRST_DATA	Multi-DAC synchronization	Refer to Table 171
0x0507	R	-	SYNC_BUFFER_OVERFLOW	Multi-DAC synchronization	Refer to Table 172
0x0603	RW	55	SERDES_ANA	To adjust gain and bandwidth according to end user board	Refer to Table 173
0x060C	R	-	PARITY_STATUS	Data parity error of HSSL links	Refer to Table 174
0x0610	R	-	A_ESISTREAM_FLASH_STATUS	ESISTREAM status	Refer to Table 175
0x0611	R	-	A_ESISTREAM_PRBS_STATUS	ESISTREAM status	Refer to Table 176
0x0612	R	-	B_ESISTREAM_FLASH_STATUS	ESISTREAM status	Refer to Table 177
0x0613	R	-	B_ESISTREAM_PRBS_STATUS	ESISTREAM status	Refer to Table 178
0x0617	RW	0	A_DDS_RAMP_MODE	Replace sinus by a ramp pattern	Refer to Table 179
0x061C	RW	0	B_DDS_RAMP_MODE	Replace sinus by a ramp pattern	Refer to Table 180
0x061E	RW	7	POWER_ON_TIMER	Power on/off TIMER	Refer to Table 181

12.3 Register details

R = Read only register
RW = Read/Write register
W = Write only register
A writing in this address causes an event. The Event is described in the register description.
The value of writing can be either 0 or 1. It is recommended to write a 0 value.
The value of reading must be ignored.

Address are in hexadecimal

Table 31. CHIP_ID @0x0001

Bit	Field	Type	Default value	Core	Description
15:0	CHIP_ID	R	N/A	N/A	Chip id

Table 32. SERIAL_NUMBER @0x0002

Bit	Field	Type	Default value	Core	Description
15:0	SERIAL_NUMBER	R	N/A	N/A	Serial number

Table 33. OTP_LOADING @0x0003

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	OTP_LOADING	W	N/A	N/A	A writing in this address causes the OTP loading

Table 34. OTP_STATUS @0x0004

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	OTP_PARITY	R	N/A	N/A	1: OTP parity ok 0: OTP parity failed
0	OTP_READY				1: OTP ready, OTP are ready 200 µs maximum after the end of reset 0: OTP not ready

Table 35. EXTRA_SEE_PROTECT @0x0005

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	EXTRA_SEE_PROTECT	RW	0	AB	1: additional SEE protection: SYNC signal has no effect (optional) 0: major protections are available (default) The presence of the SPI clock, SCLK, refreshes Triple Majority Redundancy registers.

Table 36. SSO_CFG @0x0006

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3	SSO_ENA	RW	0	AB	1: clock SSO enable 0: clock SSO disable (default)

2	SSO_FULL_SWING		0		1: full swing for SSO clock 0: reduce swing for SSO clock
1:0	SSO_RATIO		0		Ratio “frequency external clock” / “frequency SSO clock” in NRZ and RF mode 11: 4 10: 8 01: 16 00: 32 (default) Ratio “frequency external clock” / “frequency SSO clock in 2RF mode 11: 8 10: 16 01: 32 00: 64 (default)

Table 37. CLKOUT_SWING @0x0007

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	CLKOUT_ENA	RW	0	N/A	0: CLKOUT disabled (default) 1: CLKOUT enabled
0	CLKOUT _FULL_SWING		0		0: CLKOUT reduced swing (default) 1: CLKOUT full swing

Table 38. SYNCOUT_CFG @0x0008

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	SYNCO_ENA	RW	0	N/A	0: SYNCOUT disabled (default) 1: SYNCOUT enabled
0	SYNCO_FULL_SWING		0		0: SYNCOUT reduced swing (default) 1: SYNCOUT full swing

Table 39. INTERPOL_MODE @0x0009

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
3:2	B_INTERPOL_MODE	RW	0	B	For core B only: 00 no interpolation 01: interpolation by 4 10: interpolation by 8 11: interpolation by 16
1:0	A_INTERPOL_MODE		0	A	For core A only: 00: no interpolation 01: interpolation by 4 10: interpolation by 8 11: interpolation by 16

Note:
For interpolation by 4, 8 serial links are used per core
For interpolation by 8, 4 serial links are used per core
For interpolation by 16, 2 serial links are used per core
For interpolation by 4 or by 8 or by 16, the serial link number 0 is activated or not with the register @FH_HSSL0_ENA Serial link number 0 is disabled by default
Without interpolation, 16 serial links are used per core

Table 40. ESISTREAM_CFG @0x000B

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
3	ESI_PARITY_ENA	RW	0	AB	1: Parity enable (*) 0: Parity disable (default value)
2	ESI_PRBS_ENA		1		1: PRBS enable (default value) 0: PRBS disable
1	ESI_DC_ENA		1		1: DC balance enable (default value) 0: DC balance disable
0	ESI_LSB_FIRST		1		The first bit transmitted of the ESISTREAM frame: 1: LSB first (default value) 0: MSB first

Note (*): The parity bit is on the 13th position in the ESIstream frame (CB2 bit)
Refer to section Serial link protocol for bit parity position

Table 41. TEST_MODE_CFG @0x000C

Bit	Field	Type	Default value	Core	Description
15:4	TEST_MODE_CST_VALUE	RW	0	AB	Constant value
3	FLASH_PATTERN_CFG		0		Flash Pattern Configuration, the following pattern is repeated in a loop at DAC output 1: 14 minimum samples + 2 maximum samples 0: 15 minimum samples + 1 maximum sample (default)
2:0	TEST_MODE		0		111: constant value 110: flash pattern 101: ramp mode 100: 128 multi tones pattern 000: test mode disable (default value)

Table 42. BEAM_ENA @0x000D

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2:0	BEAM_ENA	RW	0	AB	111: BeamHopping enable with 4 zones 110: BeamHopping enable with 3 zones 101: BeamHopping enable with 2 zones 100: BeamForming enable (with 1 zone) 000: BeamForming disable (default value)

Table 43. DDS_ENA @0x000E

Bit	Field	Type	Default value	Core	Description
15:6					Reserved
5	B_CHIRP_RUN	RW	0	B	CHIRP run on core B 1: CHIRP run enable 0: CHIRP run disable (default value)
4	B_CHIRP_ENA		0		CHIRP enable on core B 1: CHIRP enable 0: CHIRP disable (default value)
3	B_DDS_ENA		0		Direct Digital Synthesizer enable (sinus generator) on core B 1: DDS enable 0: DDS disable (default value)
2	A_CHIRP_RUN		0	A	CHIRP run on core A 1: CHIRP run enable 0: CHIRP run disable (default value)

1	A_CHIRP_ENA		0		CHIRP enable on core A 1: CHIRP enable 0: CHIRP disable (default value)
0	A_DDS_ENA		0		Direct Digital Synthesizer enable (sinus generator) on core A 1: DDS enable 0: DDS disable (default value)

Table 44. TRIGGER_ENA @0x000F

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	B_TRIG_FH_DDS	RW	0	B	The TRIGGER is enabled for Frequency Hopping or DDS mode (core B)
0	A_TRIG_FH_DDS			A	The TRIGGER is enable for Frequency Hopping or DDS mode (core A)

Table 45. FH_HSSL0_ENA @0x0010

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	FH_HSSL0_ENA	RW	0	AB	Serial link number 0 enable for Frequency Hopping 1: NCO programming by serial link number 0 0: NCO programming by SPI (default)

Table 46. OUTPUT_CFG @0x0011

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2	2RF_ENA	RW	0	AB	2RF mode 1: 2RF for core A and B, bit[1:0] are no more taken into account. 0: 2RF disable bit[1:0] are taken into account (default)
1	B_NRZ_RF_ENA		0	B	NRZ mode enable or RF mode enable (core B). 1: RF 0: NRZ (default)
0	A_NRZ_RF_ENA		0	A	NRZ mode enable or RF mode enable (core A). 1: RF 0: NRZ (default)

Example:
1xx: 2RF mode for core A and B (external clock = 24 GHz maximum)
011: RF mode for core A and B
010: NRZ mode core A and RF mode for core B
001: RF mode core A and NRZ mode for core B
000: NRZ mode for core A and B

Table 47. ASINC_ENA @0x0012

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	B_ASINC_ENA	RW	0	B	Anti-Sinc Enable (core B) 1: Anti Sinc function enable 0: Anti Sinc function disable (default)
0	A_ASINC_ENA		0	A	Anti-Sinc Enable (core A) 1: Anti Sinc function enable

					0: Anti Sinc function disable (default)

Table 48. DUAL_CORE_ENA @0x0014

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	DUAL_CORE_ENA	RW	1	AB	1: The first data of ESIstream protocol core A and core B will be available at the output of the DAC at the same time. (default value) 0: The first data of ESIstream protocol can start at any time for core A or B. In other words the 16 HSSLs core A and the 16 HSSLs core B are independents.

Note:
If @DUAL_CORE_ENA = 1, it is mandatory to start the 32 HSSLs (or ESIstream protocol) in the same timing window.
For a serial link data rate of 12 Gbps:
If the 32 HSSLs are all the same length, the timing window is 3.3 ns
If the 32 HSSLs have 10 cm difference between the shortest and the longest wire, the timing window is 2.7 ns

If @DUAL_CORE_ENA = 0, it is mandatory to start the 16 HSSLs core A (or ESIstream protocol) in the same timing window and the 16 HSSLs core B in another timing window.
For a serial link data rate of 12 Gbps:
If the 16 HSSLs core A are all the same length, the timing window core A is 3.3 ns
If the 16 HSSLs core B are all the same length, the timing window core B is 3.3 ns
If the 16 HSSLs core A have 10 cm difference between the shortest and the longest wire, the timing window core A is 2.7 ns
If the 16 HSSLs core A have 10 cm difference between the shortest and the longest wire, the timing window core B is 2.7 ns

Table 49. DATA_SIGNED_ENA @0x0015

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	B_DATA_SIGNED_ENA	RW	0	B	The data used in the ESIstream frame is in format (core B): 1: signed 0: unsigned (default)
0	A_DATA_SIGNED_ENA		0	A	The data used in the ESIstream frame is in format (core A): 1: signed 0: unsigned (default)

The DATA_SIGNED_ENA register is available only for mode with no interpolation (INTERPOL_MODE=0). With interpolation by 4, DATA_SIGNED_ENA register has no effect.

Table 50. TRIG_FH_CHIRP @0x0017

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	TRIG_FH_CHIRP	W	N/A	AB	Trigger for Frequency Hopping or DDS/CHIRP mode for core A and B. A writing in this address causes a TRIGGER.

Table 51. A_TRIG_FH_CHIRP @0x0018

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_TRIG_FH_CHIRP	W	N/A	A	Trigger for Frequency Hopping or DDS/CHIRP and for core A only. A writing in this address causes a TRIGGER.

Table 52. B_TRIG_FH_CHIRP @0x0019

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_TRIG_FH_CHIRP	W	N/A	B	Trigger for Frequency Hopping or DDS/CHIRP and for core B only. A writing in this address causes a TRIGGER.

Table 53. TRIG_BH @0x001A

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	TRIG_BH	W	N/A	AB	Trigger for Beam Hopping/forming mode for core A and B A writing in this address causes a TRIGGER.

Table 54. A_TRIG_BH @0x001B

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_TRIG_BH	W	N/A	A	Trigger for Beam Hopping/forming mode for core A only A writing in this address causes a TRIGGER.

Table 55. B_TRIG_BH @0x001C

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_TRIG_BH	W	N/A	B	Trigger for Beam Hopping/forming mode for core B only A writing in this address causes a TRIGGER.

Table 56. A_HSSL_POWER_ON @0x0020

Bit	Field	Type	Default value	Core	Description
15:0	A_HSSL_POWER_ON	RW	0x FFFF	A	Bit[15] = power ON serial link number 15 . . Bit[2] = power ON serial link number 2 Bit[1] = power ON serial link number 1 Bit[0] = power ON serial link number 0 Bit[n]=0: serial link number n is powered OFF Bit[n]=1: serial link number n is powered ON By default all serial link are powered ON

Table 57. B_HSSL_POWER_ON @0x0021

Bit	Field	Type	Default value	Core	Description

15:0	B_HSSL_POWER_ON	RW	0x FFFF	B	Bit[15] = power ON serial link number 15 . . Bit[2] = power ON serial link number 2 Bit[1] = power ON serial link number 1 Bit[0] = power ON serial link number 0 Bit[n]=0: serial link number n is powered OFF Bit[n]=1: serial link number n is powered ON By default all serial links are powered ON

Table 58. FLAG_OUTPUT_CFG @0x0022 (R/W register for core A & core B)

<table>
<tr><th>Bit</th><th>Field</th><th>Default value</th><th>Description</th></tr>
<tr><td>15:6</td><td></td><td></td><td>Reserved</td></tr>
<tr><td>5:3</td><td>FLAG_OUT_13_CFG</td><td>0</td><td>
<table>
<tr><td></td><td>DIG_OUT1 output pin indicates a parity error of core B HSSL links (*):</td><td>DIG_OUT3 output pin indicates a parity error of core A HSSL links (*):</td></tr>
<tr><td>000</td><td>Disable</td><td>Disable</td></tr>
<tr><td>001</td><td>Low level : Parity is ok on HSSL0
High level : Parity error on HSSL0</td><td>Low level : Parity is ok on HSSL0
High level : Parity error on HSSL0</td></tr>
<tr><td>010</td><td>Low level : Parity is ok on all HSSL1 to HSSL15
High level : Parity error on any HSSL1 to HSSL15</td><td>Low level : Parity is ok on all HSSL1 to HSSL15
High level : Parity error on any HSSL1 to HSSL15</td></tr>
<tr><td>011</td><td>Low level : Parity is ok on all HSSL0 to HSSL15
High level : Parity error on any HSSL0 to HSSL15</td><td>Low level : Parity is ok on all HSSL0 to HSSL15
High level : Parity error on any HSSL0 to HSSL15</td></tr>
<tr><td>111</td><td>High Level : Overflow DUC & ASINC</td><td>High level : Overflow DUC & ASINC</td></tr>
</table>
</td></tr>
<tr><td>2:0</td><td>FLAG_OUT_02_CFG</td><td>0</td><td>
<table>
<tr><td></td><td>DIG_OUT0 output pin indicates a parity error of core B HSSL links (*):</td><td>DIG_OUT2 output pin indicates a parity error of core A HSSL links (*):</td></tr>
<tr><td>000</td><td>Disable</td><td>Disable</td></tr>
<tr><td>001</td><td>Low level : Parity is ok on HSSL0
High level : Parity error on HSSL0</td><td>Low level : Parity is ok on HSSL0
High level : Parity error on HSSL0</td></tr>
<tr><td>010</td><td>Low level : Parity is ok on all HSSL1 to HSSL15
High level : Parity error on any HSSL1 to HSSL15</td><td>Low level : Parity is ok on all HSSL1 to HSSL15
High level : Parity error on any HSSL1 to HSSL15</td></tr>
<tr><td>011</td><td>Low level : Parity is ok on all HSSL0 to HSSL15
High level : Parity error on any HSSL0 to HSSL15</td><td>Low level : Parity is ok on all HSSL0 to HSSL15
High level : Parity error on any HSSL0 to HSSL15</td></tr>
<tr><td>111</td><td>High level : Overflow DUC & ASINC</td><td>High level : Overflow DUC & ASINC</td></tr>
</table>
</td></tr>
</table>

NOTE: (*) : a sample with a wrong parity will cause a high level on the DIG_OUTx output pin during 1024*Ts ns (Ts = 1/Fs).

Table 59. POWER_ISOLATION @0x0023

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	POWER_ISOLATION	RW	1	N/A	1: core A is power ON, no power isolation is needed 0: core A is power OFF, enable the power isolation between core A and B.

Table 60. DUC_LOAD_NCO @0x0025

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2:0	DUC_LOAD_NCO	RW	0	AB	000 : NCO is not taken into account (default value) 111 : NCO is taken into account by digital Must be set to “111” after NCO parameters update and before the SYNC signal. This SPI instruction is mandatory

Procedure to load NCO parameters before SYNC signal:

RESET
WRITE @A_NCO_MSB 0x ----
WRITE @A_NCO_LSB 0x ----
WRITE @B_NCO_MSB 0x ----
WRITE @B_NCO_LSB 0x ----
WRITE @DUC_LOAD_NCO 0x 0007
SYNC

Table 61. A_HSSL_STATUS_EYE_DRIFT_1 @0x0100

Bit	Field	Type	Default value	Core	Description
15:14	A_HSSL7_STATUS_EYE_DRIFT	R	N/A	A	This is a warning when the serial link eye has drifted and reached the limit of reception. The drift can be due to a variation of temperature for example. 11: warning, eye has reached the sampling limit 10 or 10 : warning, eye is near the sampling limit 00: status OK
13:12	A_HSSL6_STATUS_EYE_DRIFT				
11:10	A_HSSL5_STATUS_EYE_DRIFT				
9:8	A_HSSL4_STATUS_EYE_DRIFT				
7:6	A_HSSL3_STATUS_EYE_DRIFT				
5:4	A_HSSL2_STATUS_EYE_DRIFT				
3:2	A_HSSL1_STATUS_EYE_DRIFT				
1:0	A_HSSL0_STATUS_EYE_DRIFT				

Table 62. A_HSSL_STATUS_EYE_DRIFT_2 @0x0101

Bit	Filed	Type	Default value	Core	Description
15:14	A_HSSL15_STATUS_EYE_DRIFT	R	N/A	A	This is a warning when the serial link eye has drifted and reached the limit of reception. The drift can be due to a variation of temperature for example. 11: warning, eye has reached the sampling limit 10 or 10: warning, eye is near the sampling limit 00: status OK
13:12	A_HSSL14_STATUS_EYE_DRIFT				
11:10	A_HSSL13_STATUS_EYE_DRIFT				
9:8	A_HSSL12_STATUS_EYE_DRIFT				
7:6	A_HSSL11_STATUS_EYE_DRIFT				
5:4	A_HSSL10_STATUS_EYE_DRIFT				
3:2	A_HSSL9_STATUS_EYE_DRIFT				
1:0	A_HSSL8_STATUS_EYE_DRIFT				

Table 63. A_HSSL_STATUS_EYE_OPENING_1 @0x0102

Bit	Field	Type	Default value	Core	Description
15					Reserved
14:12	A_HSSL4_STATUS_EYE_OPENING	R	N/A	A	This is an information about the quality of serial link eye number 0 to 4. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed
11:9	A_HSSL3_STATUS_EYE_ OPENING				
8:6	A_HSSL2_STATUS_EYE_ OPENING				
5:3	A_HSSL1_STATUS_EYE_ OPENING				
2:0	A_HSSL0_STATUS_EYE_ OPENING				

Table 64. A_HSSL_STATUS_EYE_OPENING_2 @0x0103

Bit	Field	Type	Default value	Core	Description
15					Reserved
14:12	A_HSSL9_STATUS_EYE_ OPENING	R	N/A	A	This is an information about the quality of serial link eye number 5 to 9. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed
11:9	A_HSSL8_STATUS_EYE_ OPENING				
8:6	A_HSSL7_STATUS_EYE_ OPENING				
5:3	A_HSSL6_STATUS_EYE_ OPENING				
2:0	A_HSSL5_STATUS_EYE_ OPENING				

Table 65. A_HSSL_STATUS_EYE_OPENING_3 @0x0104

Bit	Field	Type	Default value	Core	Description
15					Reserved
14:12	A_HSSL14_STATUS_EYE_ OPENING	R	N/A	A	This is an information about the quality of serial link eye number 10 to 14. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed
11:9	A_HSSL13_STATUS_EYE_ OPENING				
8:6	A_HSSL12_STATUS_EYE_ OPENING				
5:3	A_HSSL11_STATUS_EYE_ OPENING				
2:0	A_HSSL10_STATUS_EYE_ OPENING				

Table 66. A_HSSL_STATUS_EYE_OPENING_4 @0x0105

Bit	Field	Type	Default value	Core	Description
15:3					Reserved

2:0	A_HSSL15_STATUS_EYE_ OPENING	R	N/A	A	This is an information about the quality of serial link eye number 15. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed

Table 67. B_HSSL_STATUS_EYE_DRIFT_1 @0x0106

Bit	Field	Type	Default value	Core	Description
15:14	B_HSSL7_STATUS_EYE_DRIFT	R	N/A	B	This is a warning when the serial link eye has drifted and reached the limit of reception. The drift can be due to a variation of temperature for example. 11: warning, eye has reached the sampling limit 10 or 10 : warning, eye is near the sampling limit 00: status OK
13:12	B_HSSL6_STATUS_EYE_DRIFT				
11:10	B_HSSL5_STATUS_EYE_DRIFT				
9:8	B_HSSL4_STATUS_EYE_DRIFT				
7:6	B_HSSL3_STATUS_EYE_DRIFT				
5:4	B_HSSL2_STATUS_EYE_DRIFT				
3:2	B_HSSL1_STATUS_EYE_DRIFT				
1:0	B_HSSL0_STATUS_EYE_DRIFT				

Table 68. B_HSSL_STATUS_EYE_DRIFT_2 @0x0107

Bit	Field	Type	Default value	Core	Description
15:14	B_HSSL15_STATUS_EYE_DRIFT	R	N/A	B	This is a warning when the serial link eye has drifted and reached the limit of reception. The drift can be due to a variation of temperature for example. 11: warning, eye has reached the sampling limit 10 or 10 : warning, eye is near the sampling limit 00: status OK
13:12	B_HSSL14_STATUS_EYE_DRIFT				
11:10	B_HSSL13_STATUS_EYE_DRIFT				
9:8	B_HSSL12_STATUS_EYE_DRIFT				
7:6	B_HSSL11_STATUS_EYE_DRIFT				
5:4	B_HSSL10_STATUS_EYE_DRIFT				
3:2	B_HSSL9_STATUS_EYE_DRIFT				
1:0	B_HSSL8_STATUS_EYE_DRIFT				

Table 69. B_HSSL_STATUS_EYE_OPENING_1 @0x0108

Bit	Field	Type	Default value	Core	Description
15					Reserved
14:12	B_HSSL4_STATUS_EYE_ OPENING	R	N/A	B	This is an information about the quality of serial link eye number 0 to 4. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed
11:9	B_HSSL3_STATUS_EYE_ OPENING				
8:6	B_HSSL2_STATUS_EYE_ OPENING				
5:3	B_HSSL1_STATUS_EYE_OPENING				
2:0	B_HSSL0_STATUS_EYE_OPENING				

Table 70. B_HSSL_STATUS_EYE_OPENING_2 @0x0109

Bit	Field	Type	Default value	Core	Description
15					Reserved
14:12	B_HSSL9_STATUS_EYE_OPENING	R	N/A	B	This is an information about the quality of serial link eye number 5 to 9. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed
11:9	B_HSSL8_STATUS_EYE_OPENING				
8:6	B_HSSL7_STATUS_EYE_OPENING				
5:3	B_HSSL6_STATUS_EYE_OPENING				
2:0	B_HSSL5_STATUS_EYE_OPENING				

Table 71. B_HSSL_STATUS_EYE_OPENING_3 @0x010A

Bit	Field	Type	Default value	Core	Description
15					Reserved
14:12	B_HSSL14_STATUS_EYE_OPENING	R	N/A	B	This is an information about the quality of serial link eye number 10 to 14. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed
11:9	B_HSSL13_STATUS_EYE_OPENING				
8:6	B_HSSL12_STATUS_EYE_OPENING				
5:3	B_HSSL11_STATUS_EYE_OPENING				
2:0	B_HSSL10_STATUS_EYE_OPENING				

Table 72. B_HSSL_STATUS_EYE_OPENING_4 @0x010B

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2:0	B_HSSL15_STATUS_EYE_OPENING	R	N/A	B	This is an information about the quality of serial link eye number 15. 111: eye's search is in progress 100: opening eye is very good 011: opening eye is good 010: opening eye is correct 001: opening eye is critical 000: eye's search failed

Table 73. A_ASINC_GAIN @0x0201

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	A_ASINC_GAIN	RW	0	A	11 1111 1111 : gain = 1023 * 2^{-12} (gain max) . . . . . . 00 0000 0010 : gain = 2 * 2^{-12} 00 0000 0001 : gain = 2^{-12} (gain step) 00 0000 0000 : gain = 0

Table 74. B_ASINC_GAIN @0x0301

Bit	Field	Type	Default value	Core	Description
15:10					Reserved

9:0	B_ASINC_GAIN	RW	0	B	11 1111 1111 : gain = 1023 * 2^{-12} (gain max) . . . . . . 00 0000 0010 : gain = 2 * 2^{-12} 00 0000 0001 : gain = 2^{-12} (gain step) 00 0000 0000 : gain = 0

Note: example for core B
Example for core B
GAIN = 1 – B_ASINC_GAIN * 2^{-12} if BEAMFORMING is disable
GAIN = 1 – B_BH_GAIN_ZONE_1 * 2^{-12} if BEAMFORMING is enable
GAIN = 1 – B_BH_GAIN_ZONE_(X) * 2^{-12} if BEAMHOPPING is enable, with X =1,2,3,4

Table 75. A_GAIN_CAL @0x0202

Bit	Field	Type	Default value	Core	Description
15:5					Reserved
4:0	A_ GAIN_CAL	RW OTP	0	A	1 1111 : gain_calibration = 31 * 2^{-12} . . . . . . 0 0010 : gain_calibration = 2 * 2^{-12} 0 0001 : gain_calibration = 2^{-12} 0 0000 : gain_calibration = 0

Table 76. B_ GAIN_CAL @0x0302

Bit	Field	Type	Default value	Core	Description
15:5					Reserved
4:0	B_ GAIN_CAL	RW OTP	0	B	1 1111 : gain_calibration = 31 * 2^{-12} . . . . . . 0 0010 : gain_calibration = 2 * 2^{-12} 0 0001 : gain_calibration = 2^{-12} 0 0000 : gain_calibration = 0

Table 77. A_ASINC_OVERFLOW @0x0203

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_ASINC_OVERFLOW	R	N/A	A	1: filter for anti-sinc are in overflow 0: filter for anti-sinc are in range

Table 78. B_ASINC_OVERFLOW @0x0303

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_ASINC_OVERFLOW	R	N/A	B	1: filter for anti-sinc are in overflow 0: filter for anti-sinc are in range

Table 79. A_ASINC_OVERFLOW_CLEAR @0x0204

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_ASINC_OVERFLOW_CLEAR	W	N/A	A	The action of writing in this register causes the reset of the overflow flag A_ASINC_OVERFLOW

Table 80. B_ASINC_OVERFLOW_CLEAR @0x0304

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_ASINC_OVERFLOW_CLEAR	W	N/A	B	The action of writing in this register causes the reset of the overflow flag B_ASINC_OVERFLOW

Table 81. A_ASINC_COEFF_1 @0x0205

Bit	Field	Type	Default value	Core	Description
15:09					Reserved
8:0	A_ASINC_COEFF_1	RW	0x 080	A	[6:0] bits are fractional 10 0000000= gain of 2.0 value 01 0000000= gain of 1.0 value (default) 00 0000000= gain of 0.0 value See NOTE below

Note: internal calculations use **two's complement** representation.

Example: for A_ASINC_COEFF_1 with 9 bits the mapping would be:
0x0FF → 2.0 - 2^{-7}
0x0FE → 2.0 - 2*2^{-7}
…
0x080 → 1.0
…
0x001 → 2^{-7}
0x000 → 0.0
0x1FF → -2^{-7}
…
0x101 → -2.0 + 2^{-7}
0x100 → -2.0

Table 82. A_ASINC_COEFF_2 @0x0206

Bit	Field	Type	Default value	Core	Description
15:8					Reserved
7:0	A_ASINC_COEFF_2	RW	0	A	[6:0] bits are fractional 1000 0000 = gain of 1.0 value 0000 0000 = gain of 0.0 value (default) See NOTE below

Notes:
- If A_ASINC_COEFF_1= 1.0 and A_ASINC_COEFF_2=0 then the ASINC function is disabled for core A.
- Internal calculations use **two's complement** representation.

Example: for A_ASINC_COEFF_2 with 8 bits the mapping would be:
0x7F → 1.0 - 2^{-7}
0x7E → 1.0 - 2*2^{-7}
…
0x01 → 2^{-7}
0x00 → 0.0
0xFF → -2^{-7}
…
0x81 → -1.0 + 2^{-7}
0x100 → -1.0

Table 83. B_ASINC_COEFF_1 @0x0305

Bit	Field	Type	Default value	Core	Description
15:9					Reserved
8:0	B_ASINC_COEFF_1	RW	0x 080	B	[6:0] bits are fractional 10 0000000= gain of 2.0 value 01 0000000 = gain of 1.0 value (default) 00 0000000 = gain of 0.0 value See NOTE below

Table 84. B_ASINC_COEFF_2 @0x0306

Bit	Field	Type	Default value	Core	Description
15:8					Reserved
7:0	B_ASINC_COEFF_2	RW	0	B	[6:0] bits are fractional 1000 0000 = gain of 1.0 value 0000 0000 = gain of 0.0 value See NOTE below

Note: if B_ASINC_COEFF_1= 1.0 and B_ASINC_COEFF_2=0 then the ASINC function is disabled for core B

Table 85. A_DUC_OVERFLOW @0x0210

Bit	Field	Type	Default value	Core	Description
15:6					Reserved
5	A_DUC_OVER_FDELAY	R	N/A	A	Digital Up Converter Overflow in the Fractional Delay filter
4	A_DUC_OVER_MIXER				Digital Up Converter Overflow in the Mixer function
3	A_DUC_OVER_INT4				Digital Up Converter Overflow in the interpolation stage 4
2	A_DUC_OVER_INT3				Digital Up Converter Overflow in the interpolation stage 3
1	A_DUC_OVER_INT2				Digital Up Converter Overflow in the interpolation stage 2
0	A_DUC_OVER_INT1				Digital Up Converter Overflow in the interpolation stage 1

Table 86. B_ DUC_OVERFLOW @0x0310

Bit	Field	Type	Default value	Core	Description
15:6					Reserved
5	B_DUC_OVER_FDELAY	R	N/A	B	Digital Up Converter Overflow in the fractional delay filter
4	B_DUC_OVER_MIXER				Digital Up Converter Overflow in the mixer function
3	B_DUC_OVER_INT4				Digital Up Converter Overflow in the interpolation stage 4
2	B_DUC_OVER_INT3				Digital Up Converter Overflow in the interpolation stage 3
1	B_DUC_OVER_INT2				Digital Up Converter Overflow in the interpolation stage 2
0	B_DUC_OVER_INT1				Digital Up Converter Overflow in the interpolation stage 1

Table 87. A_DUC_OVER_INT1_CLEAR @0x0211

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_DUC_OVER_INT1_CLEAR	W	N/A	A	A writing in this register causes the reset of A_DUC_OVER_INT1 overflow

Table 88. B_DUC_OVER_INT1_CLEAR @0x0311

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_DUC_OVER_INT1_CLEAR	W	N/A	B	A writing in this register causes the reset of B_DUC_OVER_INT1 overflow

Table 89. A_DUC_OVER_INT2_CLEAR @0x0213

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_DUC_OVER_INT2_CLEAR	W	N/A	A	A writing in this register causes the reset of A_DUC_OVER_INT2 overflow

Table 90. B_DUC_OVER_INT2_CLEAR @0x0313

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_DUC_OVER_INT2_CLEAR	W	N/A	B	A writing in this register causes the reset of B_DUC_OVER_INT2 overflow

Table 91. A_DUC_OVER_INT3_CLEAR @0x0215

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_DUC_OVER_INT3_CLEAR	W	N/A	A	A writing in this register causes the reset of A_DUC_OVER_INT3 overflow

Table 92. B_DUC_OVER_INT3_CLEAR @0x0315

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_DUC_OVER_INT3_CLEAR	W	N/A	B	A writing in this register causes the reset of B_DUC_OVER_INT3 overflow

Table 93. A_DUC_OVER_INT4_CLEAR @0x0217

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_DUC_OVER_INT4_CLEAR	W	N/A	A	A writing in this register causes the reset of A_DUC_OVER_INT4 overflow

Table 94. B_DUC_OVER_INT4_CLEAR @0x0317

Bit	Field	Type	Default value	Core	Description

15:1					Reserved
0	B_DUC_OVER_INT4_CLEAR	W	N/A	B	A writing in this register causes the reset of B_DUC_OVER_INT4 overflow

Table 95. A_DUC_OVER_MIXER_CLEAR @0x0219

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_DUC_OVER_MIXER_CLEAR	W	N/A	A	A writing in this register causes the reset of A_DUC_OVER_MIXER overflow

Table 96. B_DUC_OVER_ MIXER _CLEAR @0x0319

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_DUC_OVER_MIXER_CLEAR	W	N/A	B	A writing in this register causes the reset of B_DUC_OVER_MIXER overflow

Table 97. A_DUC_OVER_FDELAY_CLEAR @0x021B

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_DUC_OVER_FDELAY_CLEAR	W	N/A	A	A writing in this register causes the reset of A_DUC_OVER_FDELAY overflow

Table 98. B_DUC_OVER_FDELAY_CLEAR @0x031B

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_DUC_OVER_FDELAY_CLEAR	W	N/A	B	A writing in this register causes the reset of B_DUC_OVER_FDELAY overflow

Table 99. A_IIR_ROUNDING_ENA @0x0220

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_IIR_ROUDING_ENA	RW	0	A	Enable IIR filter compensation of NCO accumulator quantization error Default OFF, can be enabled if an issue is observed with phase accumulator quantization

Table 100. B_IIR_ROUNDING_ENA @0x0320

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_IIR_ROUDING_ENA	RW	0	B	Enable IIR filter compensation of NCO accumulator quantization error Default OFF, can be enabled if an issue is observed with phase accumulator quantization

Table 101. A_CHIRP_MIN_FREQ_LSB @0x0230

Bit	Field	Type	Default value	Core	Description
15:0	A_CHIRP_MIN_FREQ_LSB	RW	0	A	Starting frequency bit[15:0] for CHIRP mode See NOTE below for more information

Table 102. A_CHIRP_MIN_FREQ_MSB @0x0231

Bit	Field	Type	Default value	Core	Description
15:0	A_CHIRP_MIN_FREQ_MSB	RW	0	A	Starting frequency bit[31:16] for CHIRP mode See NOTE below for more information

Table 103. A_CHIRP_MAX_FREQ_LSB @0x0232

Bit	Field	Type	Default value	Core	Description
15:0	A_CHIRP_MAX_FREQ_LSB	RW	0	A	Stop frequency bit[15:0] for CHIRP mode See NOTE below for more information

Table 104. A_CHIRP_MAX_FREQ_MSB @0x0233

Bit	Field	Type	Default value	Core	Description
15:0	A_CHIRP_MAX_FREQ_MSB	RW	0	A	Stop frequency bit[31:16] for CHIRP mode See NOTE below for more information

Note for MIN and MAX frequency:
Programming example with a 12 GSps sampling rate, the frequency size is 32 bit.
FFFF FFFF = 12.000 GHz
0FFF FFFF = 12000/16 = 750.000 MHz
00FF FFFF = 12000/256 = 46.875 MHz
000F FFFF = 12000/4096 = 2.929 MHz
0001 FFFF = 366.210 KHz
0000 FFFF = 183.105 KHz
0000 0FFF = 11.444 KHz
0000 00FF = 715 Hz
0000 000F = 45 Hz

Table 105. A_CHIRP_STEP_FREQ_LSB @0x0234

Bit	Field	Type	Default value	Core	Description
15:0	A_CHIRP_STEP_FREQ_LSB	RW	0	A	Frequency bit[15:0] step for CHIRP mode See NOTE below for more information

Table 106. A_CHIRP_STEP_FREQ_MSB @0x0235

Bit	Field	Type	Default value	Core	Description
15:0	A_CHIRP_STEP_FREQ_MSB	RW	0	A	Frequency bit[31:16] step for CHIRP mode See NOTE below for more information

Note:
For a 12GSps sampling rate, the sweep rate is settable from 2.095 GHz/s to $4.5*10^9$ GHz/s in steps of 2.095 GHz/s.
The highest sweep rates are not usable since they go through the whole Nyquist band in 16 clock cycles (with clock cycle = 1/Fs).
Programming example for frequency step (the frequency step size is 32 bit):

0008 0000 ≥ 10^6 GHz/s	= 1.098 MHz/ns	= 1.464 MHz/”16 samples”
0000 FFFF =137 295 GHz/s	= 137 295 Hz/ns	= 183 039 Hz/”16 samples”
0000 000F = 33.520 GHz/s	= 33.520 Hz/ns	= 44.690 Hz/”16 samples”
0000 0001 = 2.095 GHz/s	= 2.095 Hz/ns	= 2.793 Hz/”16 samples”

Table 107. A_CHIRP_REPEAT @0x0237

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_CHIRP_REPEAT	RW	1	A	1: Automatic repeat another CHIRP after reaching the MAX frequency 0: DC level after reaching the MAX frequency

Table 108. A_CHIRP_RESET_TO_ZERO @0x0238

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_CHIRP_RESET_TO_ZERO	RW	1	A	1: set DC level to zero between successive chirps 0: set DC level between successive chirps

Table 109. B_CHIRP_MIN_FREQ_LSB @0x0330

Bit	Field	Type	Default value	Core	Description
15:0	B_CHIRP_MIN_FREQ_LSB	RW	0	B	Starting frequency bit[15:0] for chirp See NOTE below for more information

Table 110. B_CHIRP_MIN_FREQ_MSB @0x0331

Bit	Field	Type	Default value	Core	Description
15:0	B_CHIRP_MIN_FREQ_MSB	RW	0	B	Starting frequency bit[31:16] for chirp See NOTE below for more information

Table 111. B_CHIRP_MAX_FREQ_LSB @0x0332

Bit	Field	Type	Default value	Core	Description
15:0	B_CHIRP_MAX_FREQ_LSB	RW	0	B	Stop frequency bit[15:0] for chirp See NOTE below for more information

Table 112. B_CHIRP_MAX_FREQ_MSB @0x0333

Bit	Field	Type	Default value	Core	Description
15:0	B_CHIRP_MAX_FREQ_MSB	RW	0	B	Stop frequency bit[31:16] for chirp See NOTE below for more information

Note for MIN and MAX frequency:
Programming example with a 12 GSps sampling rate, the frequency size is 32 bit.
FFFF FFFF = 12.000 GHz
0FFF FFFF = 12000/16 = 750.000 MHz
00FF FFFF = 12000/256 = 46.875 MHz
000F FFFF = 12000/4096 = 2.929 MHz
0001 FFFF = 366.210 KHz
0000 FFFF = 183.105 KHz
0000 0FFF = 11.444 KHz
0000 00FF = 715 Hz
0000 000F = 45 Hz

Table 113. B_CHIRP_STEP_FREQ_LSB @0x0334

Bit	Field	Type	Default value	Core	Description

15:0	B_CHIRP_STEP_FREQ_LSB	RW	0	B	Frequency bit[15:0] step (rate) for chirp See NOTE below for more information

Table 114. B_CHIRP_STEP_FREQ_MSB @0x0335

Bit	Field	Type	Default value	Core	Description
15:0	B_CHIRP_STEP_FREQ_MSB	RW	0	B	Frequency bit[31:16] step (rate) for chirp See NOTE below for more information

Note:
For a 12GSps sampling rate, the sweep rate is settable from 2.095 GHz/s to $4.5*10^9$ GHz/s in steps of 2.095 GHz/s.
The highest sweep rates are not usable since they go through the whole Nyquist band in 16 clock cycles (with clock cycle = 1/Fs).
Programming example for frequency step (the frequency step size is 32 bit):
0008 0000 ≥ 10^6 GHz/s = 1.098 MHz/ns = 1.464 MHz/sample = 65.445 MHz/"16 samples"
0000 FFFF =137 295 GHz/s = 137 295 Hz/ns = 183 039 Hz/sample = 2.928 MHz/"16 samples"
0000 000F = 33.520 GHz/s = 33.520 Hz/ns = 44.690 Hz/sample = 715.090 Hz/"16 samples"
0000 0001 = 2.095 GHz/s = 2.095 Hz/ns = 2.793 Hz/sample = 44.693 Hz/"16 samples"

Table 115. B_CHIRP_REPEAT @0x0337

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_CHIRP_REPEAT	RW	1	B	Enable automatic repeat of chirp after reaching stop frequency

Table 116. B_CHIRP_RESET_TO_ZERO @0x0338

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_CHIRP_RESET_TO_ZERO	RW	1	B	Set DC level to zero between successive chirps

Table 117. A_NCO_LSB @0x0241

Bit	Field	Type	Default value	Core	Description
15:0	A_NCO_LSB	RW	0	A	Frequency bit[15:0] for mixer/DDS

Table 118. A_NCO_MSB @0x0242

Bit	Field	Type	Default value	Core	Description
15:0	A_NCO_MSB	RW	0	A	Frequency bit[31:16] for mixer/DDS

Table 119. B_NCO_LSB @0x0341

Bit	Field	Type	Default value	Core	Description
15:0	B_NCO_LSB	RW	0	B	Frequency bit[15:0] for mixer/DDS

Table 120. B_NCO_MSB @0x0342

Bit	Field	Type	Default value	Core	Description
15:0	B_NCO_MSB	RW	0	B	Frequency bit[31:16] for mixer/DDS

Table 121. A_FH_CLEAR_PHASE @0x0243

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_FH_CLEAR_PHASE	RW	1	A	1: mixer phase is reset when hopping. (default) 0: mixer keeps the current phase when hopping.

Table 122. A_FH_ROT_MIXER @0x0244

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2:0	A_FH_ROT_MIXER	RW	0	A	Shift of one of the complex mixer phase

Table 123. A_PHASE_OFFSET_LSB @0x0245

Bit	Field	Type	Default value	Core	Description
15:0	A_PHASE_OFFSET_LSB	RW	0	A	Optional constant phase offset bit[15:0] to add to mixer.

Table 124. A_ PHASE_OFFSET_MSB @0x0246

Bit	Field	Type	Default value	Core	Description
15:0	A_PHASE_OFFSET_MSB	RW	0	A	Optional constant phase offset bit[31:16] to add to mixer.

Table 125. B_FH_CLEAR_PHASE @0x0343

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_FH_CLEAR_PHASE	RW	1	B	1: mixer phase is reset when hopping. (default) 0: mixer keeps the current phase when hopping.

Table 126. B_FH_ROT_MIXER @0x0344

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2:0	B_FH_ROT_MIXER	RW	0	B	Shift of one of the complex mixer phase

Table 127. B_PHASE_OFFSET_LSB @0x0345

Bit	Field	Type	Default value	Core	Description
15:0	B_PHASE_OFFSET_LSB	RW	0	B	Optional constant phase offset bit[15:0] to add to mixer.

Table 128. B_PHASE_OFFSET_MSB @0x0346

Bit	Field	Type	Default value	Core	Description
15:0	B_PHASE_OFFSET_MSB	RW	0	B	Optional constant phase offset bit[31:16] to add to mixer.

Table 129. A_DDS_AMPLITUDE @0x0250

Bit	Field	Type	Default value	Core	Description
15:14					Reserved
13:0	A_DDS_AMPLITUDE	RW	0	A	Amplitude for DDS

Table 130. B_DDS_AMPLITUDE @0x0350

Bit	Field	Type	Default value	Core	Description
15:14					Reserved
13:0	B_DDS_AMPLITUDE	RW	0	B	Amplitude for DDS

Table 131. A_BH_CLEAR_PHASE @0x0260

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	A_BEAMHOP_CLEAR_PHASE	RW	1	A	1: phase is cleared when we switch to the next zone 0: phase is not cleared when we switch to next zone Next zone = new gain, new delay

Table 132. A_BH_GAIN_ZONE1 @0x0261

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	A_BH_GAIN_ZONE1	RW	0	A	Gain for beamforming first zone

Table 133. A_BH_DELAY_COARSE_ZONE1 @0x0262

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	A_BH_DELAY_COARSE_ZONE1	RW	0x 8	A	Coarse delay for beamforming first zone

Table 134. A_BH_DELAY_FINE_ZONE1 @0x0263

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	A_BH_DELAY_FINE_ZONE1	RW	0	A	Fine delay for beamforming first zone

Table 135. A_BH_GAIN_ZONE2 @0x0264

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	A_BH_GAIN_ZONE2	RW	0	A	Gain for beamforming second zone

Table 136. A_BH_DELAY_COARSE_ZONE2 @0x0265

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	A_BH_DELAY_COARSE_ZONE2	RW	0x 8	A	Coarse delay for beamforming second zone

Table 137. A_BH_DELAY_FINE_ZONE2 @0x0266

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	A_BH_DELAY_FINE_ZONE2	RW	0	A	Fine delay for beamforming second zone

Table 138. A_BH_GAIN_ZONE3 @0x0267

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	A_BH_GAIN_ZONE3	RW	0	A	Gain for beamforming third zone

Table 139. A_BH_DELAY_COARSE_ZONE3 @0x0268

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	A_BH_DELAY_COARSE_ZONE3	RW	0x 8	A	Coarse delay for beamforming third zone

Table 140. A_BH_DELAY_FINE_ZONE3 @0x0269

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	A_BH_DELAY_FINE_ZONE3	RW	0	A	Fine delay for beamforming third zone

Table 141. A_BH_GAIN_ZONE4 @0x026A

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	A_BH_GAIN_ZONE4	RW	0	A	Gain for beamforming fourth zone

Table 142. A_BH_DELAY_COARSE_ZONE4 @0x026B

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	A_BH_DELAY_COARSE_ZONE4	RW	0x 8	A	Coarse delay for beamforming fourth zone

Table 143. A_BH_DELAY_FINE_ZONE4 @0x026C

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	A_BH_DELAY_FINE_ZONE4	RW	0	A	Fine delay for beamforming fourth zone

Table 144. B_BH_CLEAR_PHASE @0x0360

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	B_BEAMHOP_CLEAR_PHASE	RW	0	B	1: phase is cleared when switching to the next zone 0: phase is not cleared when switching to next zone Next zone = new gain, new delay

Table 145. B_BH_GAIN_ZONE1 @0x0361

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	B_BH_GAIN_ZONE1	RW	0	B	Gain for beamforming first zone

Table 146. B_BH_DELAY_COARSE_ZONE1 @0x0362

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	B_BH_DELAY_COARSE_ZONE1	RW	0x 8	B	Coarse delay for beamforming first zone

Table 147. B_BH_DELAY_FINE_ZONE1 @0x0363

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	B_BH_DELAY_FINE_ZONE1	RW	0	B	Fine delay for beamforming first zone

Table 148. B_BH_GAIN_ZONE2 @0x0364

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	B_BH_GAIN_ZONE2	RW	0	B	gain for beamforming second zone

Table 149. B_BH_DELAY_COARSE_ZONE2 @0x0365

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	B_BH_DELAY_COARSE_ZONE2	RW	0x 8	B	Coarse delay for beamforming second zone

Table 150. B_BH_DELAY_FINE_ZONE2 @0x0366

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	B_BH_DELAY_FINE_ZONE2	RW	0	B	Fine delay for beamforming second zone

Table 151. B_BH_GAIN_ZONE3 @0x0367

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	B_BH_GAIN_ZONE3	RW	0	B	Gain for beamforming third zone

Table 152. B_BH_DELAY_COARSE_ZONE3 @0x0368

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	B_BH_DELAY_COARSE_ZONE3	RW	0x 8	B	Coarse delay for beamforming third zone

Table 153. B_BH_DELAY_FINE_ZONE3 @0x0369

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	B_BH_DELAY_FINE_ZONE3	RW	0	B	Fine delay for beamforming third zone

Table 154. B_BH_GAIN_ZONE4 @0x036A

Bit	Field	Type	Default value	Core	Description
15:10					Reserved
9:0	B_BH_GAIN_ZONE4	RW	0	B	Gain for beamforming fourth zone

Table 155. B_BH_DELAY_COARSE_ZONE4 @0x036B

Bit	Field	Type	Default value	Core	Description
15:4					Reserved
3:0	B_BH_DELAY_COARSE_ZONE4	RW	0x 8	B	Coarse delay for beamforming fourth zone

Table 156. B_BH_DELAY_FINE_ZONE4 @0x036C

Bit	Field	Type	Default value	Core	Description
15:7					Reserved
6:0	B_BH_DELAY_FINE_ZONE4	RW	0	B	Fine delay for beamforming fourth zone

Table 157. A_HSSL_POL @0x0280

Bit	Field	Type	Default value	Core	Description
15	A_HSSL_POL	RW	0	A	Inversion of pin N&P of Serial Link 15
14			0		Inversion of pin N&P of Serial Link 14
13			0		Inversion of pin N&P of Serial Link 13
12			0		Inversion of pin N&P of Serial Link 12
11			1		Inversion of pin N&P of Serial Link 11
10			0		Inversion of pin N&P of Serial Link 10
9			1		Inversion of pin N&P of Serial Link 9
8			0		Inversion of pin N&P of Serial Link 8
7			1		Inversion of pin N&P of Serial Link 7
6			1		Inversion of pin N&P of Serial Link 6
5			1		Inversion of pin N&P of Serial Link 5
4			1		Inversion of pin N&P of Serial Link 4
3			1		Inversion of pin N&P of Serial Link 3
2			1		Inversion of pin N&P of Serial Link 2
1			1		Inversion of pin N&P of Serial Link 1
0			1		Inversion of pin N&P of Serial Link 0

Table 158. B_HSSL_POL @0x0380

Bit	Field	Type	Default value	Core	Description
15	B_HSSL_POL	RW	0	B	Inversion of pin N&P of Serial Link 15
14			0		Inversion of pin N&P of Serial Link 14
13			0		Inversion of pin N&P of Serial Link 13
12			0		Inversion of pin N&P of Serial Link 12

11			1		Inversion of pin N&P of Serial Link 11
10			0		Inversion of pin N&P of Serial Link 10
9			1		Inversion of pin N&P of Serial Link 9
8			0		Inversion of pin N&P of Serial Link 8
7			1		Inversion of pin N&P of Serial Link 7
6			1		Inversion of pin N&P of Serial Link 6
5			1		Inversion of pin N&P of Serial Link 5
4			1		Inversion of pin N&P of Serial Link 4
3			1		Inversion of pin N&P of Serial Link 3
2			1		Inversion of pin N&P of Serial Link 2
1			1		Inversion of pin N&P of Serial Link 1
0			1		Inversion of pin N&P of Serial Link 0

Table 159. PLUS10_PERCENT_DAC_CORE @0x0400

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	B_PLUS10_PERCENT_DAC_CORE	RW	0	B	Enhance B output Gain by 10% 0 if BEAMFORMING/ASINC disable 1 if a gain amplification is needed when using BEAMFORMING / ASINC
0	A_PLUS10_PERCENT_DAC_CORE		0	A	Enhance A output Gain by 10%

Table 160. POWER_ON_CORE_ANA @0x0402

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	B_POWER_ON_CORE_ANA	RW	1	B	0 : Power OFF 1 : Power ON
0	A_POWER_ON_CORE_ANA		1	A	0 : Power OFF 1 : Power ON

Table 161. POWER_ON_MUX21 @0x0406

Bit	Field	Type	Default value	Core	Description
15:2					Reserved
1	B_POWER_ON_MUX21	RW	1	B	0 : Power OFF 1 : Power ON
0	A_POWER_ON_MUX21		1	A	0 : Power OFF 1 : Power ON

Table 162. A_LOOP_CFG @0x0270

Bit	Field	Type	Default value	Core	Description
7:4					Reserved
3:0	A_LOOP_CFG	RW	78	A	Manual Loop Delay timing adjustment 0000: 1 delay (6 ps) 0001: 2 delays (12 ps) 0010: 3 delays (18 ps) … 1111: 16 delays

Table 163. B_LOOP_CFG @0x0370

Bit	Field	Type	Default value	Core	Description
7:4					Reserved
3:0	B_LOOP_CFG	RW	78	B	Manual Loop Delay timing adjustment 0000: 1 delay (6 ps) 0001: 2 delays (12 ps) 0010: 3 delays (18 ps) … 1111: 16 delays

Table 164. SDA_MUX21 @0x0407

Bit	Field	Type	Default value	Core	Description
15:12					Reserved
11:0	SDA_MUX21	RW	820	AB	11:6: Internal timing adjustment for Core B 5:0: Internal timing adjustment for Core A See NOTE.

Note: only values between 0x10 and 0x2F are used.

Table 165. SYNC_FLAG @0x0500

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	SYNC_FLAG	R	N/A	AB	1: SYNC is in the forbidden area, SYNC edge and clock edge are too close 0: no timing violation with SYNC sample

Table 166. SYNC_FLAG_RST @0x0501

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	SYNC_FLAG_RST	W	N/A	AB	Writing in this register resets the SYNC_FLAG

Table 167. SYNC_CFG @0x0502

Bit	Field	Type	Default value	Core	Description
15:8					Reserved
7:6	COARSE_SYNC_SHIFT	RW	0	AB	External clock cycles added to SYNC: 11: 96 external clock cycles added 10: 64 external clock cycles added 01: 32 external clock cycles added 00: 0 external clock cycles added (default)
5	MEDIUM_SYNC_SHIFT		0		External clock cycles added to SYNC: 1: 16 external clock cycles added 0: 0 external clock cycles added (default)
4	LOW_SYNC_SHIFT		0		External clock cycles added to SYNC: 1: 8 external clock cycles added 0: 0 external clock cycles added (default)
3:1	FINE_SYNC_SHIFT		0		External clock cycles added to SYNC: 111: 7 external clock cycles added 110: 6 external clock cycles added 101: 5 external clock cycles added 100: 4 external clock cycles added 011: 3 external clock cycles added 010: 2 external clock cycles added 001: 1 external clock cycles added

					000: 0 external clock cycles added (default)
0	SYNC_EDGE_SEL		0		SYNC sample edge selection : 1: SYNC sample with falling edge 0: SYNC sample with rising edge (default)

Note: The SYNCO (SYNC output) is not affected by this register

Table 168. SHIFT_BUFFER @0x0503

Bit	Field	Type	Default value	Core	Description
15:6					Reserved
5:3	SHIFT_BUFFER	RW	0	B	For multi DAC synchronisation 100: data delay by 4*16 external clock cycles 011: data delay by 3*16 external clock cycles 010: data delay by 2*16 external clock cycles 001: data delay by 1*16 external clock cycles 000: no data delay (default)
2:0				A	For multi DAC synchronisation 100: data delay by 4*16 external clock cycles 011: data delay by 3*16 external clock cycles 010: data delay by 2*16 external clock cycles 001: data delay by 1*16 external clock cycles 000: no data delay

Table 169. BUFFER_CFG @0x0504

Bit	Field	Type	Default value	Core	Description
15:1					Reserved
0	BUFFER_CFG	RW	0	AB	0: manual delay, SHIFT_BUFFER is taken into account (default value) 1: Semi-automatic delay, SHIFT_BUFFER is automatically adjusted with the formula: LATENCY_FIRST_DATA + SHIFT_BUFFER = MAX_LATENCY_FIRST_DATA

Table 170. MAX_LATENCY_FIRST_DATA @0x0505

Bit	Field	Type	Default value	Core	Description
15:8	B_ MAX_LATENCY_FIRST_DATA	RW	0x 43	B	For multi DAC synchronisation
7:0	A_ MAX_LATENCY_FIRST_DATA		0x 43	A	For multi DAC synchronisation

Table 171. LATENCY_FIRST_DATA @0x0506

Bit	Field	Type	Default value	Core	Description
15:8	B_ LATENCY_FIRST_DATA	R	N/A	B	Counter between SYNC and first data of ESIstream protocol The unit is period of external clock /16
7:0	A_ LATENCY_FIRST_DATA			A	Counter between SYNC and first data of ESIstream protocol The unit is period of external clock /16

Table 172. SYNC_BUFFER_OVERFLOW @0x0507

Bit	Field	Type	Default value	Core	Description
15:2		R	N/A		Reserved
1	B_SYNC_BUFFER_OVERFLOW			B	Data alignment for multi DAC synchronization in order to have a deterministic and fixed latency 1: data buffer OVERFLOW

					0: data buffer OK
0	A_SYNC_BUFFER_OVERFLOW			A	Data alignment for multi DAC synchronization in order to have a deterministic and fixed latency 1: data buffer OVERFLOW 0: data buffer OK

Table 173. SERDES_ANA @0x0603

Bit	Field	Type	Default value	Core	Description
15:8		RW	55		Reserved
7:4	B_SERDES_ANA			B	7:6 To adjust the bandwidth (cutoff frequency) 00 : 9 GHz 01 : 6 GHz 11 : 2 GHz (the higher the bandwidth, the best it operates at high speed) 5:4 :To adjust low frequency (<500MHz) gain 00 : -6 dB 01 -2 dB 11 : 4 dB (Low gain can be used to enhanced high frequency operation)
3:0	A_SERDES_ANA			A	3:2 To adjust the bandwidth (cutoff frequency) 00 : 9 GHz 01 : 6 GHz 11 : 2 GHz (the higher the bandwidth, the best it operates at high speed) 1:0 :To adjust low frequency (<500MHz) gain 00 : -6 dB 01 -2 dB 11 : 4 dB (Low gain can be used to enhanced high frequency operation)

Table 174. PARITY_STATUS @0x060C

Bit	Field	Type	Default value	Core	Description
15:4		R	N/A		Reserved
3	B_ PARITY_STATUS_1_TO_15			B	Parity for link number 1 to 15 1 : Parity KO on at least one link 0 : Parity OK
2	B_ PARITY_STATUS_0			B	Parity for link number 0 1 : Parity KO 0 : Parity OK
1	A_ PARITY_STATUS_1_TO_15			A	Parity for link number 1 to 15 1 : Parity KO on at least one link 0 : Parity OK
0	A_ PARITY_STATUS_0			A	Parity for link number 0 1 : Parity KO 0 : Parity OK

Table 175. A_ESISTREAM_FLASH_STATUS @0x0610

Bit	Field	Type	Default value	Core	Description
15:0	A_ESISTREAM_FLASH_STATUS	R	N/A	A	FLASH STATUS FOR SYNCHRONISATION BETWEEN ESISTREAM & FPGA bit[15] = flash status for HSSL 15 bit[14] = flash status for HSSL 14

					... bit[1] = flash status for HSSL 1 bit[0] = flash status for HSSL 0 1: OK, flash pattern was found 0: FAILED, flash pattern was not found and a SYNC must be applied again

Table 176. A_ESISTREAM_PRBS_STATUS @0x0611

Bit	Field	Type	Default value	Core	Description
15:0	A_ESISTREAM_PRBS_STATUS	R	N/A	A	PRBS STATUS FOR SYNCHRONISATION BETWEEN ESISTREAM & FPGA bit[15] = PRBS status for HSSL 15 bit[14] = PRBS status for HSSL 14 ... bit[1] = PRBS status for HSSL 1 bit[0] = PRBS status for HSSL 0 1: OK, 32 PRBS patterns were found and they are correct 0: FAILED, error was detected in the 32 PRBS patterns and a SYNC must be applied again

Table 177. B_ESISTREAM_FLASH_STATUS @0x0612

Bit	Field	Type	Default value	Core	Description
15:0	B_ESISTREAM_FLASH_STATUS	R	N/A	B	FLASH STATUS FOR SYNCHRONISATION BETWEEN ESISTREAM & FPGA bit[15] = flash status for HSSL 15 bit[14] = flash status for HSSL 14 ... bit[1] = flash status for HSSL 1 bit[0] = flash status for HSSL 0 1: OK, flash pattern was found 0: FAILED, flash pattern was not found and a SYNC must be applied again

Table 178. B_ESISTREAM_PRBS_STATUS @0x0613

Bit	Field	Type	Default value	Core	Description
15:0	B_ESISTREAM_PRBS_STATUS	R	N/A	B	PRBS STATUS FOR SYNCHRONISATION BETWEEN ESISTREAM & FPGA bit[15] = PRBS status for HSSL 15 bit[14] = PRBS status for HSSL 14 ... bit[1] = PRBS status for HSSL 1 bit[0] = PRBS status for HSSL 0 1: OK, 32 PRBS patterns were found and they are correct 0: FAILED, error was detected in the 32 PRBS pattern and a SYNC must be applied again

Table 179. A_DDS_RAMP_MODE @0x0617

Bit	Field	Type	Default value	Core	Description
15:1		RW			Reserved
0	A_DDS_RAMP_MODE		0	A	Replace sinus by a ramp pattern

Table 180. B_DDS_RAMP_MODE @0x061C

Bit	Field	Type	Default value	Core	Description

15:1		RW			Reserved
0	B_DDS_RAMP_MODE		0	B	Replace sinus by a ramp pattern

Table 181. POWER_ON_TIMER @0x061E

Bit	Field	Type	Default value	Core	Description
15:3					Reserved
2	POWER_ON_CENTRAL_TIMER	RW	1	A & B	
1	B_POWER_ON_LOOP_TIMER		1	B	0 : Power OFF 1 : Power ON
0	A_POWER_ON_LOOP_TIMER		1	A	0 : Power OFF 1 : Power ON

13. APPLICATION INFORMATION

13.1 Power supplies recommendations & power-up sequence

13.1.1 Power-up sequence

A power-up sequence is mandatory to avoid any over-shoot currents. V_{CCA} has to be powered-up before V_{CCD_3} then V_{CCIO_A}/V_{CCIO_B}, then V_{CCD2_A}/ V_{CCD2_B} then V_{CCD1_A}/ V_{CCD1_B}.

13.1.2 Bypassing, decoupling and grounding

Each power supply has to be bypassed as close as possible to its source or access by 22 µF capacitors (value depending of DC/DC regulators).

In addition it is recommended to place decoupling capacitors (0402 chip size) on the bottom side of the PCB as described in Figure 64 and Table 182.

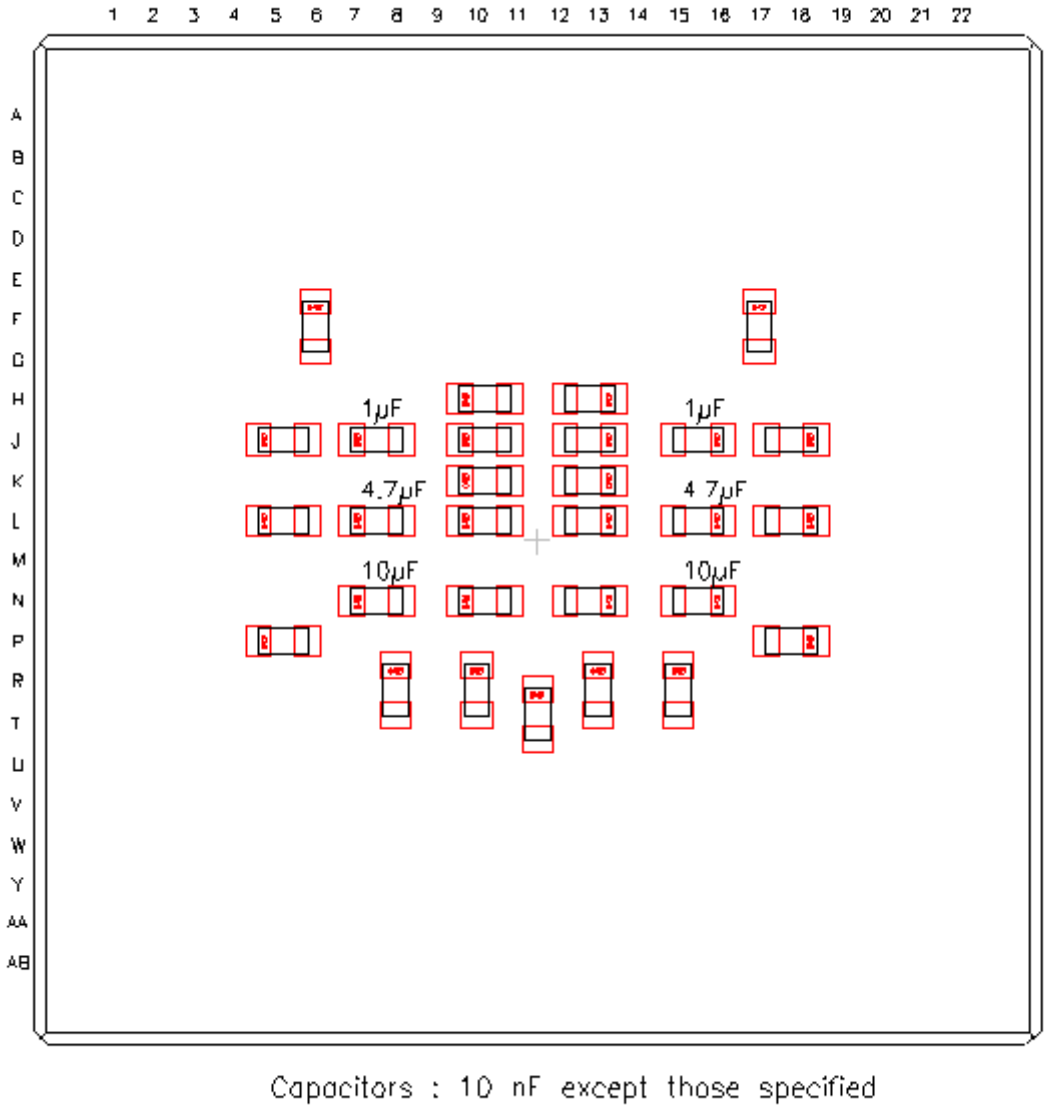


Figure 64: Power Supplies decoupling scheme (view from TOP of board through translucent board)

Table 182. List of recommended neighboring pins for power supply decoupling

(V_{CCA}, AGND)	
Pins (T8-R8) (T10-R10) (T13-R13) (T15-R15) Pins (N11-N10) (N12-N13)	10 nF
(V_{CCD_3}, AGND)	
Pins (R11-T11) (R12-T12)	10 nF
V_{CCD_1A}, DGND	
Pins (J7-J8) (K8-K7) (L8-L7) (M8-M7) (N8-N7)	1 µF, not used, 4.7 µF, not used, 10 µF

V_{CCD_1B}, DGND	
Pins (J16-J15) (K15-K16) (L15-L16) (M15-M16) (N15-N16)	1 µF, not used, 4.7 µF, not used, 10 µF

V_{CCD_2A}, DGND	
Pins (H10-H11) (J10-J11) (K10-K11) (L10-L11)	10 nF
V_{CCD_2B}, DGND	
Pins (H13-H12) (J13-J12) (K13-K12) (L13-L12)	10 nF
V_{CCIO_A}, GND_{IO_A}	
Pins (G6-F6) (J6-J5) (L6-L5) (P6-P5)	10 nF
V_{CCIO_B}, GND_{IO_B}	
Pins (G17-F17) (J17-J18) (L17-L18) (P17-P18)	10 nF

13.1.3 ESD and latchup

The customer shall be compliant to ANSI/ESD S20.20 and IEC 61340-5-1 standards.

- HBM: PASS at 50V on CLK, 125V on SYNC and 1KV on other pins. The DAC is declared as HBM Class 0Z in accordance with JS-001-2017
- CDM: PASS at 250V on all pins. The DAC is declared as CDM Class C0b in accordance with JS-002-2018
- Latchup: The DAC is compliant to latchup requirement in accordance with JESD78.

13.1.4 Single channel DAC mode

It is possible to use only one core (core A or core B).
In order to reduce the power consumption of the device and be able to use the SPI for registers access, Teledyne e2v recommends the following.

13.1.4.1 Core A only

Vccd2_B must be grounded.
Vccd_1B and Vccio_B must be powered (to be able to use the SPI for registers access)

Core B, MUX21 B and loop timer B blocks must be powered-off thanks to registers POWER_ON_CORE_ANA, POWER_ON_MUX21, POWER_ON_TIMER.
HSSL B links must be powered-off thanks to B_HSSL_POWER_ON register

13.1.4.2 Core B only

Vccd2_A must be grounded.

Vccd_1A and Vccio_A must be powered (to be able to use DIG_INx and DIG_MODEx inputs)

Core A, MUX21 A and loop timer A blocks must be powered-off thanks to registers POWER_ON_CORE_ANA, POWER_ON_MUX21, POWER_ON_TIMER

13.1.5 Lid connection

DD700 package lid is not grounded. This is a floating metal.
For space applications, to avoid charging issues, Teledyne e2v strongly recommends grounding package lid.

13.2 Interfaces configurations

13.2.1 DAC analog output

The analog output should be used as a differential signal, as described in the figures below.
If the application requires a single-ended analog output, then a balun is necessary to generate a single ended signal from the differential output of the DAC.

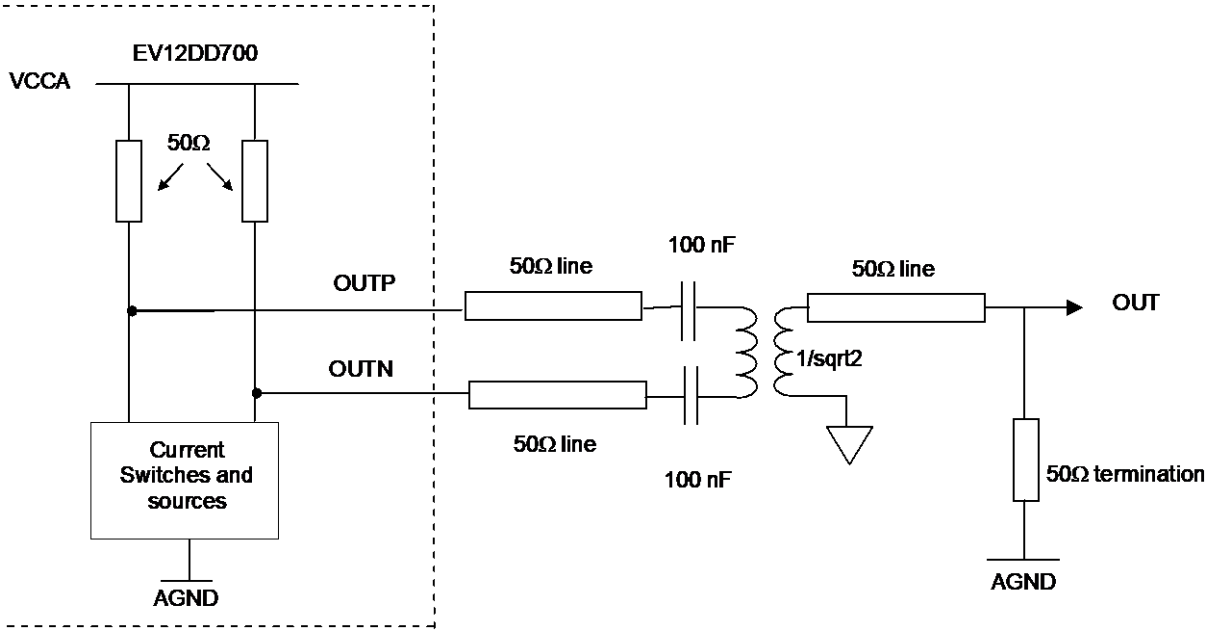


Figure 65: Analog output differential termination using a 1/sqrt(2) Balun

Note: 100nf AC coupling capacitors need to be High frequency broadband capacitors.

13.2.2 DAC clock input

The DAC input clock (sampling clock) should be provided as a differential signal as described in the following figures:

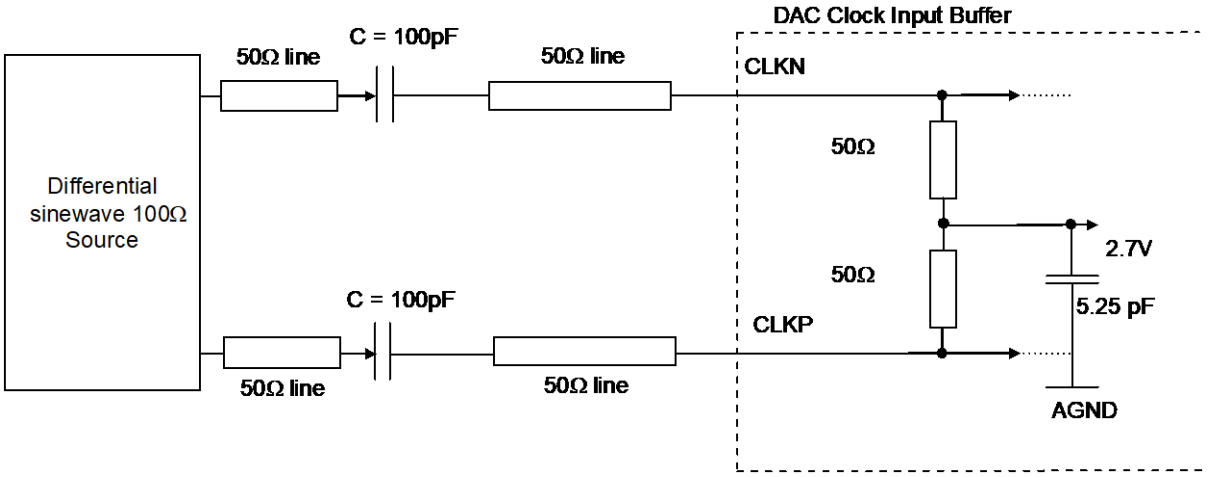


Figure 66: Clock input differential termination

Note: the buffer is internally pre-polarized to 2.7V (buffer between V_{CCA} and AGND).

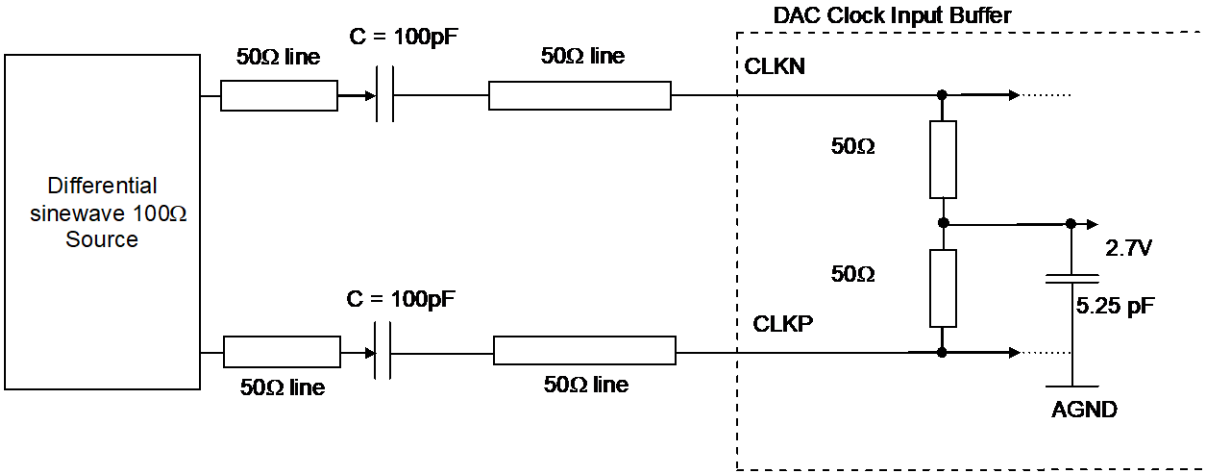


Figure 67: Clock input differential with balun

The AC coupling capacitor should be chosen as broadband capacitors with a value depending on the application.

13.2.3 DAC clock output (CLKout)

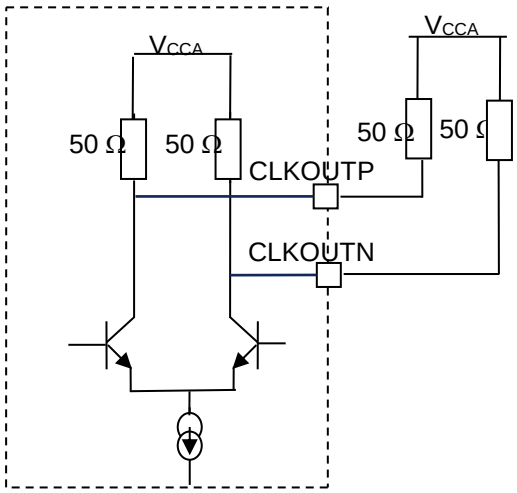


Figure 68: Clock output loading

If not used CLKout output buffer can be turned OFF and can remain open.

13.2.4 SSO and SYNCO

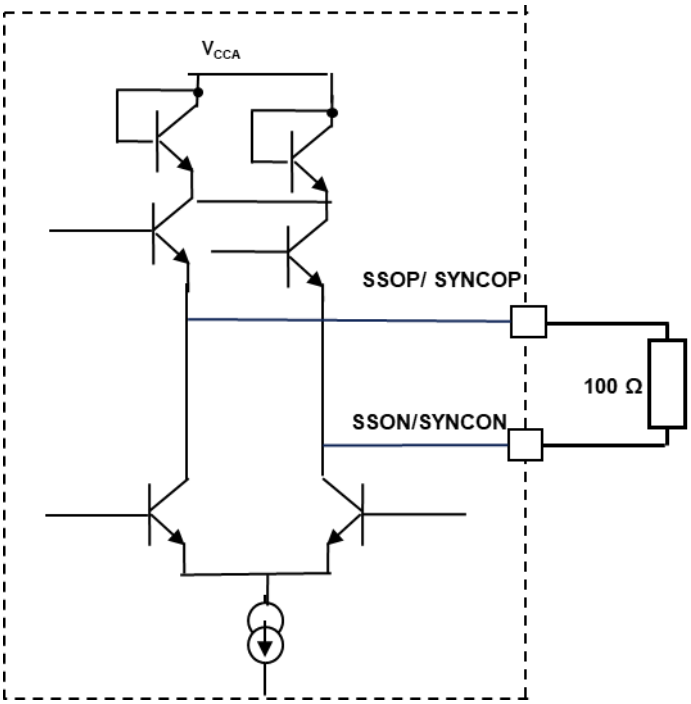


Figure 69: SSO and SYNCO output loading

If not used output buffer needs to be turned OFF.

13.2.5 Input Serial Lanes (HSSLs)

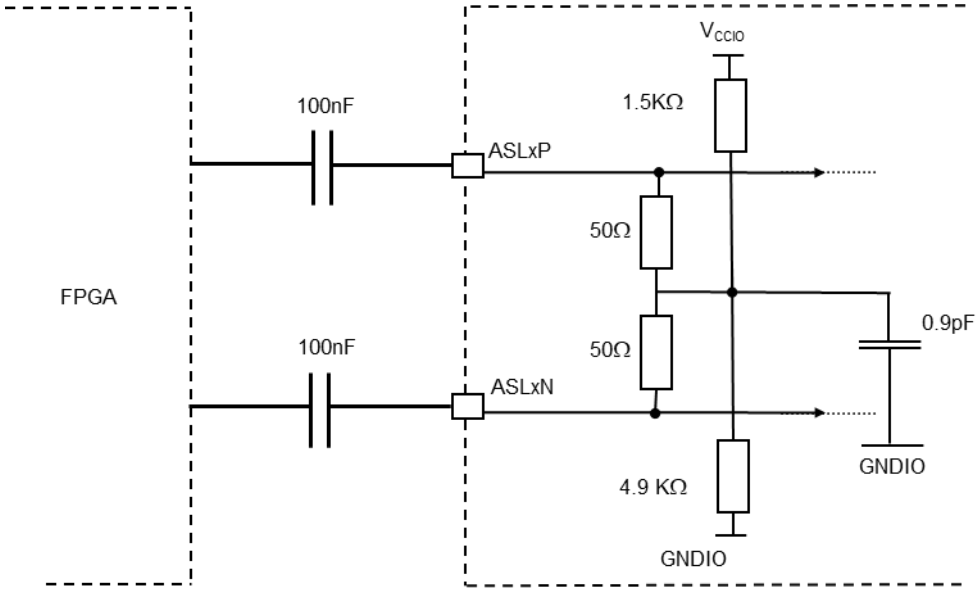


Figure 70: HSSL application scheme

Unused HSSLs must remain open (not connected).

14. ORDERING INFORMATION

Table 183. Ordering part numbers

Part Number	Package	Temperature Range	Screening Level	Comments
EVP8DD700UH	CBGA480 with SAC balls	Ambient	Prototype	8-bit initial prototype part. Further Part Numbers will be released in future datasheet revisions.
EVP8DD700JH	CBGA480 with Pb90Sn10 balls	Ambient	Prototype	8-bit initial prototype part. Further Part Numbers will be released in future datasheet revisions.
EVP12DD700UH	CBGA480 with SAC balls	Ambient	Prototype	12-bit initial prototype part. Further Part Numbers will be released in future datasheet revisions.
EVP12DD700JH	CBGA480 with Pb90Sn10 balls	Ambient	Prototype	12-bit initial prototype part. Further Part Numbers will be released in future datasheet revisions.
XDCHAIN480UH	CBGA480 With SAC balls	Ambient	Prototype	Refer to specification SP 31S 217230
XDCHAIN480JH	CBGA480 With Pb90Sn10 balls	Ambient	Prototype	Refer to specification SP 31S 217230

Table 184. Evaluation kit

Part Number	Temperature Range	Screening Level	Comments
EV12DD700A-EVM	Ambient	Prototype	
EVxxDD700-FPG-EVM	Ambient	Prototype	
EV12DD700A-2D-EVM	Ambient	Prototype	

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