# ADC 10-bit 2 Gsps Evaluation Board - TSEV83102G0B

## User Guide

**ATMEL** ®

# Table of Contents

**TSEV83102G0B - Evaluation Board User Guide**

# Section 1

# Overview

## 1.1 Description

The TSEV83102G0B Evaluation Board (EB) is a prototype board which has been designed in order to facilitate the evaluation and the characterization of the TS83102G0B device (in CBGA152) up to its 3 GHz full power bandwidth at up to 2 Gsps in the extended temperature range.

The high speed of the TS83102G0B requires careful attention to circuit design and layout to achieve optimal performance. This four metal layer board with an internal ground plane has the functions that allow a quick and simple evaluation of the TS83102G0B ADC performances over the temperature range.

The TS83102G0B Evaluation Board (EB) is very straightforward as it only implements the TS83102G0B ADC device, SMA connectors for input/output accesses and a 2.54 mm pitch connector compatible with high speed acquisition system high frequency probes.

The board has been designed to be fully compatible with Atmel's DMUX evaluation board (TSEV81102G0).

The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the input microstrip lines.

The board is constructed like a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board dimensions are 120 mm x 150 mm.

The board set comes fully assembled and tested, with the TS83102G0B installed and with a heatsink.

## 1.2    TSEV83102G0B Evaluation Board

*Figure 1-1.*  TSEV83102G0B Block Diagram

**TSEV83102G0B - Evaluation Board User Guide**
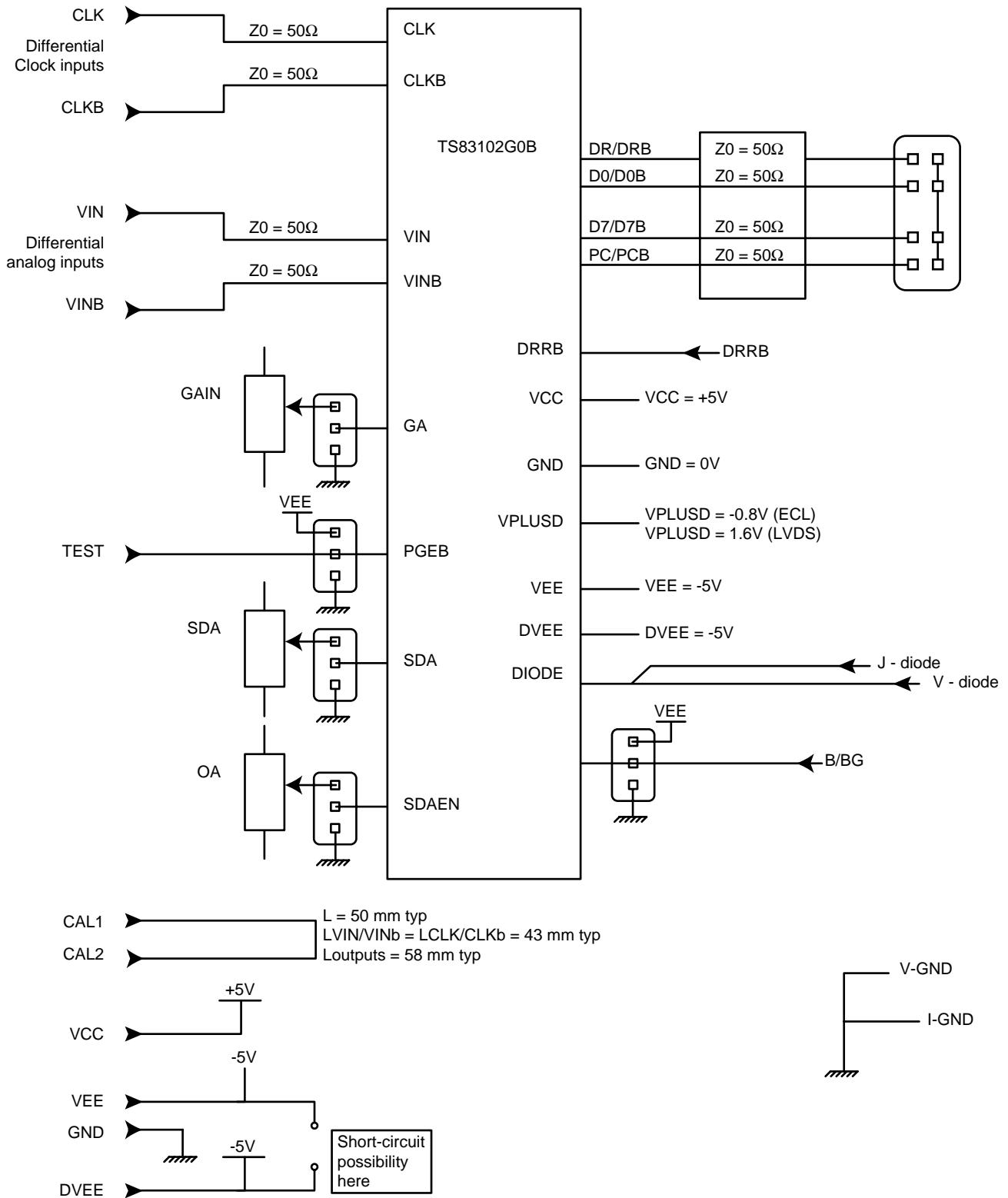
## 1.3 Board Mechanical Characteristics

The board's layer number, thickness, and functions are given below, from top to bottom.

***Table 1-1.*** Board's Layer Thickness Profile

| Layer | Characteristics |
|---|---|
| Layer 1<br>Copper layer | Copper thickness = 40 µm<br>AC signal traces = 50Ω microstrip lines<br>DC signal traces (B/GB, GAIN, DIODE, OA, TEST, SDA) |
| Layer 2<br>RO4003 dielectric layer<br>(Hydrocarbon/Wovenglass) | Layer thickness = 200 µm<br>Dielectric constant = 3.4 at 10 GHz<br>-0.044 dB/inch insertion loss at 2.5 GHz<br>-0.318 dB/inch insertion loss at 18 GHz |
| Layer 3<br>Copper layer | Copper thickness = 39 µm<br>Ground plane = reference plane 50Ω microstrip return |
| Layer 4<br>BT/Epoxy dielectric layer | Layer thickness = 330 µm |
| Layer 5<br>Copper layer | Copper thickness = 35 µm<br>Power and ground planes |
| Layer 6<br>BT/Epoxy dielectric layer | Layer thickness = 330 µm |
| Layer 7<br>Copper layer | Copper thickness = 35 µm<br>Power and ground planes (identical to layer 5) |
| Layer 8<br>BT/Epoxy dielectric layer | Layer thickness = 330 µm |
| Layer 9<br>Copper layer | Copper thickness = 35 µm<br>Ground planes (identical to layer 3) |
| Layer 10<br>BT/Epoxy dielectric layer | Layer thickness = 200 µm |
| Layer 11<br>Copper layer | Copper thickness = 35 µm<br>Power and ground planes |

The TSEV83102G0B is an eleven layer PCB made of six copper layers and five dielectric layers. The six metal layers correspond respectively from top to bottom to the AC and DC signals layer (layer 1), two ground layers (layers 3 and 5), and one supply layer (layer 7).

Considering the severe mechanical constraints due to the wide temperature range and the high frequency domain in which the board is to operate, it is necessary to use a sandwich of two different dielectric materials, with specific characteristics:

■ A low insertion loss RO4003 Hydrocarbon/Wovenglass dielectric layer of 200 µm thickness, chosen for its low loss (-0.318 dB/inch) and enhanced dielectric consistency in the high frequency domain. The RO4003 dielectric layer is dedicated to the routing of the 50Ω impedance signal traces (the RO4003 typical dielectric constant is 3.4 at 10 GHz). The RO4003 dielectric layer characteristics are very close to PTFE in terms of insertion loss characteristics.

■ A BT/Epoxy dielectric layer of 0.9 mm total thickness which is sandwiched between the upper ground plane and the back-side supply layer.

The BT/Epoxy layer has been chosen because of its enhanced mechanical characteristics for elevated temperature operation. The typical dielectric constant is 4.5 at 1 MHz.

More precisely, the BT/Epoxy dielectric layer offers enhanced characteristics compared to FR4 Epoxy, namely:

■ Higher operating temperature values: 170° C (125° C for FR4).

■ Better withstanding of thermal shocks (-65° C up to 170° C).

The total board thickness is 1.6 mm. The previously described mechanical and frequency characteristics makes the board particularly suitable for device evaluation and characterization in the high frequency domain and in military temperature ranges.

| 1.4 | **Analog Input, Clock Input and De-embedding Fixture Accesses** | The differential active inputs (Analog, Clock, De-embedding fixture) are provided by SMA connectors. |

Reference: VITELEC 142-0701-851.

Connector mounting plates have been used for fastening the SMA connectors.

**1.5 Digital Outputs Accesses**

Access to the differential output data port is provided by a 2.54 mm pitch connector, compatible with the high speed digital acquisition system. It enables access to the converter output data, as well as proper 50Ω differential termination.

**1.6 Power Supplies and Ground Accesses**

The power supply accesses are provided by five 2 mm section banana jacks respectively for $DV_{EE}$, $V_{EET}$, $V_{DD}$, $V_{PLUSD}$ and $V_{CC}$.

The power supply access is provided by one 4 mm section banana jack for $V_{EE}$.

The Ground accesses are provided by four 2 mm and one 4 mm banana jacks.

**1.7 ADC Function Setting Accesses**

For ADC function setting accesses (B/GB, Die junction temp., Test), 2 mm section banana jacks are provided.

Three potentiometers are provided for ADC gain adjust, Sampling delay adjust and Offset adjust.

One sub-screw is provided for Asynchronous data ready reset.

# Section 2

# Layout Information

| | | |
|---|---|---|
| **2.1** | **Board** | The TS83102G0B requires proper board layout for optimum full speed operation. |

The following explains the board layout recommendations and demonstrates how the Evaluation Board fulfills these implementation constraints.

A single low impedance ground plane is recommended, since it allows the user to lay out signal traces and power planes without interrupting the ground plane.

Therefore a multi-layer board structure has been retained for the TSEV83102G0B.

Six copper metal layers are used, dedicated respectively (from top to bottom) to the signal traces, ground planes and power supplies.

**2.2 AC Inputs/Digital Outputs**

The board uses 50Ω impedance microstrip lines for the differential analog inputs, clock inputs, and differential digital outputs.

The input signals and clock signals must be routed on one layer only, without using any through-hole vias. The line lengths are matched to within 2 mm.

The digital output lines are 50Ω differentially terminated.

The output data trace lengths are matched to within 0.25 inch (6 mm) to minimize the data output delay skew.

For the TSEV83102G0B the propagation delay is approximately 6.1 ps/mm (155 ps/inch). The RO4003 typical dielectric constant is 3.4 at 10 GHz.

For more informations about different output termination options refer to the specification application notes.

**2.3 DC Function Settings**

The DC signal traces are low impedance.

They have been routed with a 50Ω impedance near the device because of space restriction.

## 2.4    Power Supplies

The bottom metal layers 5 and 7 and 11 are dedicated to power supply traces ($V_{EE}$, $DV_{EE}$, $V_{EET}$, $V_{DD}$, $V_{PLUSD}$ and $V_{CC}$).

The supply traces are approximately 6 mm wide in order to present low impedance, and are surrounded by a ground plane connected to the two inner ground planes.

The analog and digital negative power supply traces are independent, but the possibility exists to short-circuit both supplies on the top metal layer).

No difference in ADC high speed performance is observed when connecting both negative supply planes together. Obviously one single negative supply plane could be used for the circuit.

Each power supply incoming is bypassed by a 1 µF Tantalum capacitor in parallel with 1 nF chip capacitor.

Each power supply access is decoupled very close to the device by 10 nF and 100 pF surface mount chip capacitors in parallel.

Note:    The decoupling capacitors are superposed. In this configuration, the 100 pF capacitors must be mounted first.

# Section 3

## Operating Procedures and Characteristics

**3.1  Introduction**

This section describes a typical single-ended configuration for analog inputs and clock inputs.

The single-ended configuration is preferable, as it corresponds to the most straightforward and quickest TSEV83102G0B board setting for evaluating the TS83102G0B at full speed in its temperature range.

The inverted analog input $V_{INB}$ and clock input CLKB common mode level is Ground (on-chip 50$\Omega$ terminated). In this configuration, no balun transformer is needed to convert properly the single-ended mixer output to balanced differential signals for the analog inputs.

In the same way, no balun is necessary to feed the TS83102G0B clock inputs with balanced signals.

Directly connect the RF sources to the in-phase analog and clock inputs of the converter.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

**3.2  Operating Procedure (ECL Mode)**

1. Connect the power supplies and Ground accesses
   ($V_{CC}$ = +5V, GND = 0V, $V_{PLUSD}$ = 0V, $V_{EE}$ = $DV_{EE}$ = -5V) through the dedicated banana jacks.
   The -5V power supplies should be turned on first.

   Note: one single -5V power supply can be used for supplying the digital $DV_{EE}$ and analog $V_{EE}$ power planes.

2. The board is set by default for digital outputs in binary format.

3. Connect the CLK clock signal.
   The inverted phase clock input CLKB may be left open (as on-chip 50$\Omega$ terminated). Use a low phase noise RF source. The clock input level is typically 4 dBm and should not exceed +10 dBm into the 50$\Omega$ termination resistor (maximum ratings for the clock input power level is 15 dBm).

4. Connect the analog signal $V_{IN}$. The inverted phase clock input $V_{INB}$ may be left open (as on cavity 50Ω terminated). Use a low phase noise RF source. Full scale range is 0.5V peak to peak around 0V, (±250 mV), or -2 dBm into 50Ω. Input frequency can range from DC up to 1.8 GHz. At 3.0 GHz, the ADC attenuates the input signal by -3 dB. The board insertion loss (S21) will be furnished in the definitive document release.

5. Connect the high speed data acquisition system probes to the output connector. The connector pitch (2.54 mm) is compatible with high speed digital acquisition system probes. The digital data are on-board differentially terminated. However, the output data can be picked up either in single-ended or differential mode.

## 3.3 Use with DMUX Evaluation Board

The TSEV81102G0 DMUX evaluation board has been designed to be fully compatible with the TSEV83102G0B ADC evaluation board.

The DEMUX input configuration has been optimized to be connected to the TS83102G0B ADC (CBGA152 package).

When using the DEMUX board with the ADC board, do not forget to set, for proper use, CLKINTYPE in mode DR/2 (jumper on-board).

The power-up sequence should be:

1. Supply the ADC first
2. Supply the DMUX
3. Perform an asynchronous reset on the DMUX board

When this power up sequence has been completed, the synchronization between the DEMUX and ADC boards can be achieved via the DEMUXDelADjCtrl potentiometer on the DEMUX evaluation board. To achieve a good synchronization between the two boards, it is recommended to run the ADC at its full speed (max sampling rate) and tune the DEMUX Delay Adjust Control potentiometer to the left and take down the settings for which the boards are de-synchronized and similarly to the right to see the loss of synchronization at the other extremity. The right setting of the potentiometer is in the middle of these two settings and should be right for all sampling rates of the ADC.

Please refer to the "ADCs and Demux Application Notes" document for more information.

## 3.4 Electrical Characteristics

*Table 3-1.* Absolute Maximum Ratings

| Parameter | Symbol | Comments | Value | Unit |
|---|---|---|---|---|
| Positive supply voltage | $V_{CC}$ | | GND to 5.5 | V |
| Digital negative supply voltage | $DV_{EE}$ | | GND to -5.5 | V |
| Digital positive supply voltage | $V_{PLUSD}$ | | GND -1.1 to 2.0 | V |
| Negative supply voltage | $V_{EE}$ | | GND to -5.5 | V |
| Maximum difference between negative supply voltages | $DV_{EE}$ to $V_{EE}$ | | 0.3 | V |
| Analog input voltages | $V_{IN}$ or $V_{INB}$ | | -1.5 to +1.5 | V |
| Maximum difference between $V_{IN}$ and $V_{INB}$ | $V_{IN}$ - $V_{INB}$ | | -1.5 to +1.5 | V |
| Clock input voltage | $V_{CLK}$ or $V_{CLKB}$ | | -1 to +1 | V |
| Maximum difference between $V_{CLK}$ and $V_{CLKB}$ | $V_{CLK}$ - $V_{CLKB}$ | | -1 to +1 | V |
| Static input voltage | $V_D$ | GA/SDA | -5 to +0.8 | V |
| Digital input voltage | $V_D$ | SDAEN, DRRB, B/GB, PGEB | -5 to +0.8 | V |
| Digital output voltage | $V_O$ | | $V_{PLUSD}$ -2.2 to $V_{PLUSD}$ +0.3 | V |
| Maximum junction temperature | $T_j$ | | +125 | °C |
| Storage temperature | $T_{stg}$ | | -65 to +150 | °C |
| Lead temperature (soldering 10s) | $T_{leads}$ | | +300 | °C |

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. The use of a thermal heat sink is mandatory.

## 3.5 Operating Characteristics

The power supplies denoted by $V_{CC}$, $V_{EE}$, $DV_{EE}$ and $V_{PLUSD}$ are dedicated to the TS83102G0B ADC.

The power supplies denoted $V_{EET}$, $V_{DD}$ are dedicated to the optional MC100EL16 asynchronous differential receivers.

***Table 3-2.*** Electrical Operating Characteristics

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Positive supply voltage (dedicated to TS83102G0B ADC only) | $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| | $V_{PLUSD}$ | – | ECL: -0.8 LVDS: 1.6 | – | V V |
| | $V_{EEA}$ | -5.25 | -5 | -4.75 | V |
| | $V_{EED}$ | -5.25 | -5 | -4.75 | V |
| Positive supply current (dedicated to TS83102G0B ADC only) | $I_{CC}$ | – | 144 | 205 | mA |
| | $I_{PLUSD}$ | – | 164 | – | mA |
| | $I_{EEA}$ | – | 514 | 630 | mA |
| | $I_{EED}$ | – | 170 | 180 | mA |
| Positive supply voltage not used by default – installed (dedicated to MC100EL16 differential receivers) | $V_{EET}$ | -5.25 | -5 | -4.75 | V |
| | $V_{DD}$ | -2.15 | -2 | -185 | V |
| Positive supply current not used by default – installed (dedicated to MC100EL16 differential receivers) | $I_{EET}$ | – | 180 | – | mA |
| | $I_{DD}$ | – | 480 | – | mA |
| Nominal power dissipation (without receivers) | PD | – | 4.6 | 5.1 ($T_J$ = 125°C) | W |
| Analog input impedance | $Z_{IN}$ | – | 50 | – | Ω |
| Full power analog input bandwidth (-3 dB) | – | – | 3.0 | – | GHz |
| Analog input voltage range (differential mode) | $V_{IN}$ | -125 | – | 125 | mV |
| Clock input impedance | – | – | 50 | – | Ω |
| Clock input voltage compatibility (single-ended or differential) (See Application Notes) | – | ECL levels or 4 dBm (typ) into 50Ω | | | – |
| Clock input power level into 50Ω termination resistor | – | -2 | 2 | 4 | dBm |

# Section 4

# Application Information

## 4.1 Introduction

For this section, also refer to the product "Main features" (TS83102G0B Datasheet). More particularly, refer to sections related to single-ended and differential input configurations.

## 4.2 Analog Inputs

The analog inputs can be entered in differential or single-ended mode without any high speed performance degradation.

The board digitizes single-ended signals by choosing either input and leaving the other input open, as the latter is on-board 50$\Omega$ terminated. The nominal in-phase inputs are $V_{IN}$ (See Section 3).

## 4.3 Clock Inputs

The clock inputs can be entered in differential or single-ended mode without any performance degradation for a clock frequency up to 500 MHz. At higher rates, it is recommended to drive the clock inputs differentially. Moreover, the typical in phase clock input amplitude is 1V peak to peak, centered on 0V (Ground), or -1.3V (ECL) on common mode.

As for the analog input, either clock input can be chosen (if the single-ended output mode is used), leaving the other input open, as both clock inputs are on-chip 50$\Omega$ terminated. The nominal in-phase clock input is CLK (Section 3).

## 4.4 Setting the Digital Output Data Format

For this section, refer to the Evaluation Board Electrical schematic and to the components placement document (respectively Figure 6-2 on page 6-3 and Figure 6-8 on page 6-4).

Refer also to the TS83102G0B specification about digital output coding.

The TS83102G0B delivers data in natural binary code or in Gray code. If the B/GB input is left floating or tied to GND the data format selected will be natural binary, if this input is tied to $V_{EE}$ the data will follow the Gray code.

Use the jumper denoted B/GB to select the output data port format:

- If B/GB is left floating or tied to GND, the data output format is true binary.

- If B/GB is tied to $V_{EE}$ or driven with ECL low level, the data outputs are in the Gray format.

The V$_{PLUSD}$ positive supply voltage allows the adjustment of the output common mode level from -1.05V (V$_{PLUSD}$ = -0.8V for ECL output compatibility) to +1.35V (V$_{PLUSD}$ = 1.6V for LVDS output compatibility).

Each output voltage varies between -0.9V and -1.2V (respectively +1.2V and +1.5V), leading to ±0.3V = 660 mV in differential for V$_{PLUSD}$ = -0.8V (respectively 1.6V).

**4.5    ADC Gain Adjust**    The ADC gain is adjustable by the means of pin R9 (pad input impedance is 1 MΩ in parallel with 2 pF). A jumper denoted GAIN has been foreseen in order to have access to the ADC gain adjust pin.

The GAIN potentiometer is dedicated to adjusting the ADC gain from approximately 0.85 up to 1.15.

The gain adjust transfer function is given below.

*Figure 4-1.* ADC Gain Adjust
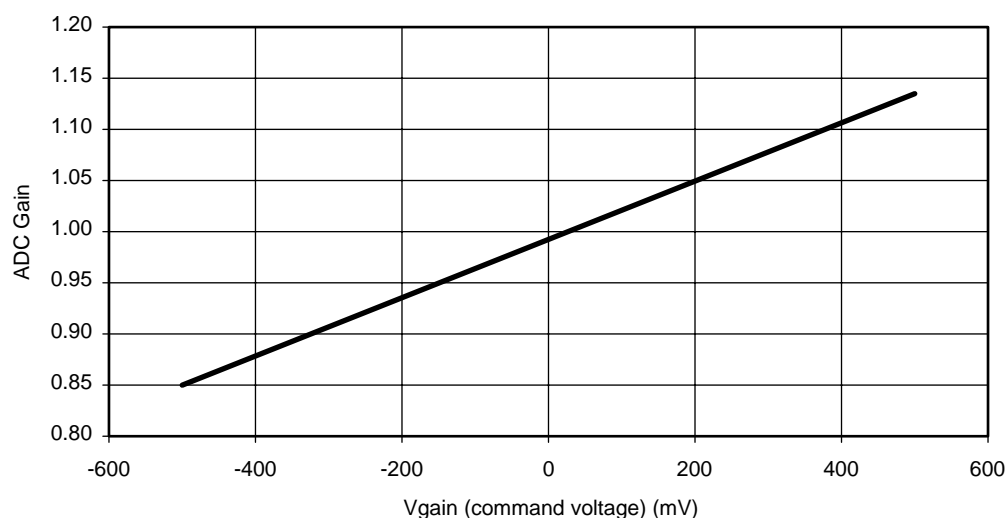


**4.6    SMA Connectors and Microstrip Lines De-embedding Fixture**    Attenuation in microstrip lines can be found by taking the difference in the log magnitudes of the S21 scattering parameters measured on two different lengths of meandering transmission lines.

Such a measurement also removes common losses such as those due to transitions and connectors.

The S21 scattering parameter corresponds to the amount of power transmitted through a two-port network.

The characteristic impedance of the microstrip meander lines must be close to 50Ω to minimize impedance mismatch with the 50Ω network analyzer test ports.

Impedance mismatch will cause ripples in the S21 parameter as a function of both the degree of mismatch and the length of the line.

**4.7    Die Junction Temperature Monitoring**

Figure 4-2 and Figure 4-3 illustrate the recommanded implementation of the die junction temperature monitoring function for the Revision B of the 10-bit 2 Gsps ADC.

The user has the choice between two possible configurations:

1.    The ADC decimation test mode is NOT ALLOWED.

Because of the use of 1 internal diode-mounted transistors, the user has to implement 2 x 2 head-to-tail protection diodes to avoid potential reverse current flows to damage the diode pin.

Note that Atmel usually recommends the use of 2 x 3 head-to-tail protection diodes but in this particular case, it is necessary to have exactly 2 diodes in the A10 to ground direction of conduction.

***Figure 4-2.***  Recommended Die Junction Temperature Monitoring Function Implementation, Test Mode Not Allowed
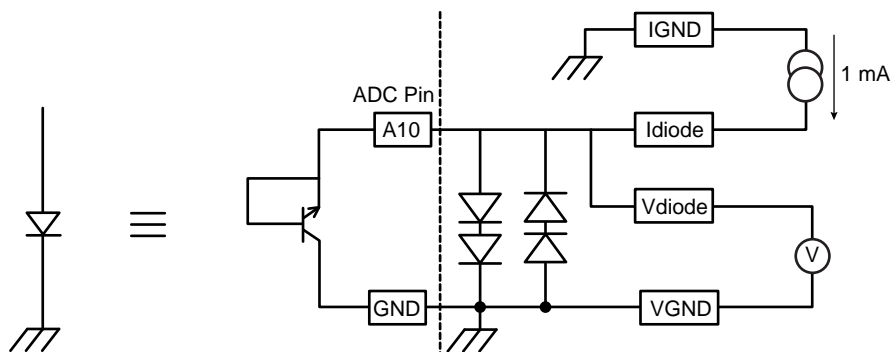


2.    The ADC test mode can be allowed

In case the user wants to still be able to switch from the normal mode to the test mode or to the die junction temperature monitoring, the protection diode configuration is slightly different and takes into account the fact that the test mode can be activated by applying $V_{EE}$ = -5V to the diode pin.

This explains why 7 protection diodes are needed in the other direction, as described in Figure 4-3.

***Figure 4-3.***  Recommended Diode Pin Implementation Allowing for Both Die Junction Temperature Monitoring Function and Test Mode
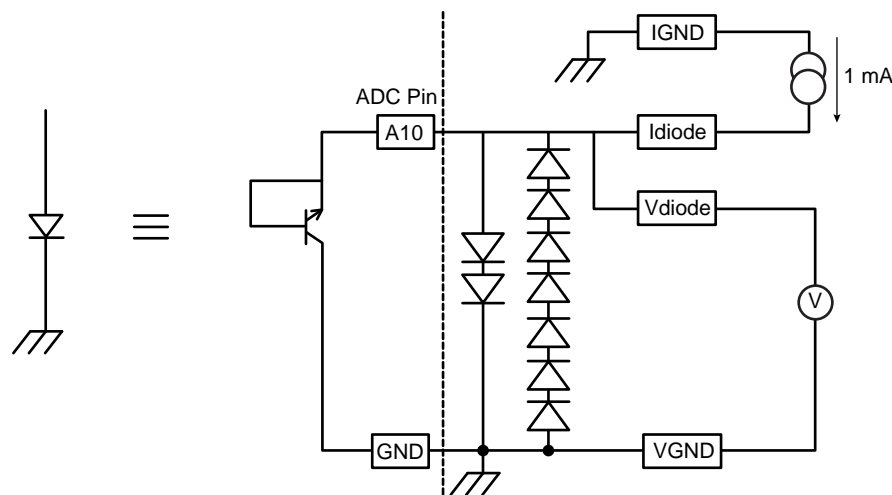
For Revision B, the $V_{DIODE}$ characteristic corresponds to a single diode characteristic over temperature, thus starting at 0.9V, as illustrated in Figure 4-4, which is only an interpolated $V_{DIODE}$ characteristic (to be confirmed by future measurements).

This modification in Revision B devices implies the modification of the processing of the $V_{DIODE}$ characteristic if any but above all, it allows the user to implement a digital temperature sensor to be interfaced with the ASIC (DSP, FPGA, etc...) loading the ADC.

*Figure 4-4.* Diode Pin Implementation in Test Mode
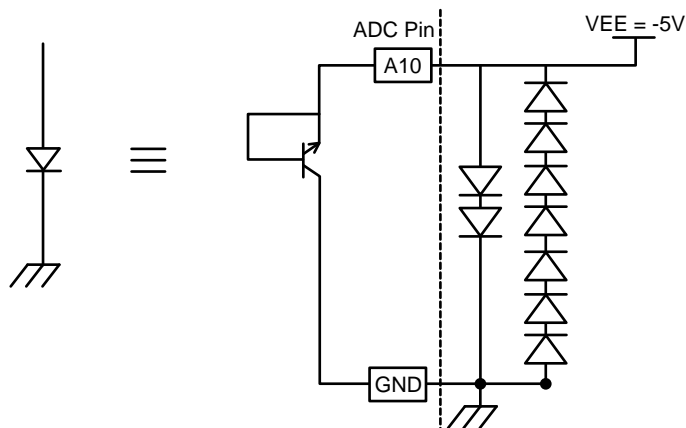


A typical configuration with a standard digital temperature sensor is depicted in Figure 4-5.

*Figure 4-5.* Typical Configuration with a Digital Temperature Sensor
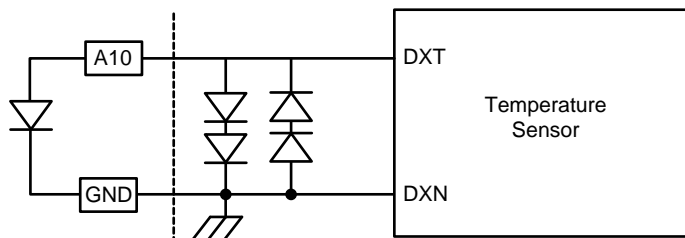
The expected diode mounted transistors $V_{DIODE}$ value (including chip parasitic resistance) versus junction temperature is given in Figure 4-6 ($I_{DIODE}$ = 1 mA).

***Figure 4-6.*** Junction Temperature Versus Diode Voltage for I = 1 mA
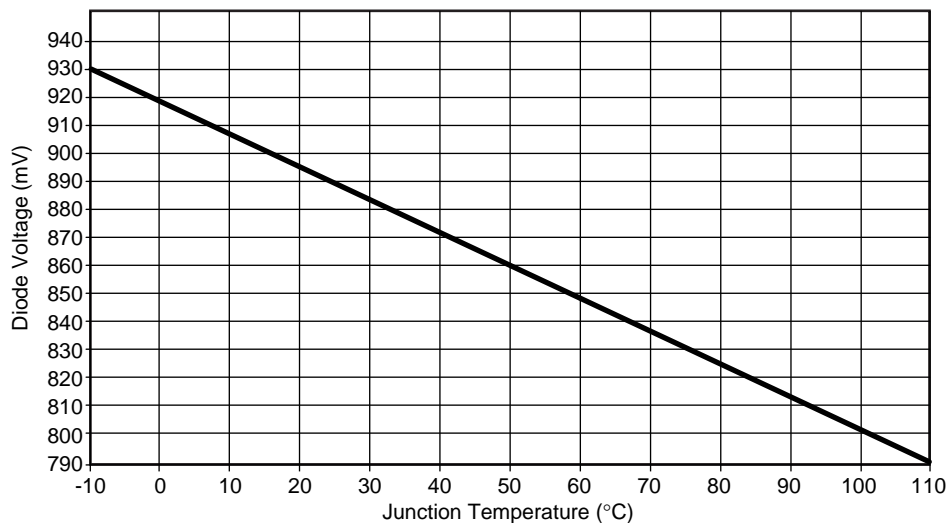


Note: The operating die junction temperature must be kept below 125° C; therefore, an adequate cooling system has to be set up.

## 4.8 Decimation Function

The decimation function can be used for debug of the ADC at initial stages. This function indeed allows to reduce the ADC output rate by 32, thus allowing for a quick debug phase of the ADC at maximum speed rate.

When active, this fuction makes the ADC output only 1 out of 32 data, thus resulting in a data rate which is 32 times slower than the clock rate.

## 4.9 Pattern Generator Enable

The TS83102G0B is able to generate by itself (without any analog input signal) a serie of patterns. If the TEST input is left floating or tied to GND the TS83102G0B will digitize the analog input signal according to B/GB. If this input is driven with ECL low level or tied to $V_{EE}$, TS83102G0B will generate Checker Board patterns.

Use the jumper denoted TEST for enabling the pattern generator.

| 4.10 | **Data Ready Output Signal Reset** | A sub-screw connector is provided for the DRRB command. |

The Data Ready signal is reset on the falling edge of the DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to $V_{EE}$ = -5V for Data Ready output signal master reset. As long as DRRB remains at a logical low level, (or tied to $V_{EE}$ = -5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data Ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typically.

TRDR is measured between the -1.3V point of the falling edge of the DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.
The Data Ready output signal restarts on the DRRB command rising edge, ECL logical high levels (-0.8V).

DRRB may also be grounded, or is allowed to float, for normal free running of the Data Ready output signal.

| 4.11 | **Sampling Delay Adjusting** | One delay adjust, controlled by SDA potentiometer, is available in order to add a delay to the input clock of the ADC. This allows the user to tune the instant of the internal sampling. To enable this delay adjustment there is an SDAEN pin on the chip. In the current revision, the SDAEN function corresponds to the OA labels (OA jumper and OA potentiometer). |

The OA potentiometer has been removed and short-circuited to $V_{EE}$.

Use the jumper denoted OA to enable the sampling delay adjustment:

■ If OA is left floating or tied to GND, the SDA is disabled

■ If OA is tied to $V_{EE}$, the SDA is enabled

The SDA input varies from -0.5 to 0.5V, according to the SDA potentiometer position.

The variation of the delay around its nominal value as a function of the SDA voltage is more or less linear, as shown in Figure 4-7 (simulation results).

*Figure 4-7.* Sampling Delay Adjust
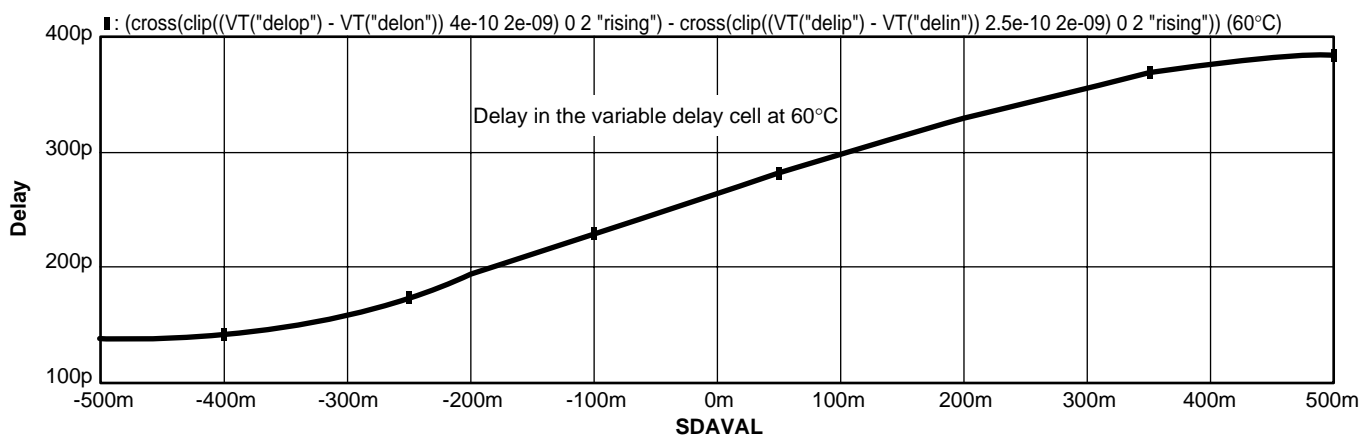


Note: The variation of the delay as a function of temperature is insignificant.

**TSEV83102G0B - Evaluation Board User Guide**

**4.12    Test Bench Description**

*Figure 4-8.* Differential Analog and Clock Input Configuration
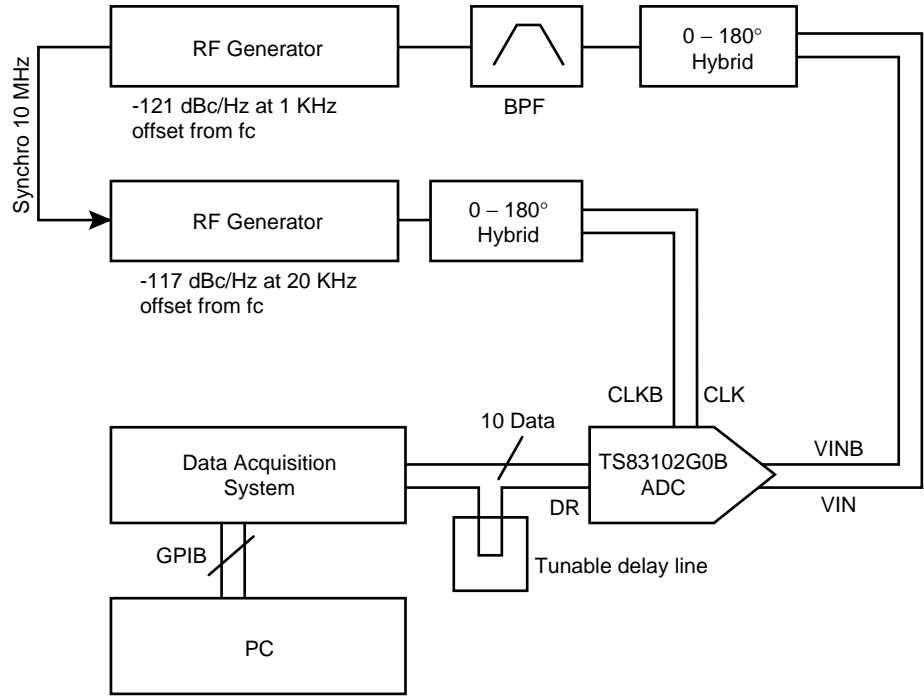


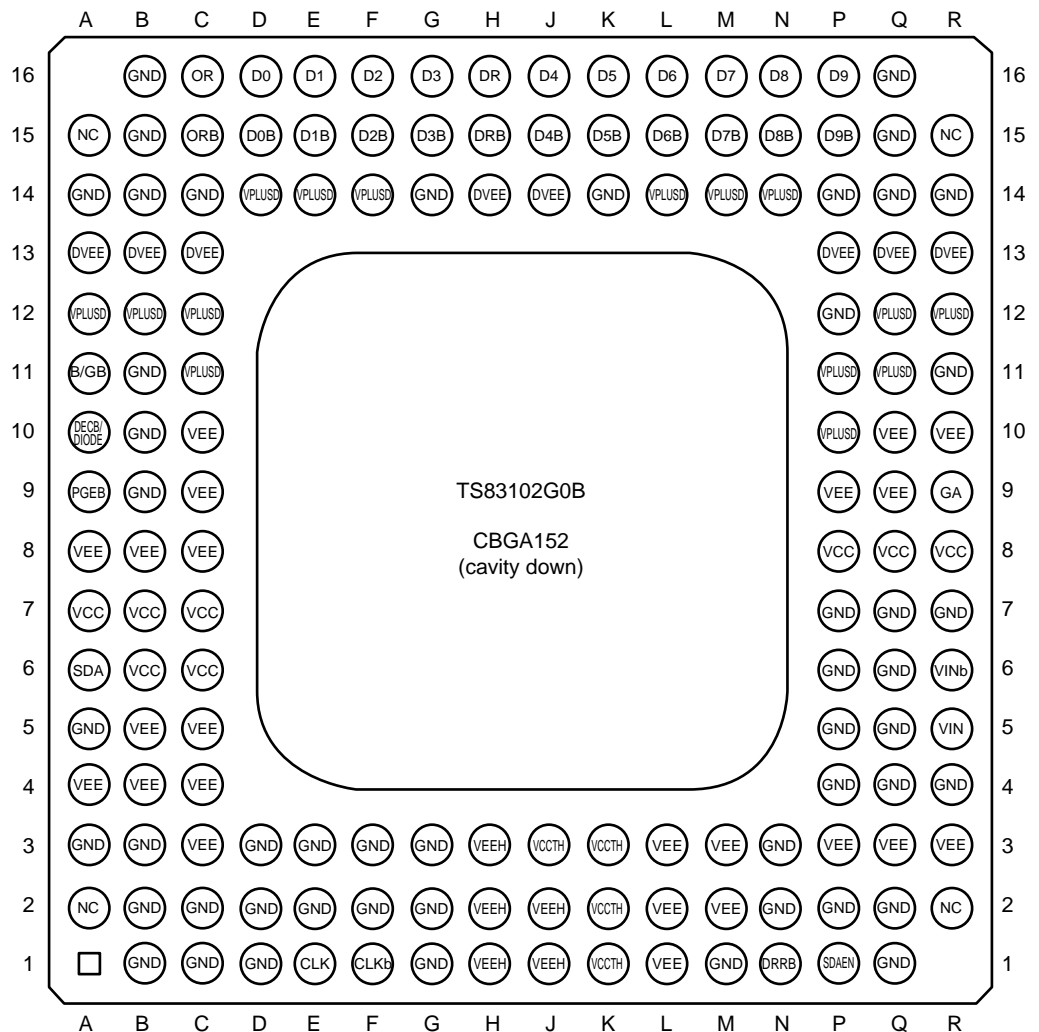*Figure 4-9.* Single-ended Analog and Clock Input Configuration

**TSEV83102G0B - Evaluation Board User Guide**
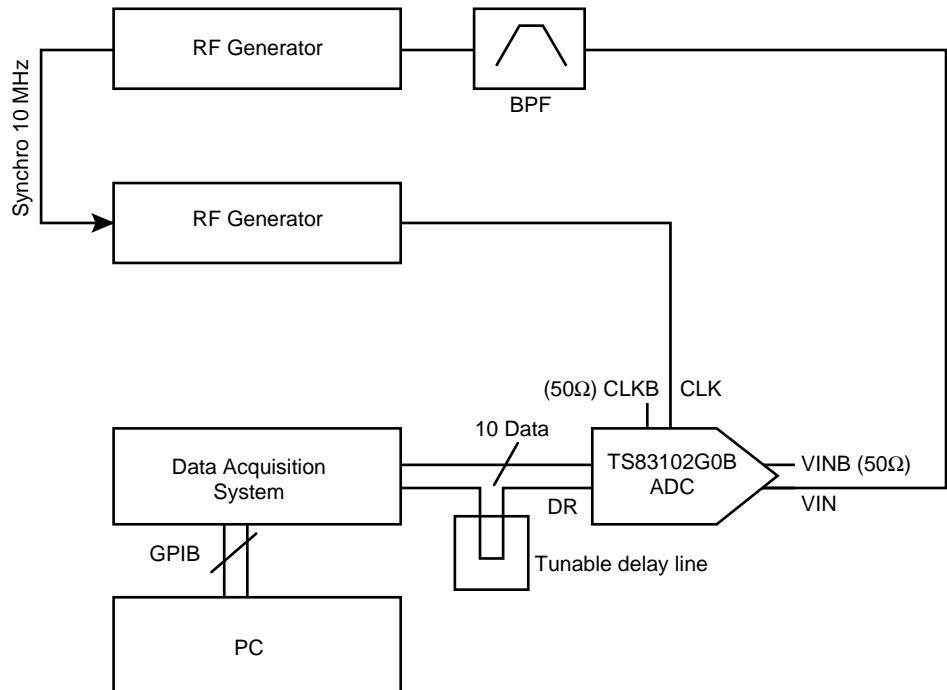
# Section 5

# Package Description

**5.1 TS83102G0B Pinout**

*Figure 5-1.* TS83102G0B Pinout of CBGA152 Package



Note: If required, four NC balls can be electrically connected to GND to simplify PCB routing.

*Table 5-1.* TSEV83102G0B Pin Description

| Symbol | Pin Number | Function |
|---|---|---|
| **Power Supplies** | | |
| $V_{CC}$ | K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8 | +5V analog supply |
| GND | B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16 | Analog ground |
| $V_{EE}$ | H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10 | -5V analog supply |
| $V_{PLUSD}$ | P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14 | Digital positive supply |
| $DV_{EE}$ | A13, B13, C13, P13, Q13, R13, H14, J14 | -5V digital supply |
| **Analog Inputs** | | |
| $V_{IN}$ | R5 | In-phase (+) analog input signal of the differential sample and hold preamplifier |
| $V_{INB}$ | R6 | Inverted phase (-) analog input signal of the differential sample and hold preamplifier |
| **Clock Inputs** | | |
| CLK | E1 | In-phase (+) clock input |
| CLKB | F1 | Inverted phase (-) clock input |
| **Digital outputs** | | |
| D0, D1, D2, D3, D4, D5, D6, D7, D8, D9 | D16, E16, F16, G16, J16, K16, L16, M16, N16, P16 | In-phase (+) digital outputs<br>D0 is the LSB. D9 is the MSB |
| D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B | D15, E15, F15, G15, J15, K15, L15, M15, N15, P15 | Inverted phase (-) digital outputs |
| OR | C16 | In-phase (+) Out-of-Range output |
| ORB | C15 | Inverted phase (-) Out-of-Range output |
| DR | H16 | In-phase (+) Data Ready Signal output |
| DRB | H15 | Inverted phase (-) Data Ready Signal output |
| **Additional Functions** | | |
| B/GB | A11 | Binary or Gray select output format control<br>- Binary output format if B/GB is floating or connected to GND<br>- Gray output format if B/GB is driven with ECL low level or B/GB is connected to $V_{EE}$ |

***Table 5-1.*** TSEV83102G0B Pin Description (Continued)

| Symbol | Pin Number | Function |
|---|---|---|
| DIODE | A10 | Decimation function enable or die junction temperature monitoring:<br>- Decimation active when LOW (die junction temperature monitoring NOT possible)<br>- Normal mode when HIGH or left floating<br>- Die junction temperature monitoring when current is applied |
| PGEB | A9 | Active low pattern generator enable<br>- Digitized input delivered at outputs according to B/GB if PGEB is floating or connected to GND<br>- Checkerboard pattern delivered at outputs if PGEB is driven with ECL low level or connected to $V_{EE}$ |
| DRRB | N1 | Asynchronous Data Ready Reset function |
| GA | R9 | Gain Adjust |
| SDA | A6 | Sampling delay adjust |
| SDAEN | P1 | Sampling delay adjust enable:<br>- inactive if floating or connected to GND<br>- active if ECL low or connected to $V_{EE}$ |

## 5.2 Thermal Characteristics

### 5.2.1 Thermal Resistance from Junction to Ambient: Rthja

Table 5-2 lists the converter's thermal performance parameters of the device itself, with no external heatsink added.

***Table 5-2.*** Thermal Resistance

| Air Flow (m/s) | Estimated ja Thermal Resistance ($^\circ$ C/W) | |
|---|---|---|
| 0 | 45 | ***Figure 5-2.*** Thermal Resistance from Junction to Ambient: Rthja |
| 0.5 | 35.8 | |
| 1 | 30.8 |  |
| 1.5 | 27.4 | |
| 2 | 24.9 | |
| 2.5 | 23 | |
| 3 | 21.5 | |
| 4 | 19.3 | |
| 5 | 17.7 | |
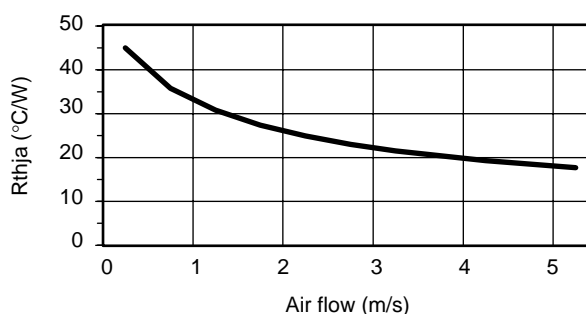
**5.2.2**   **Thermal Resistance from Junction to Case: Rthjc**

Maximum thermal Junction to Case resistance is 4.0° C/Watt.

This value does not include thermal contact resistance between the package and external heatsink (glue, paste, or thermal foil interface for example).

As an example, we can take 2.0° C/W for 50 µm thickness of thermal grease.

**5.2.3**   **Heatsink**

It is recommended to use a 50 mm x 50 mm x 30 mm heatsink (respectively L x l x H) in case of natural convection cooling mode (with no air flow).

A fan heatsink or direct conduction cooling is recommended, due to high power dissipation (4.7W).

A method should be chosen for cooling that allows less than 4.0° C/W for the case to ambient thermal resistance (Rthca).

The thermal resistance of the board is a high value (within a range of 30° C/W); thus an external heatsink is mandatory.

The heatsink must be fixed to the heatspreader which is at -5V. So the heatsink needs to be electrically isolated; using adequate low Rth electrical isolation.

Example: 4.0° C/W Rthca (case to ambient) +2.0° C/W thermal grease resistance +4.0° C/W Rthjc = 10.0° C/W total (Rthja).

The heatsink should make contact with the package on the side opposite to the balls, in a 8.5 mm diameter circle:

*Figure 5-3.* CBGA152 Board Assembly
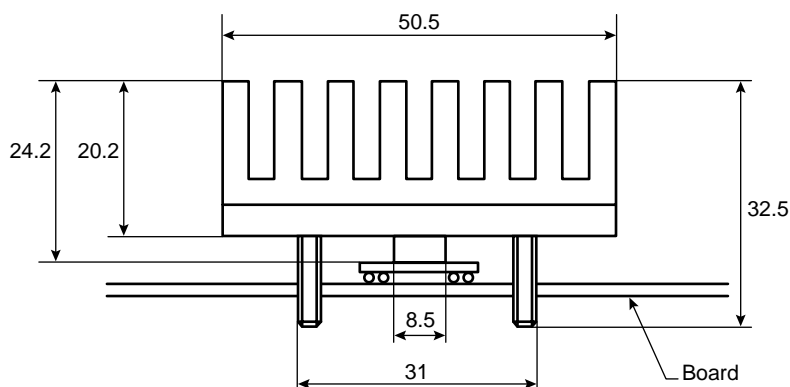


Note: The measures are given in mm.

Cooling system efficiency can be monitored using the Temperature Sensing Diodes, integrated in the device.

## 5.3    Ordering Information

| Part Number | Package | Temperature Range | Screening Level | Comments |
|---|---|---|---|---|
| JTSX83102G0-1V1B | Die | Ambient | Prototype | ON REQUEST ONLY (Please contact Marketing) |
| TSX83102G0BGL | CBGA 152 | Ambient | Prototype | Prototype Version |
| TS83102G0BCGL | CBGA 152 | "C" grade: $0^\circ C < T_C; T_J < 90^\circ C$ | Standard | |
| TS83102G0BVGL | CBGA 152 | "V" grade: $-20^\circ C < T_C; T_J < 110^\circ C$ | Standard | |
| TSEV83102G0BGL | CBGA 152 | Ambient | Prototype | Evaluation Board (delivered with heatsink) |

**TSEV83102G0B - Evaluation Board User Guide**

# Section 6

# Schematics

## 6.1 TSEV83102G0B Electrical Schematic

Figures 6-2 to Figures 6-8 shows the electrical schematic of the TSEV83102G0B.

The pinout used for the evaluation board has been translated from Atmel's pinout (refer to page 5-1) to the JEDEC standard shown in Figure 6-1. This explains the discrepancies between the pinout used on page 5-1 and the one given in the electrical schematic in Figure 6-2.
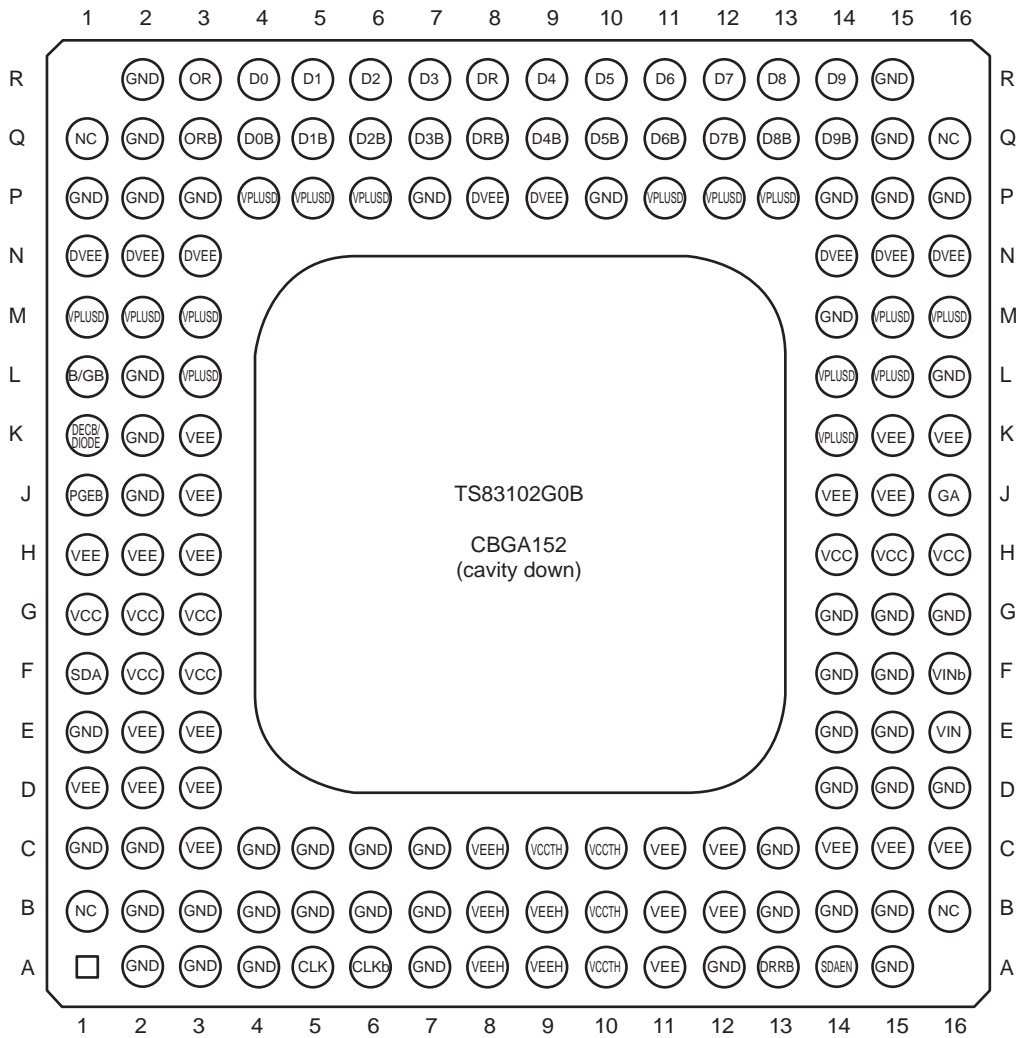
**Figure 6-1.** TS83102G0B pinout in JEDEC Standard

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | | GND | OR | D0 | D1 | D2 | D3 | DR | D4 | D5 | D6 | D7 | D8 | D9 | GND | | R |
| Q | NC | GND | ORB | D0B | D1B | D2B | D3B | DRB | D4B | D5B | D6B | D7B | D8B | D9B | GND | NC | Q |
| P | GND | GND | GND | VPLUSD | VPLUSD | VPLUSD | GND | DVEE | DVEE | GND | VPLUSD | VPLUSD | VPLUSD | GND | GND | GND | P |
| N | DVEE | DVEE | DVEE | | | | | | | | | | | DVEE | DVEE | DVEE | N |
| M | VPLUSD | VPLUSD | VPLUSD | | | | | | | | | | | GND | VPLUSD | VPLUSD | M |
| L | B/GB | GND | VPLUSD | | | | | | | | | | | VPLUSD | VPLUSD | GND | L |
| K | DECB/DIODE | GND | VEE | | | | | | | | | | | VPLUSD | VEE | VEE | K |
| J | PGEB | GND | VEE | | | | | TS83102G0B | | | | | | VEE | VEE | GA | J |
| H | VEE | VEE | VEE | | | | | CBGA152 | | | | | | VCC | VCC | VCC | H |
| G | VCC | VCC | VCC | | | | | (cavity down) | | | | | | GND | GND | GND | G |
| F | SDA | VCC | VCC | | | | | | | | | | | GND | GND | VINb | F |
| E | GND | VEE | VEE | | | | | | | | | | | GND | GND | VIN | E |
| D | VEE | VEE | VEE | | | | | | | | | | | GND | GND | GND | D |
| C | GND | GND | VEE | GND | GND | GND | GND | VEEH | VCCTH | VCCTH | VEE | VEE | GND | VEE | VEE | VEE | C |
| B | NC | GND | GND | GND | GND | GND | GND | VEEH | VEEH | VCCTH | VEE | VEE | GND | GND | GND | NC | B |
| A | □ | GND | GND | GND | CLK | CLKb | GND | VEEH | VEEH | VCCTH | VEE | GND | DRRB | SDAEN | GND | | A |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

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**Figure 6-2.** TSEV83102G0B Electrical Schematic
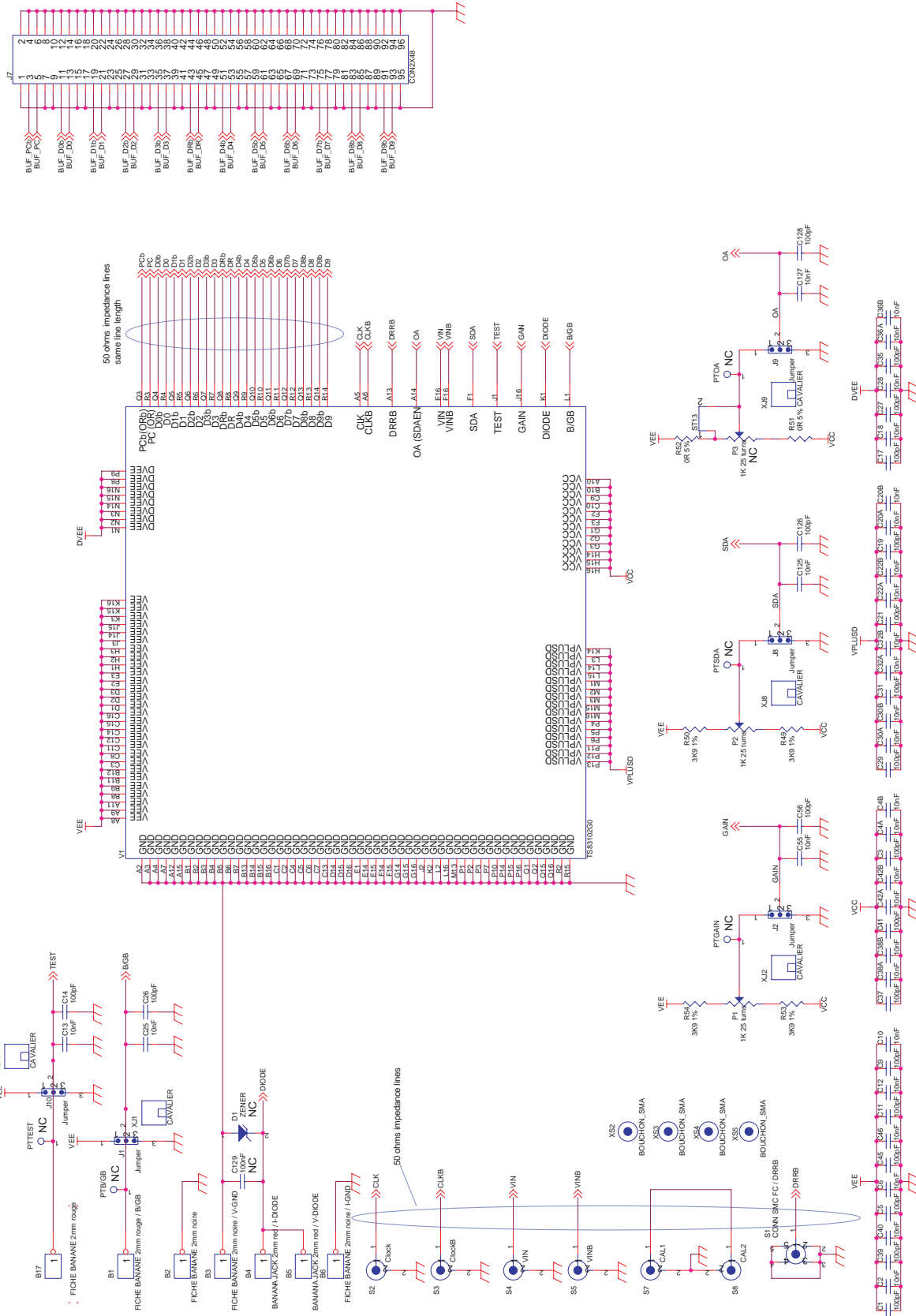
***Figure 6-3.*** Component Side Description



***Figure 6-4.*** Metal Layer 2 and 4: Ground Planes



***Figure 6-5.*** Metal Layer 3 and 3 bis: Power Supplies and Ground Planes



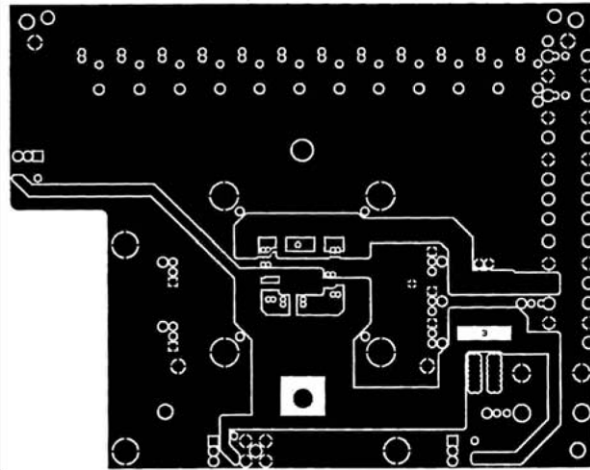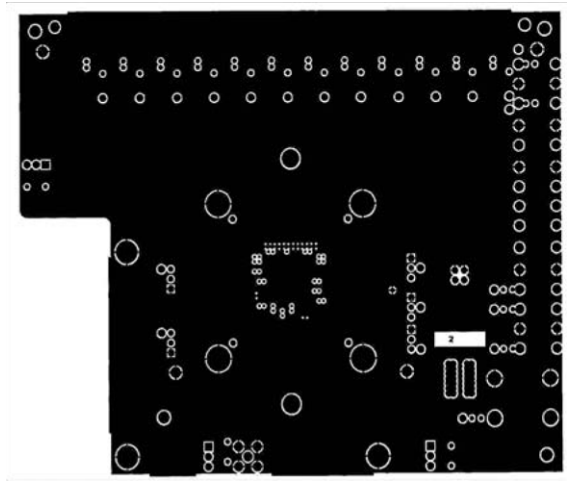***Figure 6-6.*** Metal Layer 5: Solder Side



***Figure 6-7.*** TSEV83102G0B Evaluation Board: Top View (Signal Side) without Heatsink
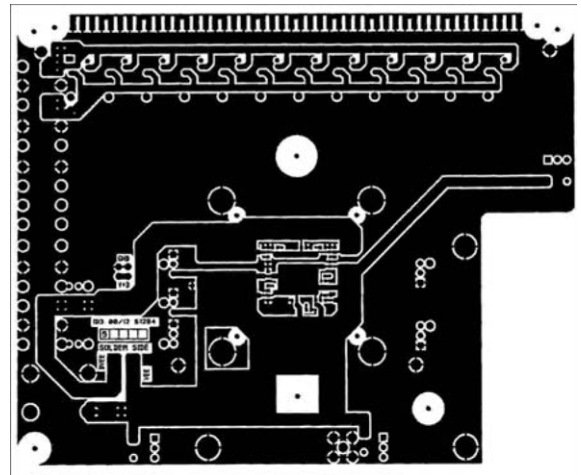


***Figure 6-8.*** TSEV83102G0B Evaluation Board: Bottom View
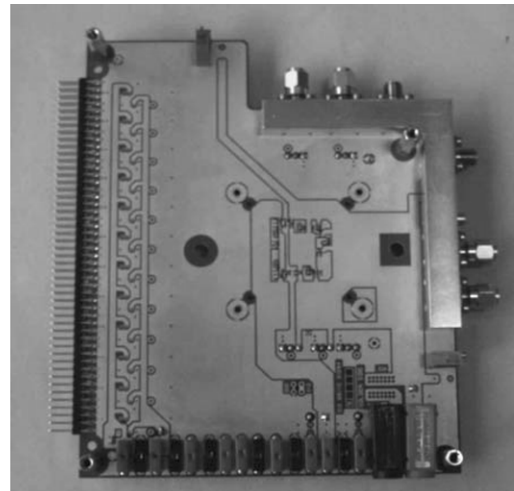
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