# Operating Atmel TS81102G0 DMUX at 2 GHz

## 1. Introduction

This application note aims at providing recommendations to help you operate Atmel TS81102G0 8-/10-bit 1:4/8 2 GHz DMUX in TBGA240 package at 2 GHz, especially when used with Atmel TS83102G0B 10-bit 2 Gsps ADC.

## 2. Operating Atmel TS81102G0 DMUX at 2 GHz: Status

### 2.1 Operation with Atmel ADCs: DMUXDelAdjust

The TS81102G0 DMUX device is used with Atmel ADCs in order to reduce the output speed of the ADC to rates which can be easily processed by standard FPGAs. Because the data and clock paths are not aligned inside the DMUX, you must adjust the delay between the data and clock lines by the means of the DMUXDelAdjust cell.

The principle of operation of this delay cell (implemented on the DMUX input clock path) is described in Figure 2-1.

The two first lines of the timing diagram represent the ADC output data and ADC output clock (Data Ready signal). It is assumed that the clock and data are properly aligned at the output of the ADC, i.e. the clock edges are perfectly centered on the data.

At the DMUX input, the data and clock signals thus arrive correctly aligned but because of different delay paths within the input circuitry of the DMUX, the DMUX internal data and clock signals are not aligned any longer and the synchronization between the clock and the data may be lost within the DMUX. The DMUXDelAdjust function has to be used to compensate for this delay. This is illustrated at the bottom of Figure 2-1.

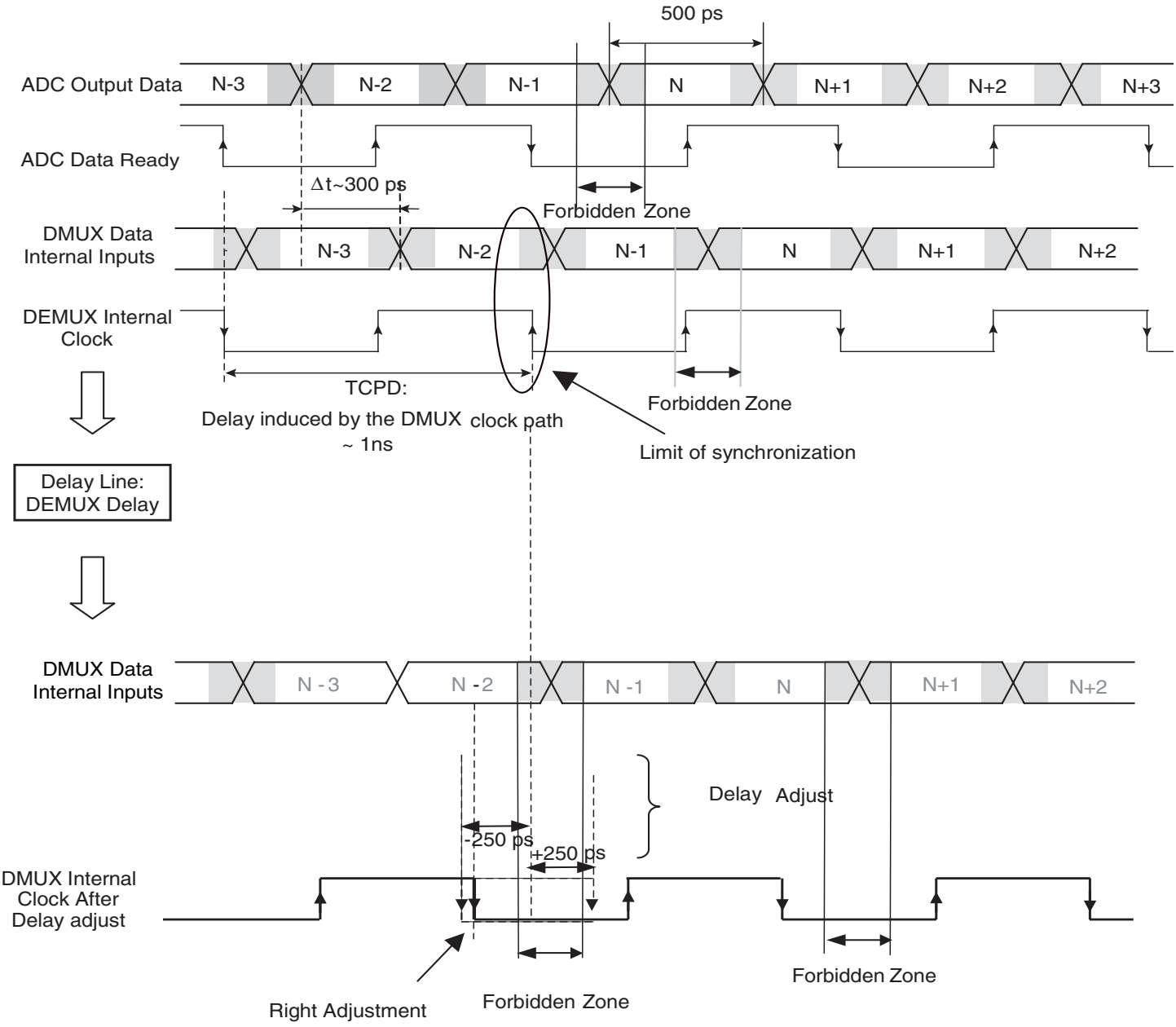
Thanks to the DMUXDelAdjust, you can ensure that the input clock and input data of the DMUX are internally aligned and guarantee that there is no data loss inside the DMUX.

**TS81102G0 DMUX 2 GHz Operation**

**Application Note**

5427A–BDC–01/05

**Figure 2-1.** TS81102G0 DMUXDelAjust Function Principle of Operation

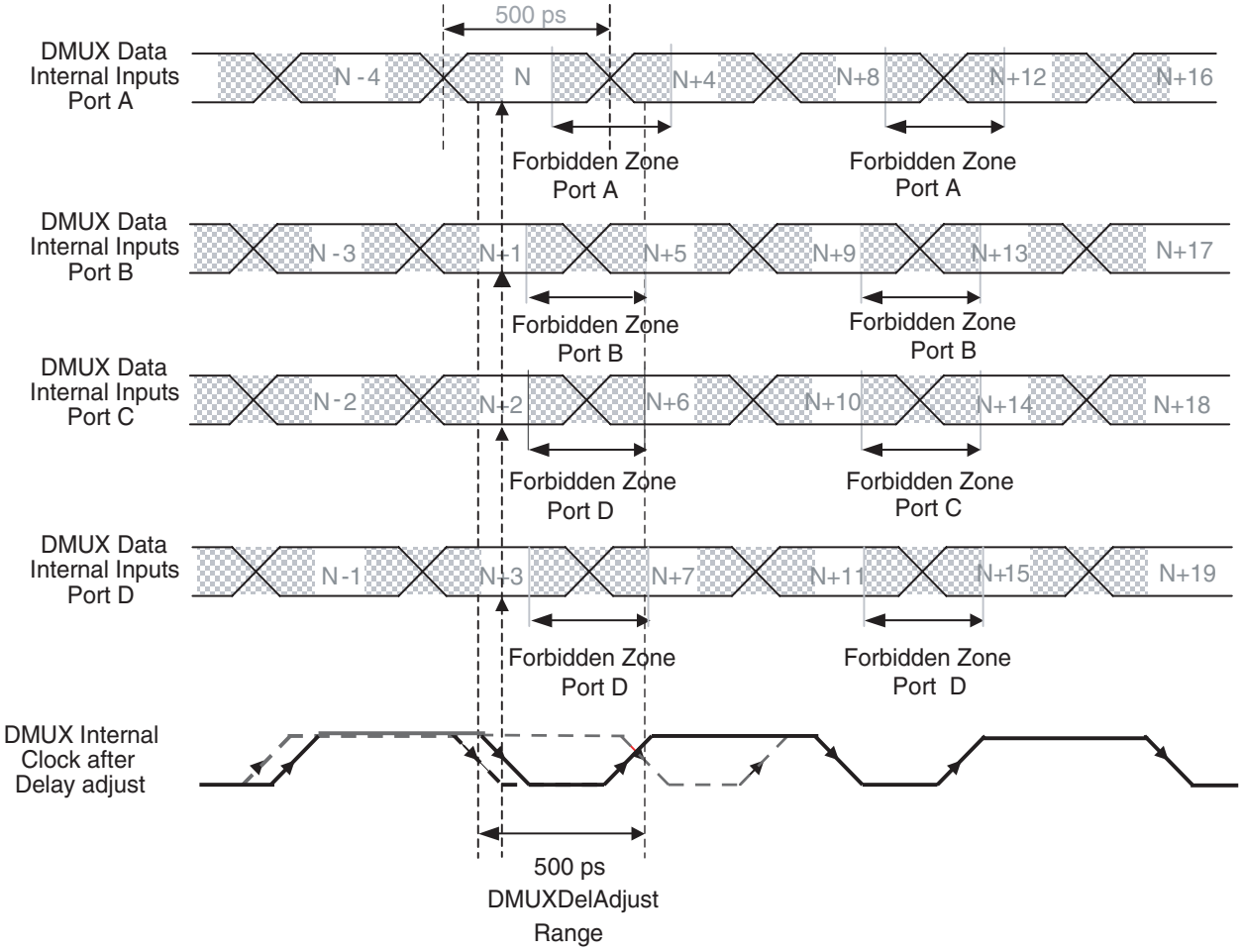


At full input speed, i.e. 2 GHz data rate (1 GHz DMUX input clock rate), it might be difficult to tune the DMUXDelAdjust to the “right” setting (because of the layout and signal integrity). This is due to the fact that the range may not be sufficient to compensate for the input clock signal internal distortion at such speeds.

As a matter of fact, at high frequencies (usually above 1.9 GHz), the clock signal might be internally distorted at the DMUX input thus leading to a distortion of the clock duty cycle and generating data loss, especially on port A, for which the phenomenon is stressed by the internal routing (die and TBGA 240 package).

Figure 2-2 illustrates this phenomenon by highlighting the fact that because of the rise and fall times, the distortion of the clock duty cycle and the delay between port A and the other ports. It might be possible to find the right setting for the DMUXDelAdjust for all ports except for port A.

**Figure 2-2.** TS81102G0 DMUXDelAdjust Limit of Operation at Full Speed




If you intend to run the TS81102G0 DMUX in TBGA 240 package at 2 GHz or if you already have a design at 2 GHz with this DMUX and experience the above issue on port A, the following section provides recommendations and potential solutions which will help you ensure that the DMUX will work at this rate, without loss of data or data errors.

# 3. Operating Atmel TS81102G0 DMUX at 2 GHz: Recommendations

## 3.1 Board Layout Recommendations

There are common rules for layout of HF systems, such as the following:

- avoid traces with angles or too many patterns (to avoid crosstalk between traces)
- keep all traces matched to 50 Ω
- have the same length for traces corresponding to signals of the same function (clock, analog in, analog out, data in, data out…)
- avoid through hole vias for signal traces
- for differential signals, keep the True and False signal traces close to one another
- for single-ended signals, make sure that all signals are far enough from their neighbor to avoid crosstalk

In the case of the TS81102G0, the matching of the line length of the data and data ready signals from the ADC is very critical in the board design. All lines should indeed be matched to within 2 mm and the two lines of a differential pair should be matched to within 1 mm of each other.

Figure 3-1 and Figure 3-2 show the recommended board layout, as used for Atmel Converter evaluation boards.

**Figure 3-1.** 50Ω Matched Line on R04003 Layout (single-ended signal)

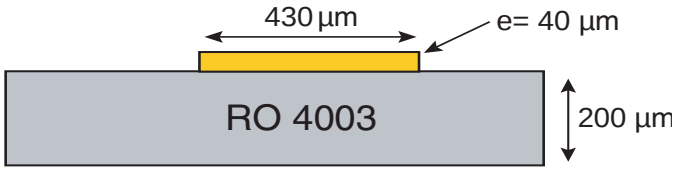
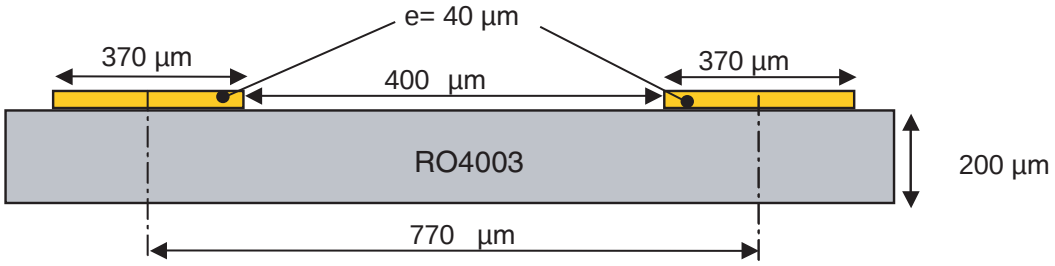


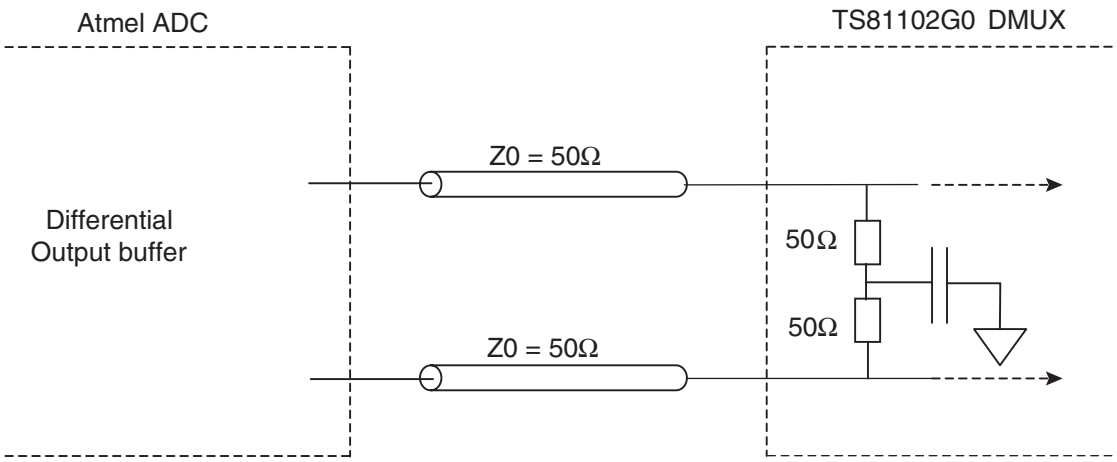

**Figure 3-2.** 50Ω Matched Line on R04003 Layout (differential signal)



## 3.2 Connection to Atmel ADCs

The TS81102G0 data and clock input buffers are internally 2 x 50Ω to ground via 40 pF capacitor terminated. It is thus not necessary to terminate the ADC outputs externally, as described on Figure 3-3.

**Figure 3-3.** Atmel ADC and TS81102G0 DMUX Interfacing




## 3.3 Compensating for the Clock Duty Cycle Distortion

At 2 GHz, the issue comes from the distortion of the clock signal inside the DMUX leading to a distortion of the duty cycle of the input clock and affecting the timings between the clock and the data.

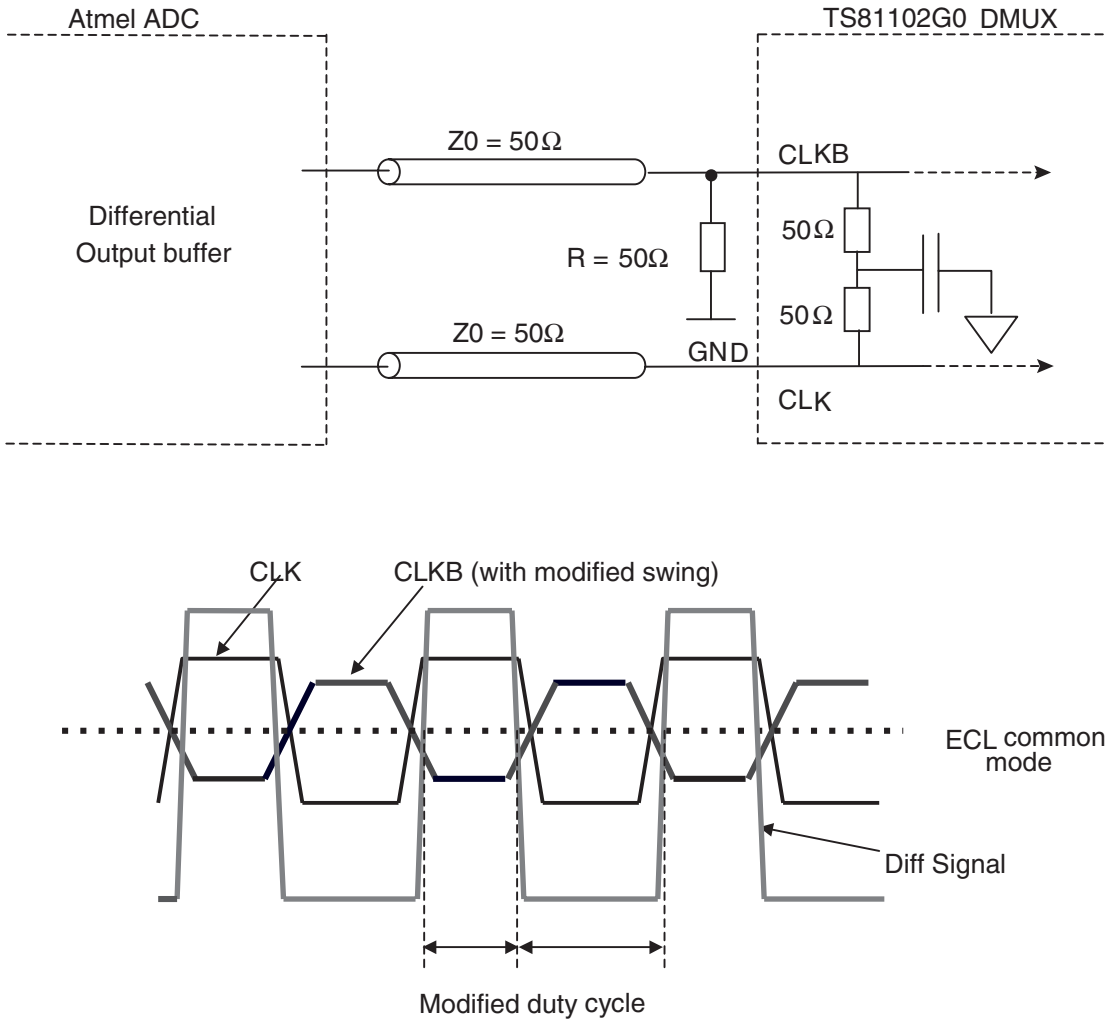
Three solutions can be explored to modify the DMUX input clock duty cycle:

- Unbalance the two signals from the differential data ready pair at the ADC output
- Add a capacitor on CLK
- Add an inductor on CLKB

## 3.4 Proposed Solution 1: Unbalancing DR/DRb from the ADC

This first proposition requires to be able to place pull-up resistors at the ADC output to unbalance the Data Ready signal pair in order to change its initial 50-50 duty cycle. The correct final duty cycle depends on the board layout, signal integrity and environment, this is why we cannot quantify exactly by which amount the duty cycle should be changed to, nevertheless, it is understood that the trend is towards a 40% High and 60% Low duty cycle.

**Figure 3-4.** Unbalancing the Data Ready Differential Pair from the ADC

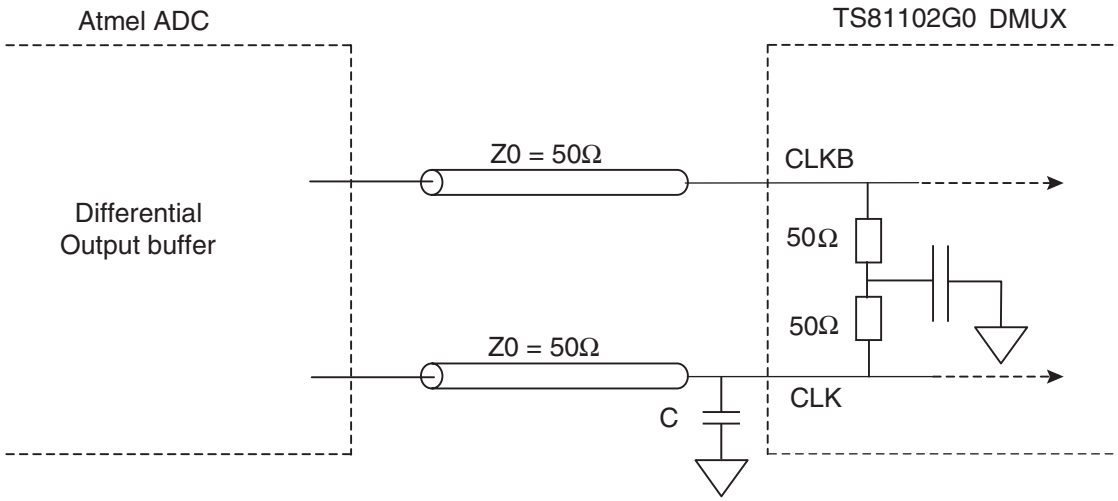



Note: It is very important that the resistor R = 50Ω is placed close to the DMUX at the end of the line from the ADC.

## 3.5 Proposed Solution 2: Add a Capacitor on CLK

In this solution, the aim is to modify the input clock duty cycle of the DMUX by adding a capacitor on the CLK signal of the differential pair. This solution allows to increase the range of the DMUXDelAdjust for which the DMUX works properly at 2 GHz. However, with this solution, this range is still narrow and depending on the location of the capacitor and the way the board was laid out, it may not be adequate for proper operation.

**Figure 3-5.** Adding a Capacitor on CLK

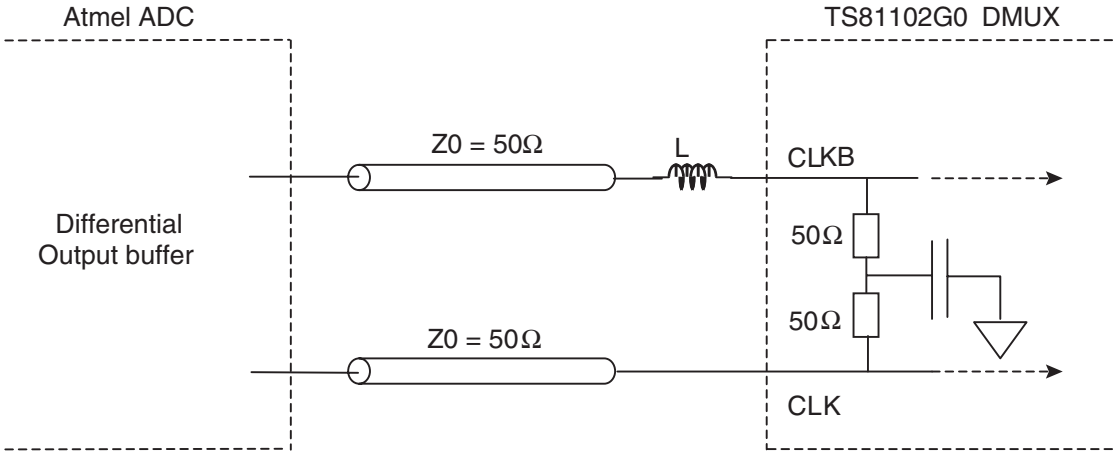



Note: On the TSEV81102G0TPZR3 evaluation board, the optimum for operation at 2 GHz was found with C = 20 pF.

## 3.6 Proposed Solution 3: Add an Inductor on CLKB

In this solution, the aim is to modify the input clock duty cycle of the DMUX by adding an inductor on the CLKB signal of the differential pair. This solution is acceptable when a specific, high speed operation at 2 GHz (±50 MHz) is required (i.e.. With this solution, it is possible that the performances of the DMUX decreases significantly below and above 2 GHz ±50 MHz).

**Figure 3-6.** Adding an inductor on CLKB




On the TSEV81102G0TPZR3 evaluation board, the optimum for operation at 2 GHz was found with L = 8.2 nH.

**From our experience, the recommended solution is solution 1.**

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