Application Note

Replacing e2v's TS81102G0 DMUX with e2v's AT84CS001 LVDS DMUX

1. Introduction

With the increasing demand for low-power devices, e2v is introducing a new demultiplexer intended as a companion chip for its high-speed ADCs (TS8388B 8-bit 1 Gsps, TS83102G0B 10-bit 2 Gsps and AT84AS008 10-bit 2.2 Gsps ADCs).

The AT84CS001 is a low-power 10-bit 1:2 or 1:4 2.2 GHz DMUX with LVDS format I/Os for easy interfacing with high-speed FPGAs.

This new DMUX has only minor differences with the TS81102G0 8 or 10-bit 2 GHz 1:4/8 DMUX in terms of I/O access and location, while offering LVDS compatibility and numerous functional improvements.

This document highlights the hardware-related differences between the TS81102G0 and the AT84CS001.

2. Main Differences Between TS81102G0 and AT84CS001 DMUX Devices

The TS81102G0 and AT84CS001 are demultiplexers for use as companion chips with e2v's high-speed ADCs.

Table 2-1 on page 2 highlights the main differences between the two devices.

Table 2-1. Differences between TS81102G0 and AT84CS001 Devices

Parameter	TS81102G0	AT84CS001
Data format	Selectable 8 or 10-bit	10-bit with additional 11th bit
Ratio	1:4 or 1:8	1:2 or 1:4
Maximum frequency	2 GHz	2.2 GHz
Power supplies	5V, –5V, V_{PLUSD} (0 to 3.3V)	3.3V, 2.5V
I/O compatibilities	ECL/PECL/TTL/SSTL2	LVDS
Output mode	Simultaneous	Simultaneous or staggered
Input rate mode	Single or double data rate (DR or DR/2)	Single or double data rate (DR or DR/2)
Output rate mode	Single data rate (DR)	Single or double data rate (DR or DR/2)
Power dissipation	4 to 9W	2.6W
Reset	Asynchronous and synchronous resets	Asynchronous reset only
Functions:		
Clock delay adjust	Yes	Yes
Standalone delay cell	Yes	Yes
Swing adjust	Yes	No
Sleep mode	No	Yes
Built-in Test	Yes	Yes
Temperature diode	Yes	Yes
Available package	TBGA 240 CQFP 196	EBGA 240

3. New Functions of the AT84CS001

In addition to improvements made on the AT84CS001 to minimize its power consumption compared to the TS81102G0, and to simplify interfacing with high-speed FPGAs – in particular thanks to its fully-differential LVDS output compatibility – the AT84CS001 benefits from numerous new functions, including:

- A selectable output clock mode (single or double rate)
- A sleep mode, allowing you to reduce the device's power consumption by 60%
- A staggered mode, providing you with simultaneous or staggered data at the device's output
- An additional 11th bit, which can be used to process the ADC's out-of-range bit
- A reset, only one of which is necessary with the AT84CS001 (asynchronous reset)

These functions are described in the following sections.

3.1 Selectable Output Clock Mode

There are two selectable modes for the type of output clock:

- DR mode: only the output clock's rising edge is active and the output clock rate is the same as the output data rate
- DR/2 mode: both the output clock's rising and falling edges are active and the output clock rate is half the output data rate.

These modes are illustrated in Figure 3-1 and Figure 3-2.

Figure 3-1. DR Mode

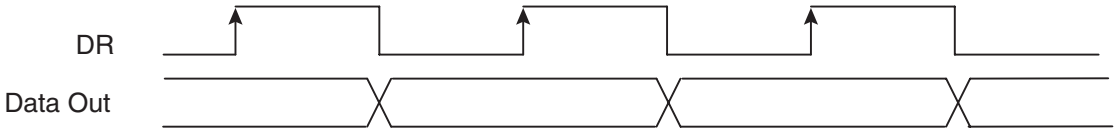


Figure 3-2. DR/2 Mode

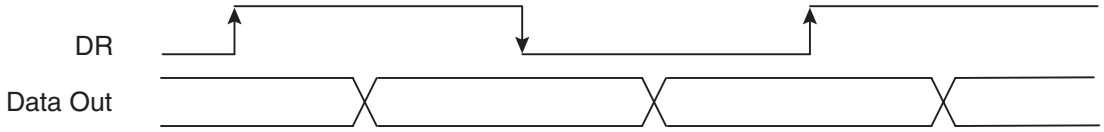


Table 3-1. DMUX Output Clock Type Selection Settings

DRTYPE	DMUX Output Clock Type
1	DR
0	DR/2

Note: When DRTYPE is left floating, the default mode is DR/2.

3.2 Sleep Mode

The sleep mode reduces the power consumption of the AT84CS001 DMUX by 60%. It is active when the sleep bit = “0”, is connected to 10Ω to ground, or to ground. In this mode, the output data of the DMUX is frozen to a known state (either low or high).

When this signal is left floating, the device operates in normal mode.

3.3 Staggered Mode

Two output modes are provided:

- Staggered, where the data packets are output one after the other. This mode is activated through the STAGG signal (active at low level when = “0”). When STAGG is left floating, the simultaneous mode is activated.
- Simultaneous, where all data packets are output at the same time (default mode).

Figure 3-3. Simultaneous Mode

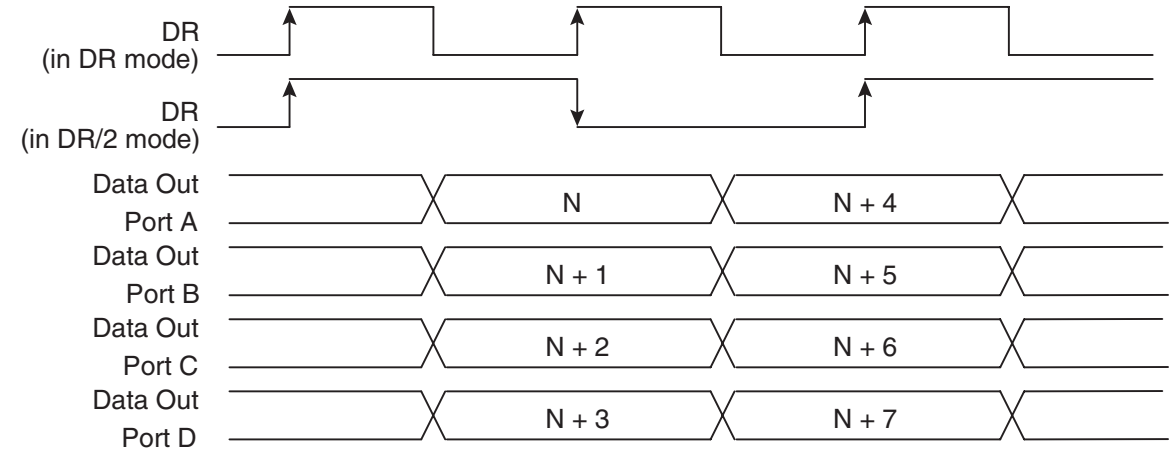


Figure 3-4. Staggered Mode (1:2 Ratio)

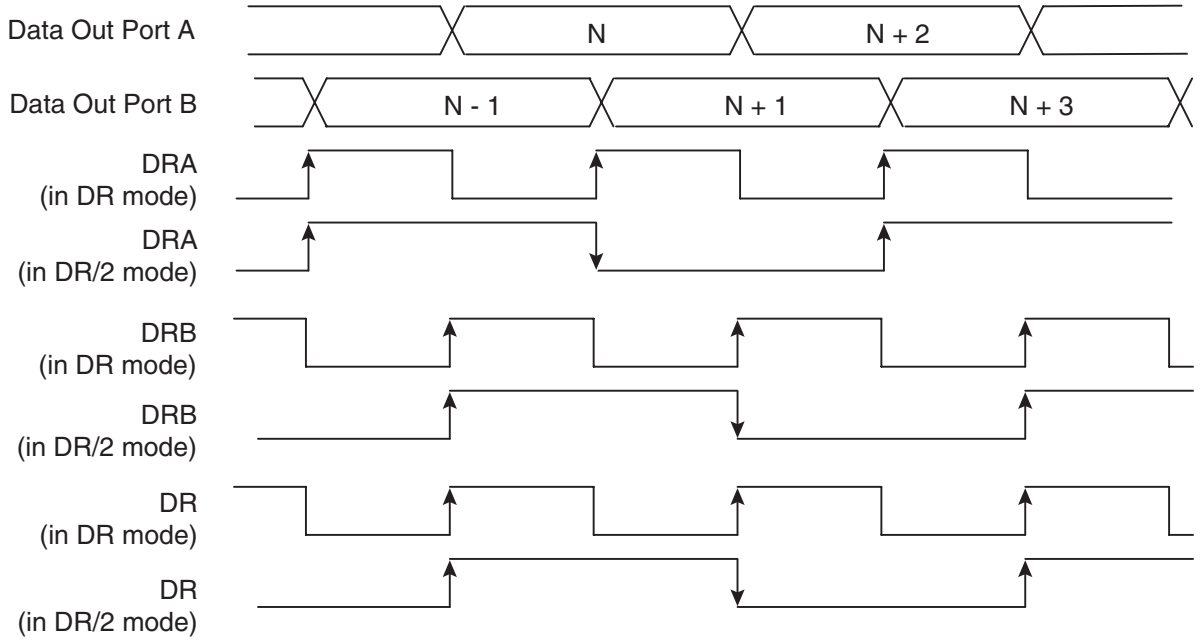
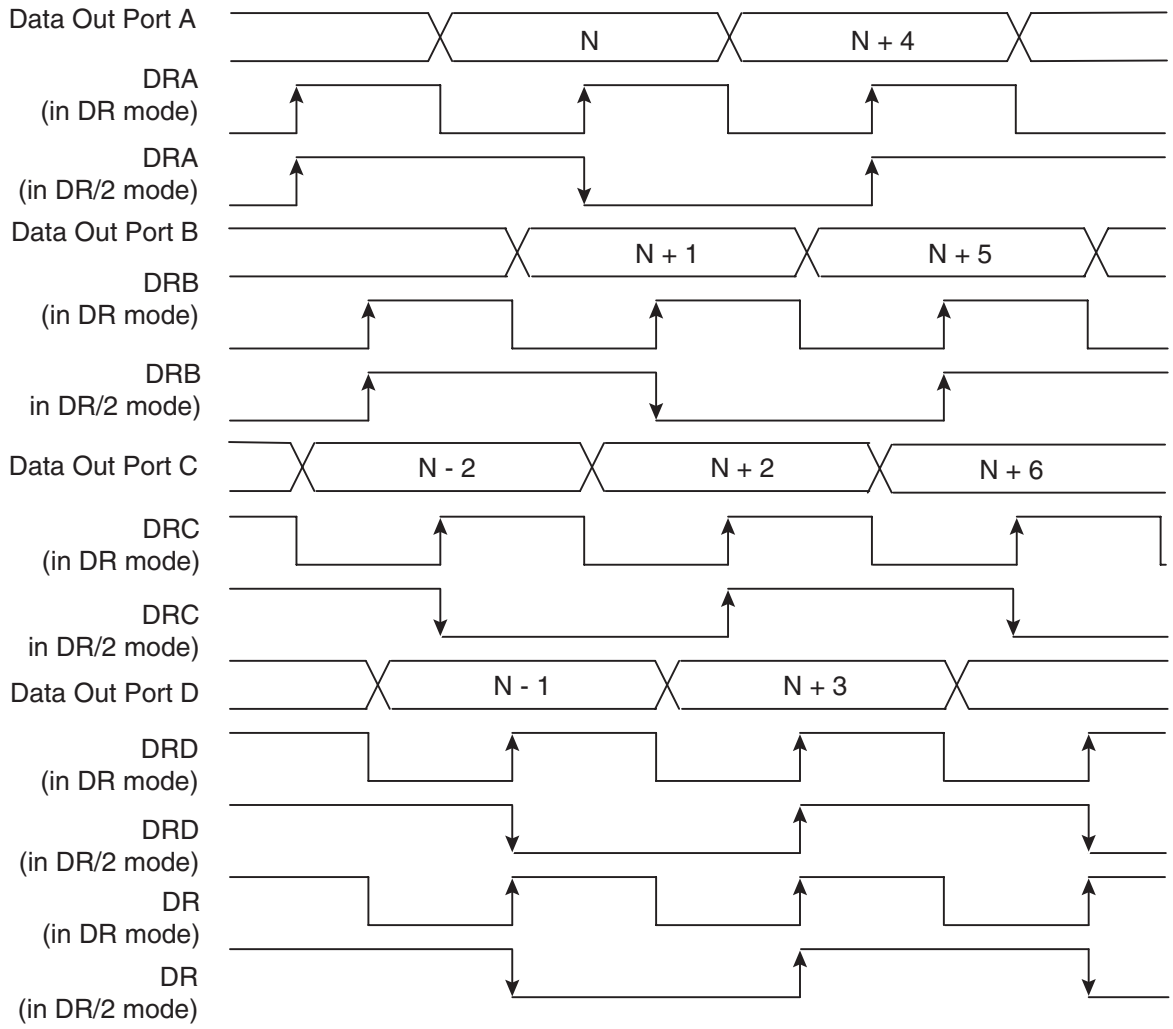


Figure 3-5. Staggered Mode (1:4 Ratio)



3.4 Additional Bit

When a signal is applied on IOR and IORN, the *additional bit* is activated. It can be used to process the out-of-range bit from the ADC and plays the role of the 11th bit in the case of a 10-bit stream.

In 1:2 ratio, AOR, DRAN and BOR, DRBN output this signal at half its initial speed (IOR, IORN is demultiplexed by the DMUX ratio).

In 1:4 ratio, AOR, DRAN, BOR, DRBN, COR, DRCN and DOR, DRDN output this signal at a quarter of its initial speed.

In staggered output mode, AOR, DRAN, BOR, DRBN, COR, DRCN and DOR, DRDN output a Data Ready signal for each port, centered on the corresponding data, in which case the additional bit is disabled.

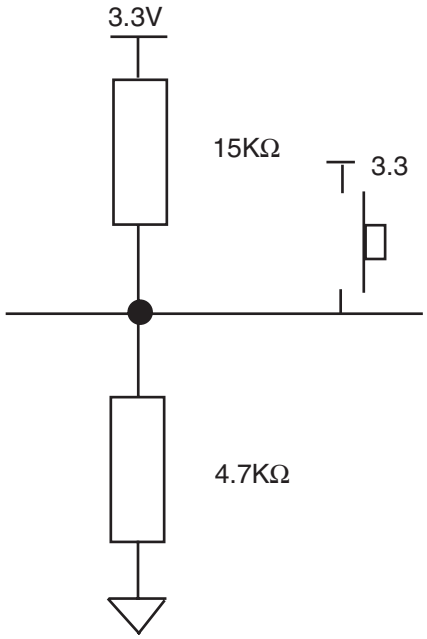
3.5 Reset

With regard to the AT84CS001 DMUX, only one master reset – the asynchronous reset – is available and necessary. This reset is required to start the device and acts as master reset of the DMUX.

The AT84CS001 does not require any synchronous reset. In the case of multichannel operation, synchronization of all ADCs and DMUXes is guaranteed by resetting both the ADC and the DMUX.

The asynchronous reset is active on high level (3.3V). When the ASYNCRST signal is grounded the device is not in reset state.

Figure 3-6. Possible Implementation of Asynchronous Reset



During an asynchronous reset, the input clock of the DMUX must be stopped at low level in order to satisfy timing constraints (this condition is met when e2v's single ADCs are in reset, in which case the Data Ready signal is held low).

The ASYNCRST signal frequency should be 200 MHz maximum.

Note: When the functions (RSTYPE, STAGG, BIST) change, we must apply an ASYNCRST signal to start out with the appropriate configuration.

4. Electrical Characteristics

The TS81102G0 was designed using a high-speed bipolar process requiring –5V and 5V power supplies whereas the AT84CS001 was designed using a 3.3V BiCMOS process. This difference has many implications on both devices in terms of electrical characteristics.

The following table focuses on changes in the signal electrical levels when migrating from one device to the other.

Table 4-1. Signal Electrical Levels

Type	TS81102G0		AT84CS001		Description
	Name	**Level**	**Name**	**Level**	
Digital inputs	I0/I0b…I9/I9b	Differential ECL	I0/I0N…I9/I9N	LVDS	Input data On-chip 100Ω differential termination
			IOR/IORN	LVDS	Additional input bit On-chip 100Ω differential termination
	CLK/CLKb	Differential ECL	CLK/CLKN	LVDS	Input clock On-chip 100Ω differential termination
Digital outputs	A0…A9 to H0…H9	Adjustable single logic	A0/A0N…A9/A9N to D0/D0N…D9/D9N	LVDS	Output data
	Ref A ... Ref B	Reference signal for each port	AOR/DRAN, AORN/DRA to DOR/DRDN, DORN/DRD	LVDS	Additional output bits or output clock in staggered mode
	DR/DRb	Adjustable differential logic	DR/DRN	LVDS	Output clock
Control signals	ClkInType	TTL	CLKTYPE	“1”: R = 10 kΩ “0”: R= 10Ω	Input clock mode
			DRTYPE	“1”: R = 10 kΩ “0”: R= 10Ω	Output clock mode
	NbBIT	TTL	(Suppressed)		Number of bit selection
			SLEEP	“1”: R = 10 kΩ “0”: R= 10Ω	Sleep mode
			STAGG	“1”: R = 10 kΩ “0”: R= 10Ω	Staggered mode
	RatioSel	TTL	RS	“1”: R = 10 kΩ “0”: R= 10Ω	Ratio selection
	BIST	TTL	BIST	“1”: R = 10 kΩ “0”: R= 10Ω	Built-in Self Test
	DIODE	Max: VDiode = 700 mV Idiode = 1 mA	DIODE	Max: VDiode = 700 mV Idiode = 1 mA	Die junction temperature monitoring
	SwiAdjust	0V ± 0.5V	(Suppressed)		Output buffers swing adjustment
Synchronization	AsynchReset	TTL	ASYNCRST	LVCMOS/CMOS	Asynchronous reset
	SynchReset/ SynchResetb	Differential ECL	(Suppressed)		Synchronous reset

Table 4-1. Signal Electrical Levels (Continued)

Type	TS81102G0		AT84CS001		Description
	DMUXDelAdjCtrl	0V ± 0.5V	CLKDACTRL	$V_{CCD}/3$ to $2V_{CCD}/3$	DMUX clock delay adjust
	ADCDelAdjCtrl	0V ± 0.5V	DACTRL	$V_{CCD}/3$ to $2V_{CCD}/3$	Standalone delay cell adjust
			DAEN	"1": R = 10 kΩ "0": R= 10Ω	Standalone delay cell adjust enable
	ADCDelAdjIn/ ADCDelAdjInb	Differential ECL	DAI/DAIN	LVDS	Stand-alone delay cell adjust input data
	ADCDelAdjOut/ ADCDelAdjOutb	Adjustable Differential logic	DAO/DAON	LVDS	Stand-alone delay cell adjust output data
Power supplies	GND	0V	DGND	0V	Common ground
	V_{EE}	–5V	(suppressed)		Digital negative supply
	V_{PLUSD}	0V to 3.3V	V_{PLUSD}	2.5V	Digital output supply
	V_{CC}	5V	V_{CCD}	3.3V	Digital positive supply
Package top side potential		–5V		Ground	

5. Hardware Implementation

5.1 Package Characteristics

The TS81102G0 is offered in both TBGA 240 and CQFP 196 packages in order to address all types of screening, from commercial to military and even space.

The AT84CS001 mainly addresses the commercial and industrial markets and is offered in an EBGA 240 package, which is quite similar to the TBGA 240.

5.1.1 Mechanical characteristics

The TBGA 240 and EBGA 240 packages have equivalent mechanical characteristics, permitting use of the same board footprint for both devices.

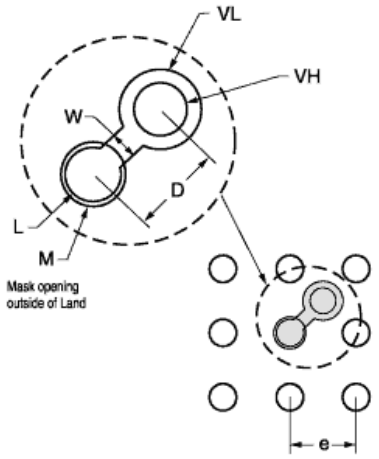
Table 5-1. Main Dimensions of TBGA 240 and EBGA 240 Packages (all Dimensions in Millimeters)

Parameter	TS81102G0			AT84CS001		
	Min	Typ	Max	Min	Typ	Max
Body size	24.80	25.00	25.20	24.80	25.00	25.20
Height (from bottom of balls to top of package)	1.30	1.50	1.70	1.25	1.45	1.60
Ball pitch	1.27	1.27			1.27	
Ball diameter	0.60	0.75	0.90	0.70	0.80	0.90

Table 5-2. Board Layout Recommendations

Description	Dimensions	e2v Standard	
		mm	mil
Component land pad diameter (pad)	–		
Solder land diameter	L	0.71	28
Diameter of opening in solder mask	M	0.71	28
Solder (ball) land pitch	e	1.27	50
Line width between via and land	W	0.51	20
Distance between via and land	D	0.71	28
Via land diameter	VL	0.66	26
Through hole diameter	VH	0.38	15

Figure 5-1. Board Layout



5.1.2 Electrical Characteristics

The electrical characteristics of the EBGA 240 are equivalent to those of the TBGA 240. The main advantage of the EBGA 240 is that it provides 4 layers for the power and ground planes, while the TBGA 240 only offers one layer.

5.1.3 Thermal Characteristics

The two packages have equivalent thermal characteristics.

Table 5-3. Thermal Characteristics of TS81102G0 and AT84CS001

Parameter	TS81102G0	AT84CS001
Rthj-bottom of balls – Thermal resistance from junction to bottom of balls	4.8°C/W	5°C/W
Rthj-case – Thermal resistance from junction to case	1.40°C/W max	1.70°C/W max
Moisture	MLS3	MSL3

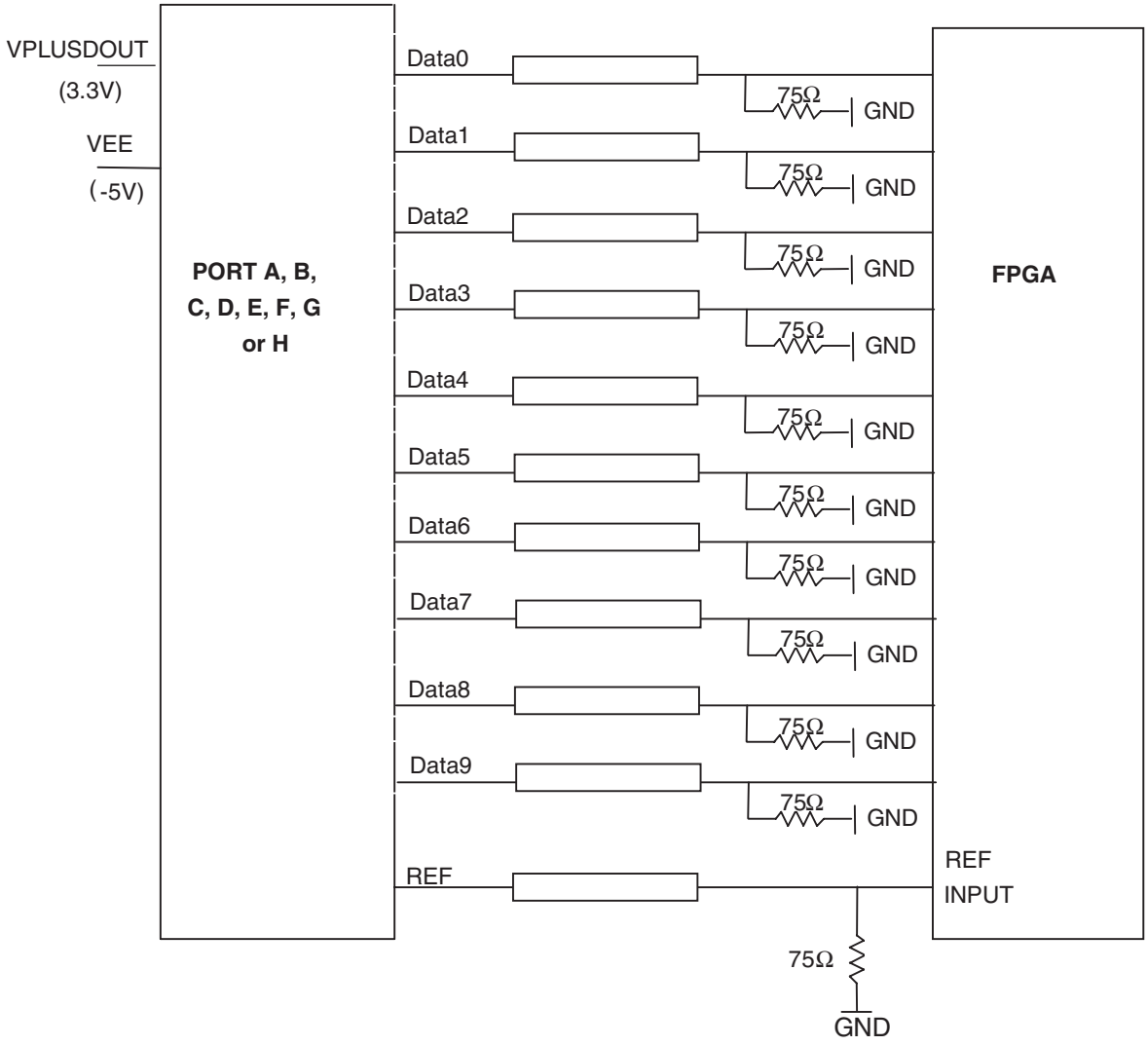
Notes: 1. The TS81102G0 package top side (copper heat spreader) is electrically connected to V_{EE} = –5V while the AT84CS001 package top side (copper heat spreader) is at 0V.

2. The same heat sink can be used for both devices.

5.2 Output Data Interfacing

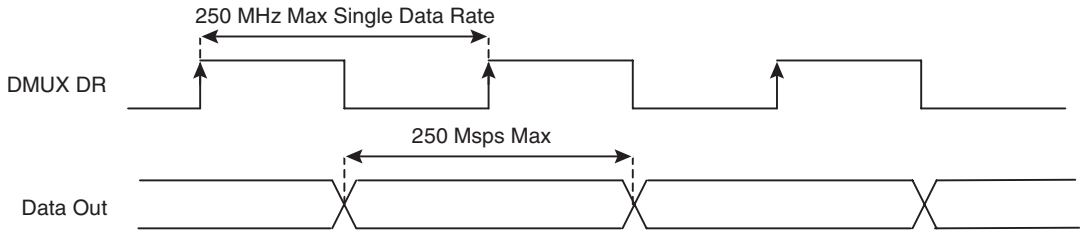
In the case of the TS81102G0, the output data were defined as pseudo differential signals as each port (A, D, C, D, E, F, G, H) was constituted by 10 single-ended signals (bit 0 to 9) and one reference signal. You then had the choice between several output standard such as SSTL 2 class I, TTL, PECL and ECL, which could be set thanks to the V_{PLUSD} output power supply, to interface the TS81102G0 to any standard FPGA using a single data rate protocol.

Figure 5-2. TS81102G0 DMUX Interfacing with a Standard FPGA (TTL Example)



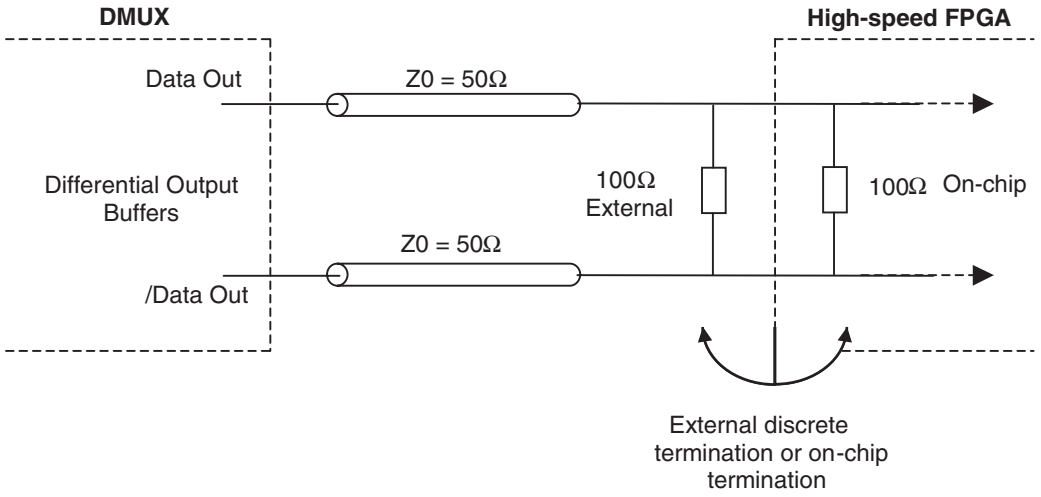
The TS81102G0 works in single data rate only, with a maximum output data rate of 250 Msps in both 1:4 and 1: 8 DMUX ratio.

Figure 5-3. TS81102G0 DMUX Interfacing with a Standard FPGA (Timings – 1:4 or 1:8 DMUX Ratio)



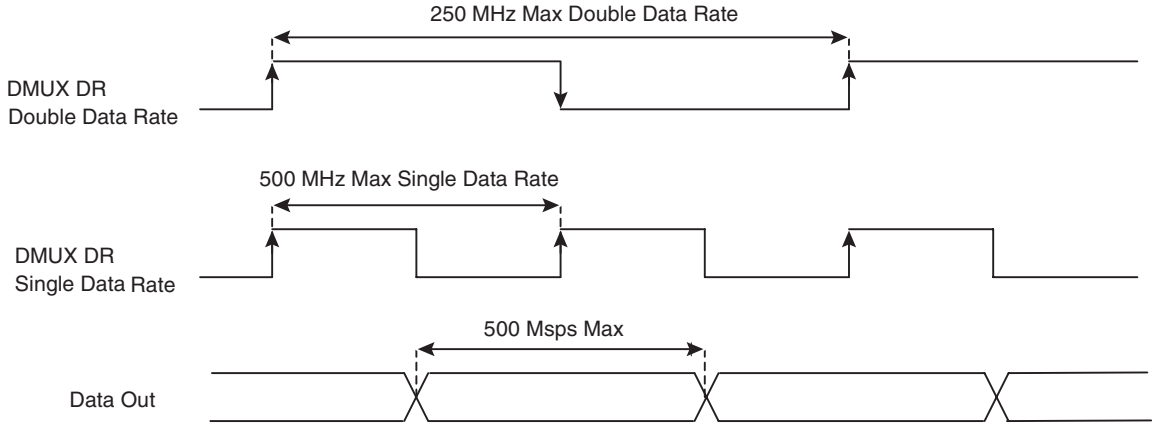
In the case of the AT84CS001, the output data and clock are LVDS and need to be 100Ω terminated (either by discrete 100Ω resistors or inside the FPGA if this feature is available in the FPGA).

Figure 5-4. AT84CS001 DMUX Interfacing with a Standard FPGA



The AT84CS001 works either in single data rate or in double data rate. The maximum output data rate is 500 Msps in both 1:2 and 1:4 DMUX ratio:500 MHz output clock in single data rate and 250 MHz output clock in double data rate, which makes it compliant with standard high speed FPGAs.

Figure 5-5. AT84CS001 DMUX Interfacing with a Standard FPGA (Timings – 1:2 or 1:4 DMUX Ratio)



6. Board Implementation

6.1 Power Supplies

In the TS81102G0 device, it was necessary to use three power supplies (or even four in some cases): V_{EE} = –5V, V_{CC} = 5V and V_{PLUSD} = 0V to 3.3V depending on the required output levels (and V_{TT} = –2V to 1.3V depending on the application).

With the AT84CS001 DMUX, only two power supplies are now necessary: V_{CCD} = 3.3V and V_{PLUSD} = 2.5V.

To simplify migration from the TS81102G0 to the AT84CS001, all the pins used for power supplies in the first device are also used as power pins in the second.

The pins formerly used for V_{EE} in the TS81102G0 are now used for V_{CCD} in the AT84CS001, thus enabling you to keep the same layer for the V_{CC} power supply as for the former V_{EE}.

The pins used formerly for V_{PLUSD} in the TS81102G0 are still used for V_{PLUSD} in the AT84CS001, also enabling you to keep the same layer for the V_{PLUSD} power supply.

The V_{CC} power supply of the TS81102G0 is replaced by 2 *N/C* (no connect) pins on D15 and D16 but pin J4 becomes V_{PLUSD} in the AT84CS001.

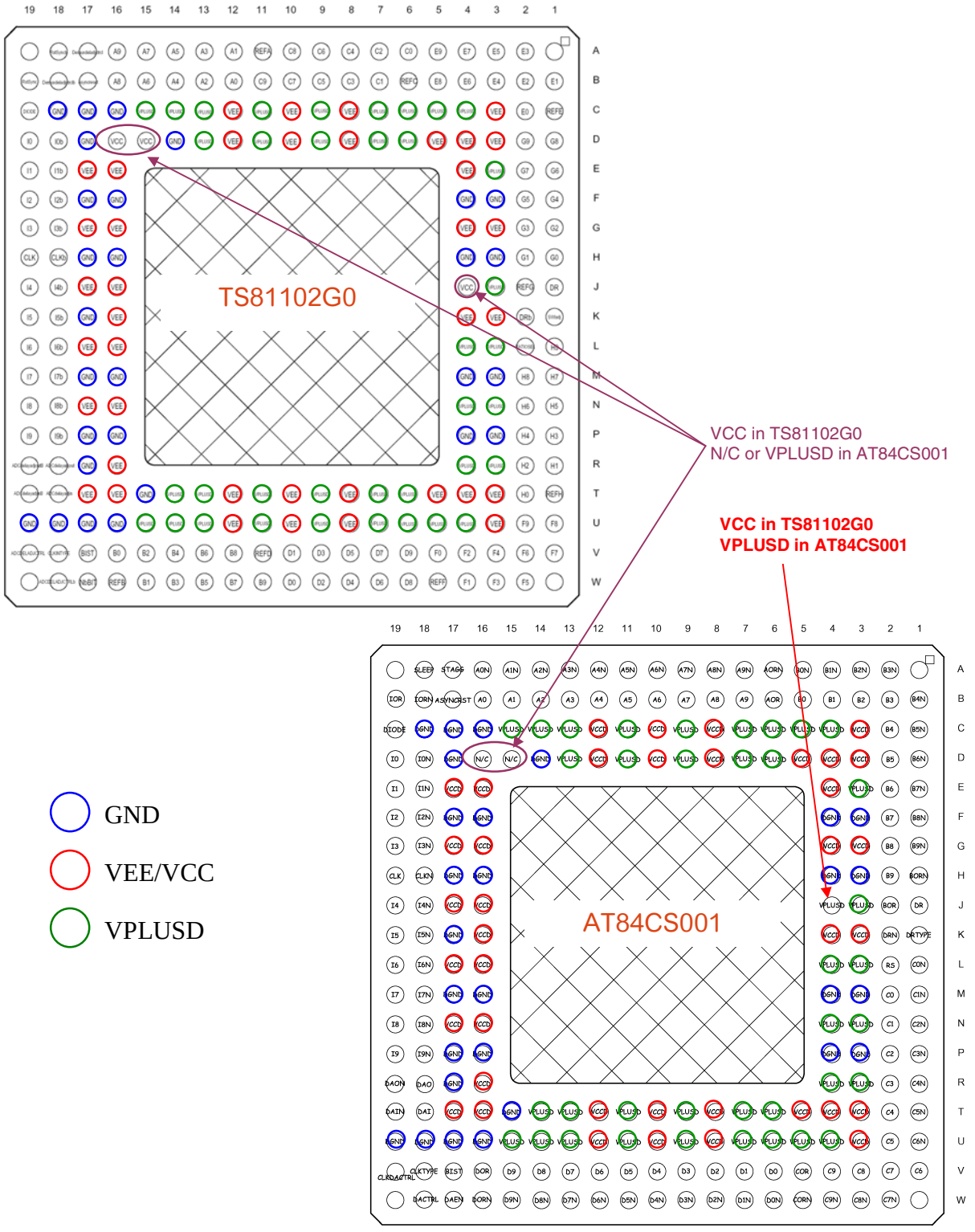
Since pins D15 and D16 are not connected to the AT84CS001 device, it is possible to connect them to V_{PLUSD} = 2.5V so as to simplify layout (the V_{CC} plane in TS81102G0 becomes V_{PLUSD}).

Finally, the same ground pins are used in both designs.

Table 6-1. Power Supplies Pin Assignment

Pin Number	TS81102G0 Signal name	AT84CS001 Signal Name
C12, C10, C8, C3, D12, D10, D8, D5, D4, D3, E17, E16, G17, G16, G4, G3, J17, J16, K16, K4, K3, L17, L16, N17, N16, R16, T17, T16, T12, T10, T8, T5, T4, T3, U12, U10, U8, U3	V_{EE}	V_{CCD}
C18, C17, C16, D17, D14, F17, F16, F4, F3, H17, H16, H4, H3, K17, M17, M16, M4, M3, P17, P16, P4, P3, R17, T15, U19, U18, U17, U16	GND	DGND
C15, C14, C13, C11 C9, C7, C6, C5, C4, D13, D11, D9, D7, D6, E3, J4, J3, L4, L3, N4, N3, R4, R3, T14, T13, T11, T9, T7, T6, U15, U14, 13, U11, U9, U7, U6, U5, U4	V_{PLUSD}	V_{PLUSD}
D15, D16	V_{CC}	N/C but can be connected to V_{PLUSD}
J4	V_{CC}	V_{PLUSD}

Figure 6-1. Matching of Power Pins on TS81102G0 and AT84CS001 Devices



6.2 Input Data, Input and Output Clock Signals

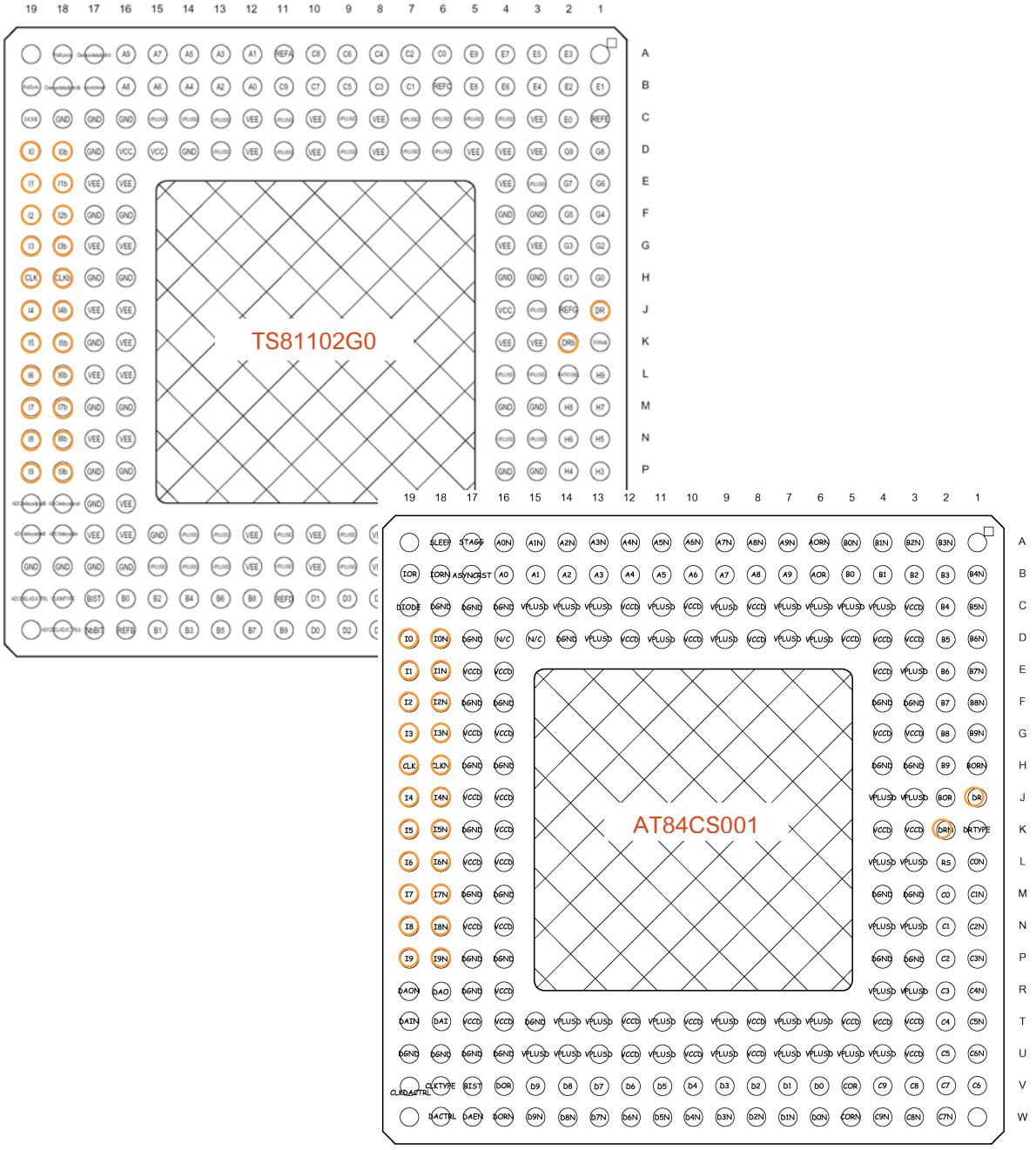
The 10-bit input data from I0/I0b to I9/I9b (I0/I0N to I9/I9N in the AT84CS001), the input clock CLK/CLKb (or CLK/CLKN in the AT84CS001) as well as the output clock DR/DRb (DR/DRN in the AT84CS001) are assigned the same pins in both devices.

This implies that the same board layout for these signals can be maintained.

Table 6-2. Input Data, Input and Output Clock Pin Assignment

Signal name	TS81102G0 Pin Number	AT84CS001 Pin Number
I0…I9	D19, E19, F19, G19, J19, K19, L19, M19, N19, P19	D19, E19, F19, G19, J19, K19, L19, M19, N19, P19
I0b…I9b (I0N…I9N)	D18, E18, F18, G18, J18, K18, L18, M18, N18, P18	D18, E18, F18, G18, J18, K18, L18, M18, N18, P18
CLK/CLKb (CLK/CLKN)	H19, H18	H19, H18
DR/DRb (DR/DRN)	J1, K2	J1, K2

Figure 6-2. Input Data, Input and Output Clock Pinout

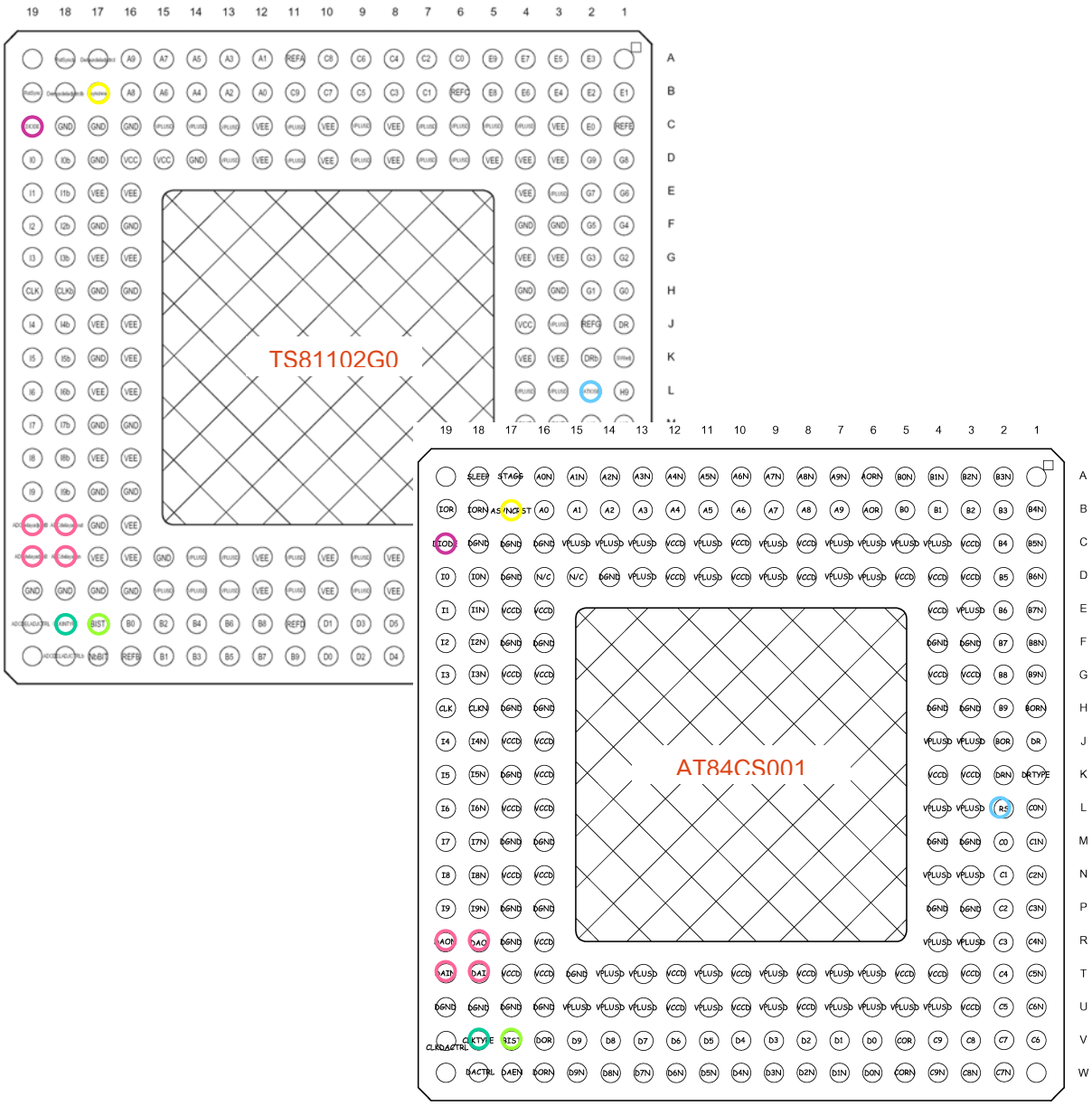


7. Other Functions

Table 7-1. Pinout Compatibility of Other Functions

Pin Number	TS81102G0 Signal name	AT84CS001 Signal name
C19	DIODE	DIODE
B17	Asyncreset	ASYNCRST
V18	CLKINTYPE	CLKTYPE
R18	ADCDelAdjOut	DAO
R19	ADCDelAdjOutb	DAON
T18	ADCDelAdjIn	DAI
T19	ADCDelAdjInb	DAIN
L2	RATIOSEL	RS
V17	BIST	BIST

Figure 7-1. Pinout Compatibility of Other Functions



7.1 Summary of Pinout Compatibility

Figure 7-2. TS81102G0 Pinout

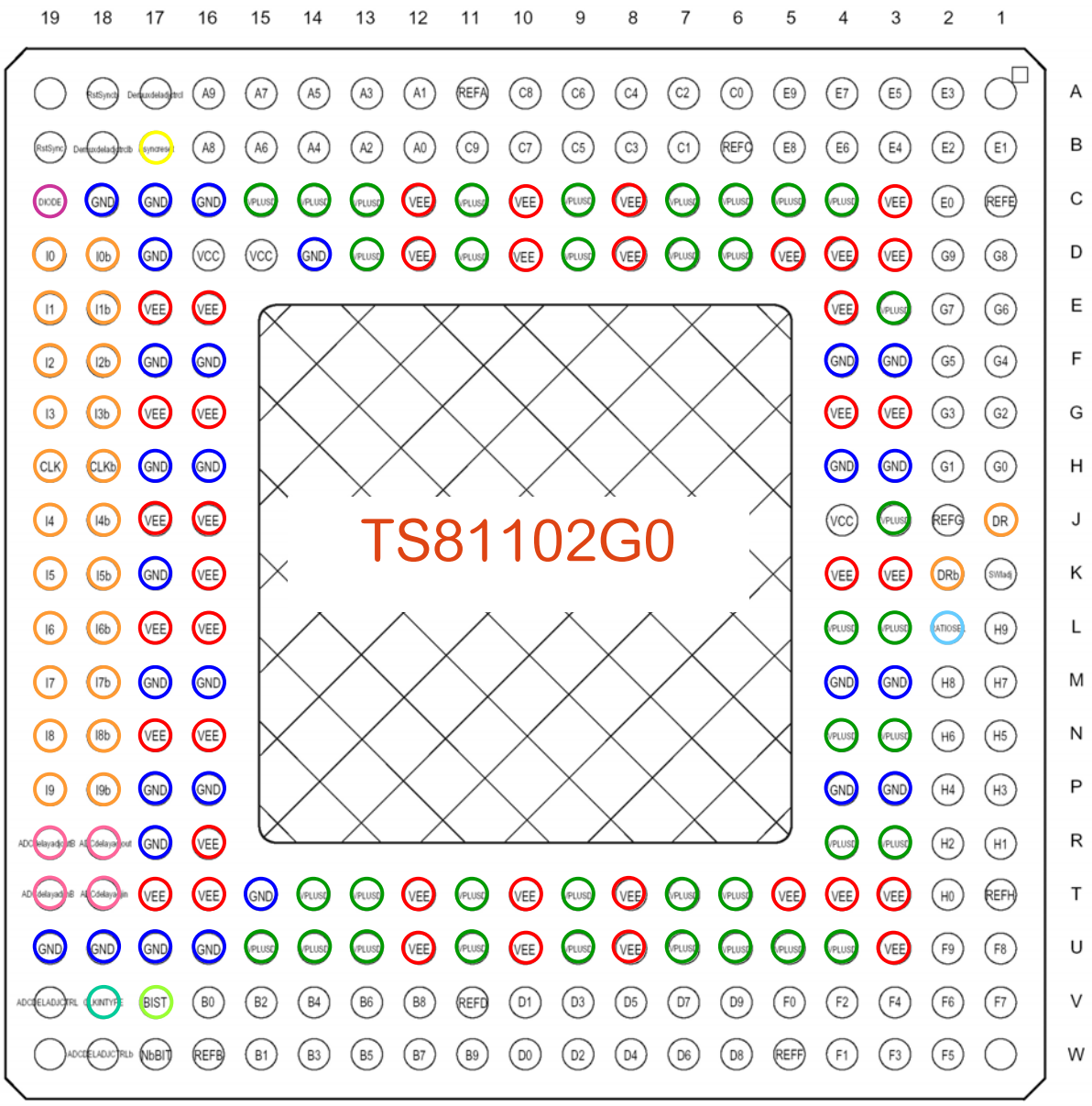
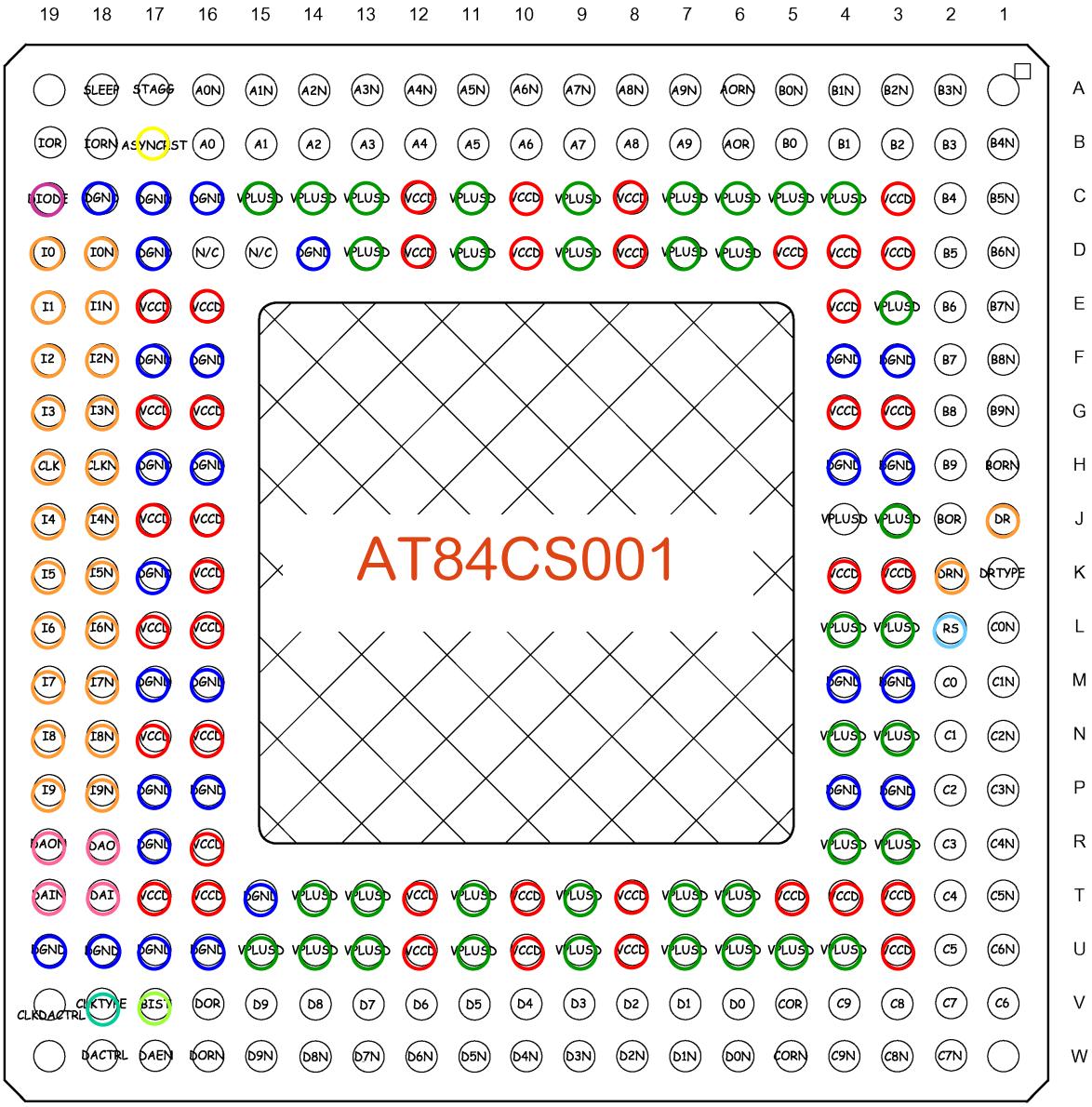


Figure 7-3. AT84CS001 Pinout



7.2 Summary of Differences in Layout

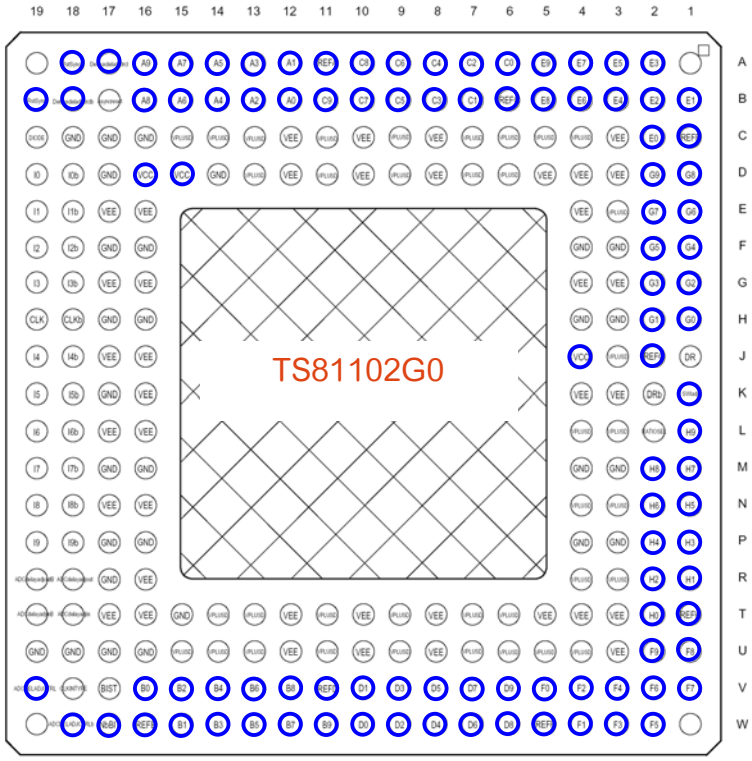
Table 7-2. Pin Differences between TS81102G0 and AT84CS001

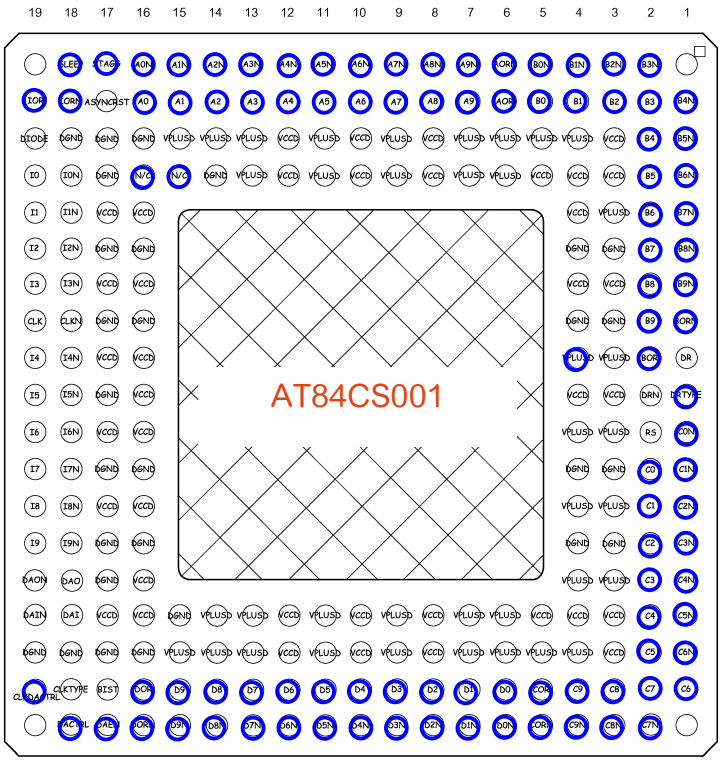
Pin Number	TS81102G0 Signal Name	AT84CS001 Signal Name	Pin Number	TS81102G0 Signal Name	AT84CS001 Signal Name
B19	RstSync	IOR	L1	H9	C0N
A18	RstSyncb	SLEEP	M2	H8	C0
A17	Demuxdeladjctrl	STAGG	M1	H7	C1N
B18	Demuxdeladjctrlb	IORN	N2	H6	C1
A16	A9	A0N	N1	H5	C2N
B16	A8	A0	P2	H4	C2
A15	A7	A1N	P1	H3	C3N
B15	A6	A1	R2	H2	C3
A14	A5	A2N	R1	H1	C4N
B14	A4	A2	T2	H0	C4
A13	A3	A3N	T1	RefH	C5N
B13	A2	A3	U2	F9	C5
A12	A1	A4N	U1	F8	C6N
B12	A0	A4	V1	F7	C6
A11	RefA	A5N	V2	F6	C7
B11	C9	A5	W2	F5	C7N
A10	C8	A6N	V3	F4	C8
B10	C7	A6	W3	F3	C8N
A9	C6	A7N	V4	F2	C9
B9	C5	A7	W4	F1	C9N
A8	C4	A8N	V5	F0	COR/DRCN
B8	C3	A8	W5	RefF	CORN/DRC
A7	C2	A9N	V6	D9	D0
B7	C1	A9	W6	D8	D0N
A6	C0	AORN/DRA	V7	D7	D1
B6	RefC	AOR/DRAN	W7	D6	D1N
A5	E9	B0N	V8	D5	D2
B5	E8	B0	W8	D4	D2N
A4	E7	B1N	V9	D3	D3
B4	E6	B1	W9	D2	D3N
A3	E5	B2N	V10	D1	D4
B3	E4	B2	W10	D0	D4N
A2	E3	B2	V11	RefD	D5
B2	E2	B3	W11	B9	D5N
B1	E1	B4N	V12	B8	D6
C2	E0	B4	W12	B7	D6N

Table 7-2. Pin Differences between TS81102G0 and AT84CS001 (Continued)

Pin Number	TS81102G0 Signal Name	AT84CS001 Signal Name	Pin Number	TS81102G0 Signal Name	AT84CS001 Signal Name
C1	RefE	B5N	V13	B6	D7
D2	G9	B5	W13	B5	D7N
D1	G8	B6N	V14	B4	D8
E2	G7	B6	W14	B3	D8N
E1	G6	B7N	V15	B2	D9
F2	G5	B7	W15	B1	D9N
F1	G4	B8N	V16	B0	DOR/DRDN
G2	G3	B8	W16	RefB	DORN/DRD
G1	G2	B9N	J4	V_{CC}	V_{PLUSD}
H2	G1	B9	K1	SWIadj	DRTYPE
H1	G0	BORN/DRB	W17	NbBIT	DAEN
J2	RefG	BOR/DRBN	V19	ADCDELADJCTRL	CLKDACTRL
D15, D16	V_{CC}	N/C or V_{PLUSD}	W18	ADCDELADJCTRLb	DACTRL

Figure 7-4. Pin Differences between TS81102G0 and AT84CS001





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