EV12AS350BTPY-EB Evaluation Board

12-bit ADC 5.4GSps
USER GUIDE

TELEDYNE e2v
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Table of contents

Section 1

General Overview

The EV12AS350BTPY-EB Evaluation Board enables the easy evaluation of the characteristics and performance of EV12AS350 12-bit ADC. The Evaluation Board is plug_and_play and needs little external equipment.

The Evaluation Board is delivered with software which allows acquisition of data using the FPGA and Graphical User Interface (GUI). The FPGA VHDL data acquisition code is supplied with the Evaluation Board.

1.1 Disclaimer

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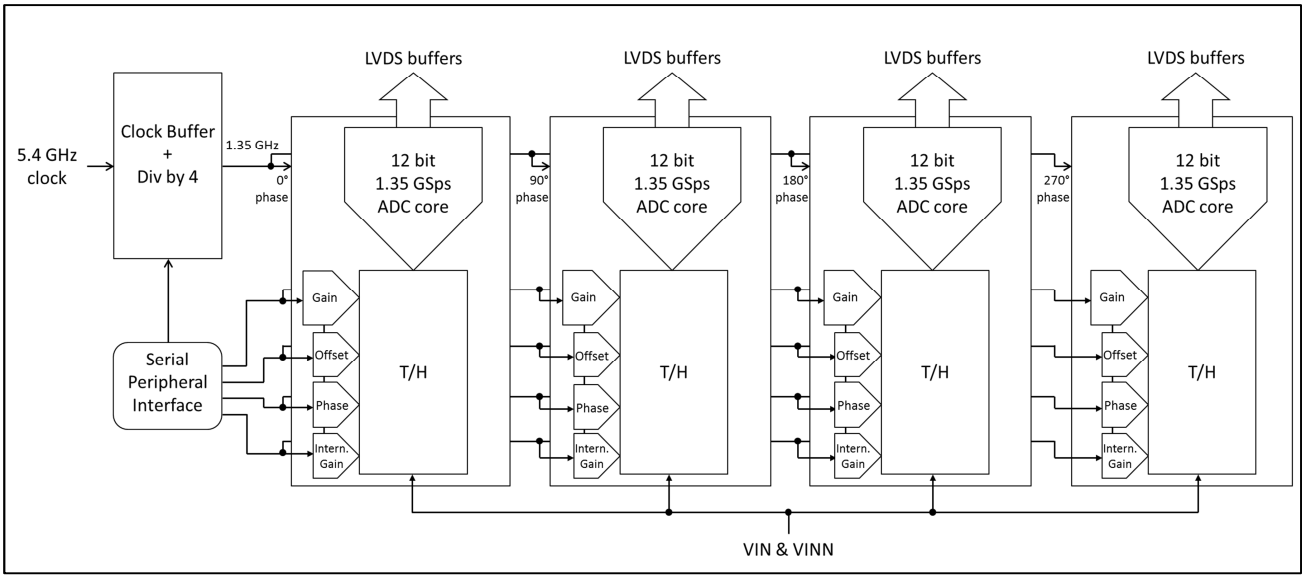
1.2 EV12AS350 ADC

The EV12AS350B-EB Evaluation Board is based on Teledyne e2v EV12AS350 12-bit 5.4Gsps ADC whose block diagram is given on figure 1-1.

Figure 1-1. EV12AS350 Simplified Block Diagram



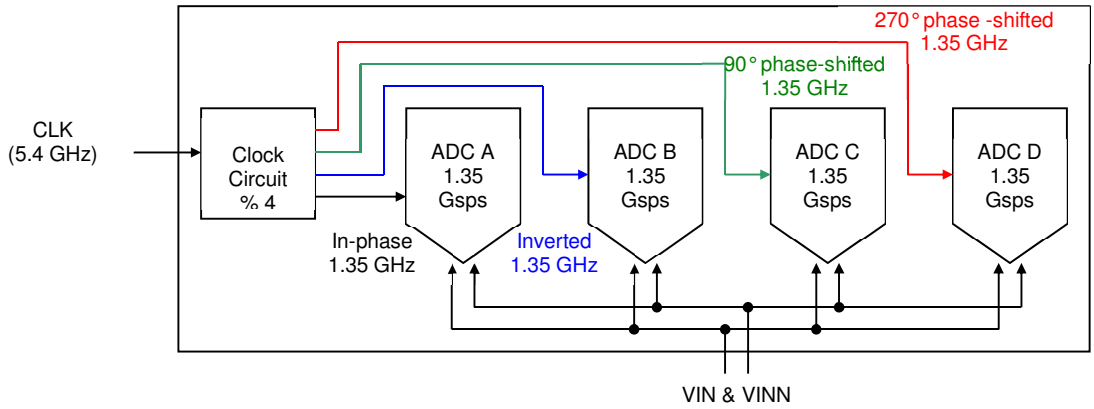
The ADC is made up of four identical 12-bit ADC cores where all four ADCs are all interleaved together.

All four ADCs are clocked by the same external input clock signal delayed with the appropriate phase.

The Clock Circuit is common to all four ADCs. This block receives an external 5.4 GHz clock (maximum frequency) and preferably a low jitter sinewave signal. In this block, the external clock signal is then divided by 4 in order to generate the internal sampling clocks.
The in-phase 1.35 GHz clock is sent to ADC A while the inverted 1.35 GHz clock is sent to ADC B; the in-phase 1.35 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1.35 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 5.4 Gsps.

Note: This document should be used in conjunction with the other documentation relating to this product, Datasheet, Application notes … etc. Several adjustments for the sampling delay and the phase are tuned during initial manufacturing test in this clock circuit to ensure a proper phase relation between the different clocks generated internally from the 5.4 GHz clock.

Figure 1-2. EV12AS350 internal interleaving configuration



Please refer to datasheet 1209A for more information on EV12AS350B 12-bit ADC.

1.3 Evaluation Board

The Evaluation Board is based on an EV12AS350B ADC with a FPGA Altera Arria V.

The Evaluation Board includes:

- PCB with a soldered EV12AS350B ADC and a FPGA Altera Arria V model 5AGXB3
- USB cable for the communication between the board and the PC (ADC settings and configuration, settings for data acquisition and data transmission)
- Analog input with two SMA connectors (differential input)
- Clock input with two SMA connectors (differential input)
- CD-ROM with GUI

Figure 1-3. Architecture of EV12AS350 - Evaluation Board

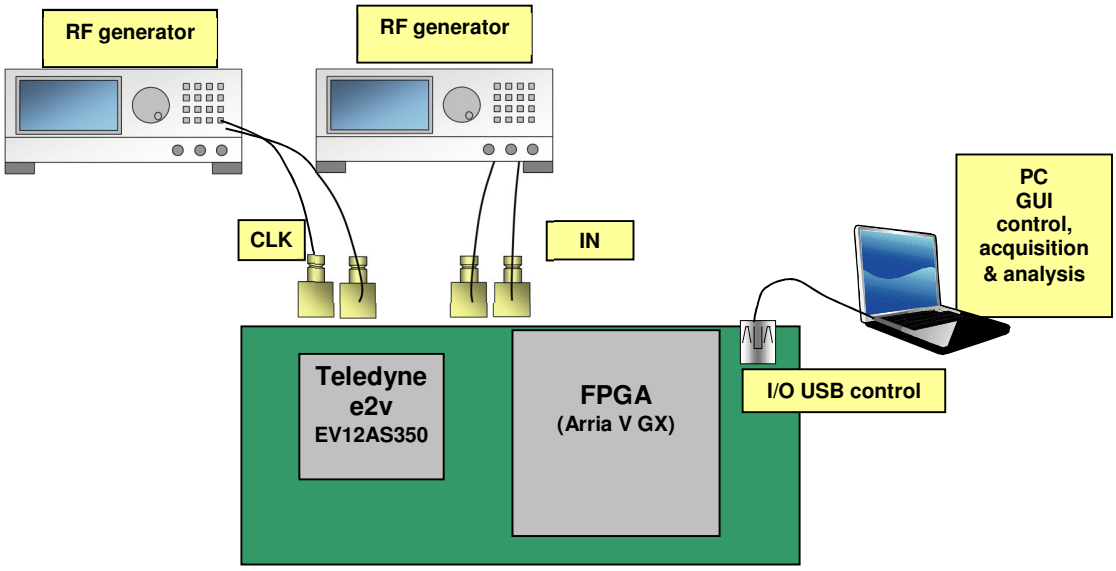
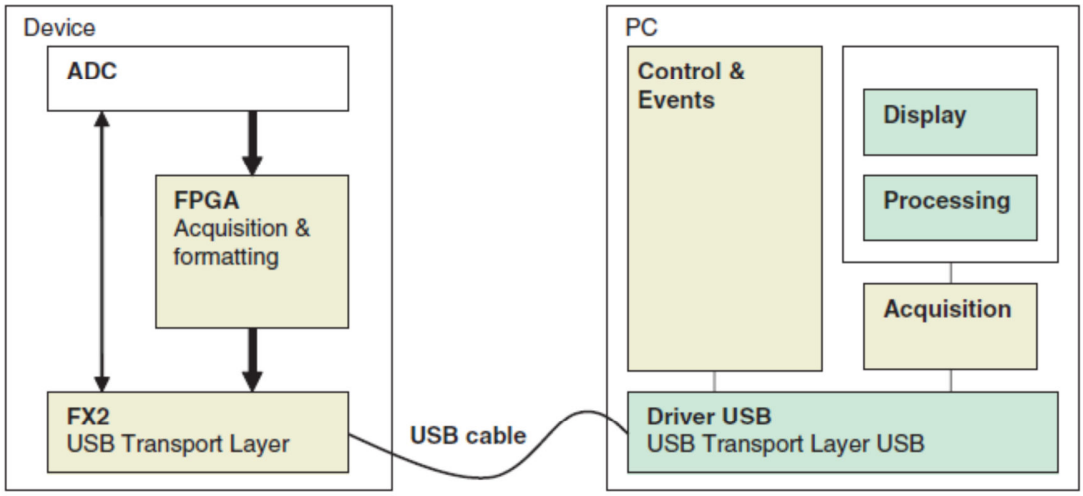


Figure 1-4. EV12AS350 - functional architecture



Acquisition and formatting of ADC digital output data are done within the FPGA.
A USB driver on the ADC Evaluation Board allows for transmission of the data to the computer that performs the display and processing of ADC output data (FFT).
Software and Graphical User Interface are provided with the Evaluation Board.
The provided software operates using Labview® RunTime (no license required).

FX2 microcontroller is used:

- To do the reset sequence (SYNC) of the ADC
- To detect the ADC
- To control and configure ADC settings via its SPI which is driven by the FPGA
- To control the FPGA by SPI
- To ensure the transmission of acquisition data from FPGA to PC via the USB port
- To communicate with the PC via USB port

Figure 1-5. EV12AS350 - Evaluation Board dimensions

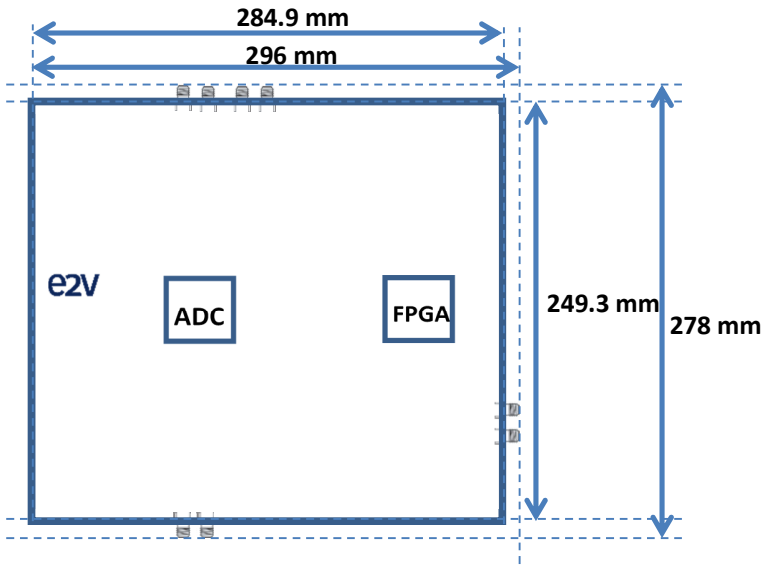
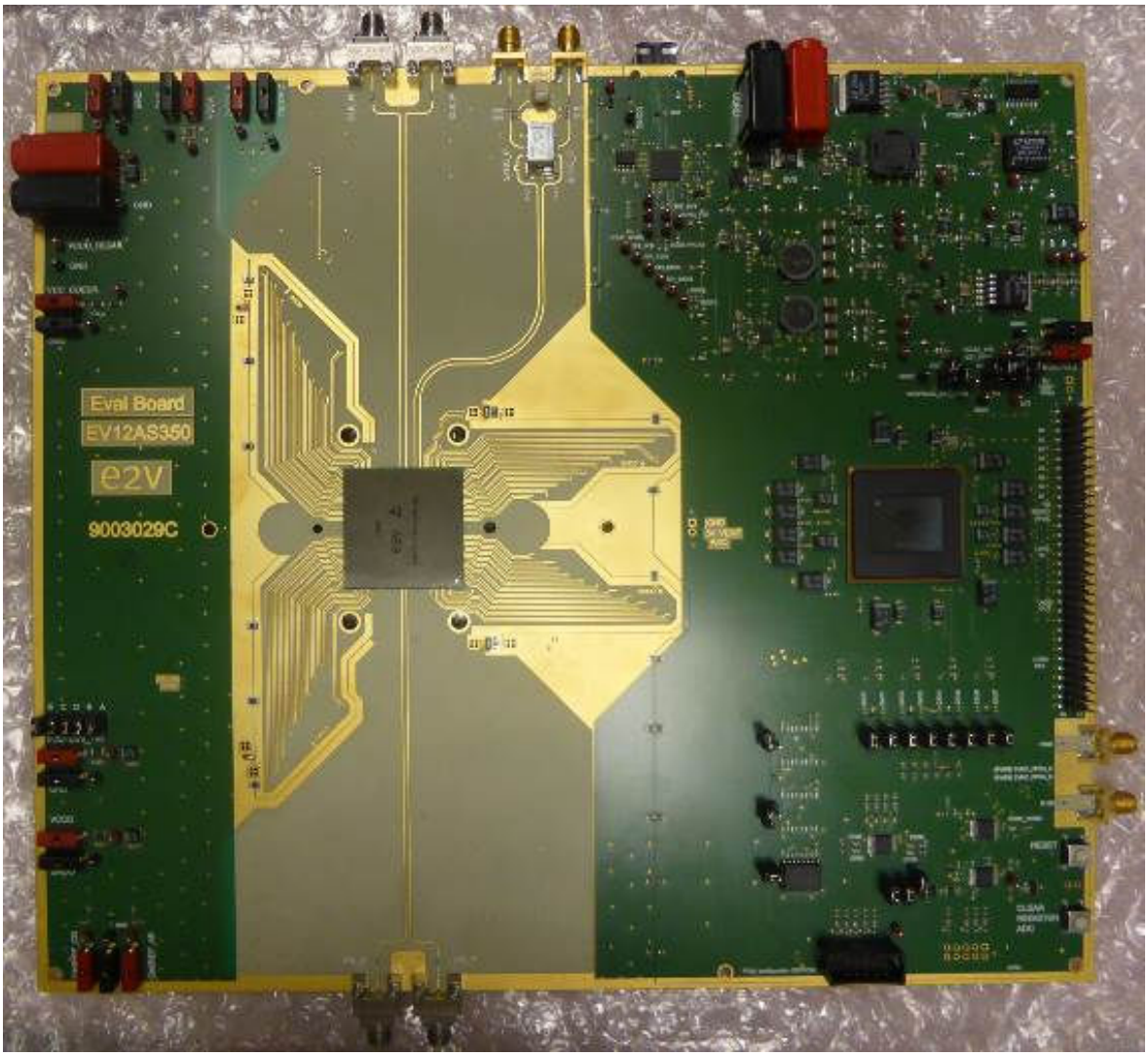


Figure 1-6. EV12AS350 - Evaluation Board photo (TOP VIEW)



Section 2

Quick start

2.1 Required equipment

The EV12AS350 - Evaluation Board requires the following equipment to operate:

- A RF generator for the clock
  To get optimum dynamic performances, a low phase noise generator is mandatory.
  A balun is mandatory to provide a differential clock to the Evaluation Board.

- A RF generator for the analog input
  To get optimum dynamic performances, a low phase noise generator is mandatory.
  A balun is mandatory to provide a differential analog input to the Evaluation Board.
  A filter is also necessary on analog input.

- Cables for power requirements (both ADC and FPGA power)

- USB cable to connect the Evaluation Board to the PC

- The differential analog and clock input are provided by SMA connectors Southwest SMA 2.92 mm.

- Incoming power supplies are bypassed by the banana jack (2mm-5A-EFJ or EMBASE-4mm-10A-DLT)

- A PC operating with Windows XP or Windows 7 (32 ou 64 bits)

Optionally:

- A multimeter to monitor the ADC junction temperature

Table 2-1. Examples of RF generators for CLK or VIN

Signal generator	**SSB phase noise @1GHz (20 KHz offset)**
Agilent E4424B 250KHz 2GHz (High spectral purity)	< -134dBc/Hz
Agilent E4426B 250KHz 4GHz (High spectral purity)	< -134dBc/Hz
Rohde & Schwarz SMA100A 9 KHz 6GHz (High spectral purity)	< -140dBc/Hz

Table 2-2. Examples of balun for CLK and VIN

Balun reference	**Frequency range**
BROADBAND BALUN MARKI (BAL0006)	200KHz – 6GHz
MACOM 96341 - H9	2MHz – 2000MHz
ANAREN 3A0056 – 3dB coupler	2GHz – 4GHz

Table 2-3. Examples of power supplies current

Power supplies current
Rohde & Schwarz HMP4040
GWInstek PST3202

2.2 Evaluation Board connections setup

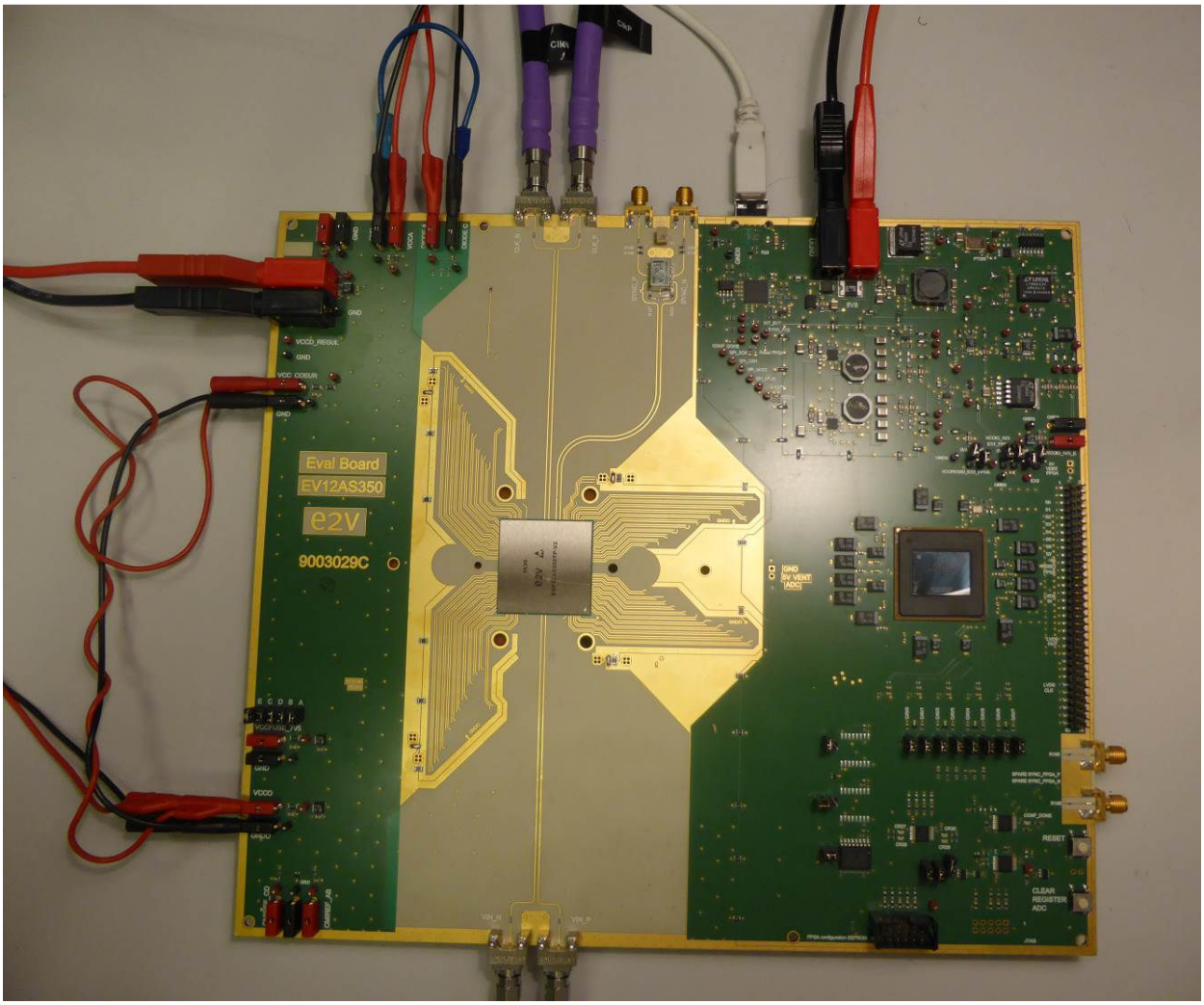
2.2.1 Power supplies

Connect Evaluation Board power supplies as described below:

- Connect a 2V power supply to connectors VCCO and VCC_COEUR
- Connect a 3.2V power supply to connector VCCD
- Connect a 4.8V power supply to VCCA
- Connect a 5.5V power supply to connector 5v5 (FPGA power supply)

Note: It is not necessary to connect GND and GNDO grounds (it is done within PCB).
It is mandatory to connect DIODEC to GND as shown on Figure 2-1, even if temperature is not monitored.

Figure 2-1. Photo of EV12AS350 board with connections



Note: VCCFUSE_7V5 connector and its GND (left side of PCB) needs to remain unconnected.

2.2.2 Clock input

Connect clock RF generator to Evaluation Board SMA (label CLK_P, CLK_N) via SMA cables and balun. A filter can be added on input clock, but it is not mandatory.

2.2.3 Analog input

Connect Analog Input RF generator to Evaluation Board SMA (label VIN_P, VIN_N) via SMA cables and balun. A filter is mandatory.

2.2.4 USB

Use the USB cable (provided with Evaluation Board) to connect PCB to the PC.

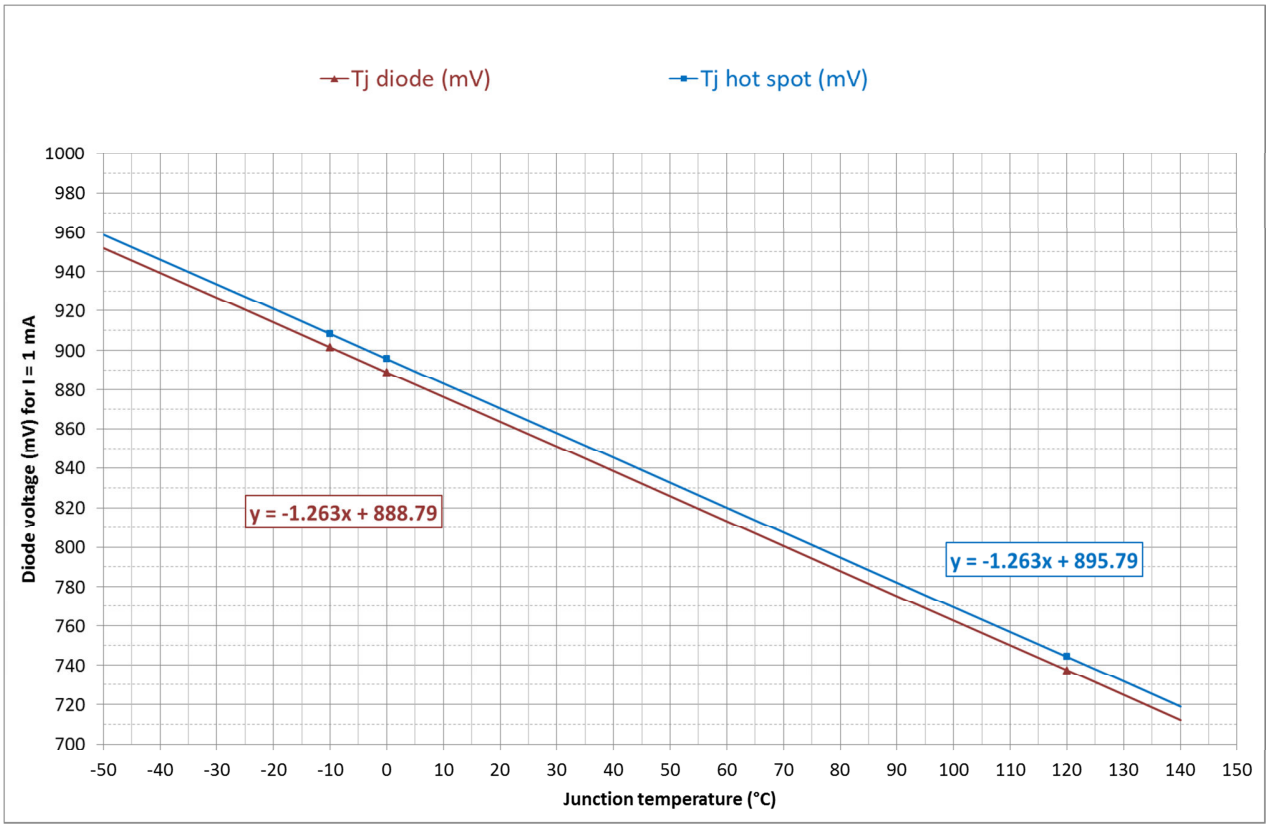
2.2.5 SYNC input

It is possible to apply a SYNC signal either by GUI, either by a potentiometer button on PCB, or by an external signal. In that case the external signal has to be connected to Evaluation Board on SMA label SYNC_P, SYNC_N. In other cases, these SMA connectors can remain unconnected.

2.2.6 Temperature Diode monitoring

A multimeter can be used to monitor the ADC junction temperature. In that case, it has to be connected between connectors DIODEA and DIODEC. It is mandatory to connect DIODEC to GND as shown on Figure 2-2.
The Diode Characteristic is provided below (for I = 1 mA)

Figure 2-2. Temperature Diode characteristic for I = 1 mA ***(with DiodeC=GND)***



Operating procedure

1. Install the Software as described in Section 4 Software Tools.
2. Connect power supplies, clock, analog input and USB cable as described in chapter 2.2.
3. Turn ON 5.5V FPGA power supply
4. Turn ON ADC power supplies
5. Turn ON clock generator
6. Turn ON Analog input generator
7. Press “RESET” button on bottom right corner of PCB
8. Launch Setup_EV12AS350x-EB_GUI_v1.6.0.exe
9. Press « Hardware Reset » button from GUI (recommended in order to configure the ADC in default mode)
10. Verify that ADC currents are in accordance to the EV12AS350 datasheet available online.
11. Configure ADC in the desired mode
12. Press « SYNC» button from GUI (recommended for a proper synchronization of the 4 ADC cores)
13. Launch an acquisition and verify that the signal is correct and that the performance math the datasheet.

Section 3

Hardware Implementation

The Evaluation Board can be hardware configured by changing manually some capacitor or resistance. This chapter allows seeing all hardware configurations.

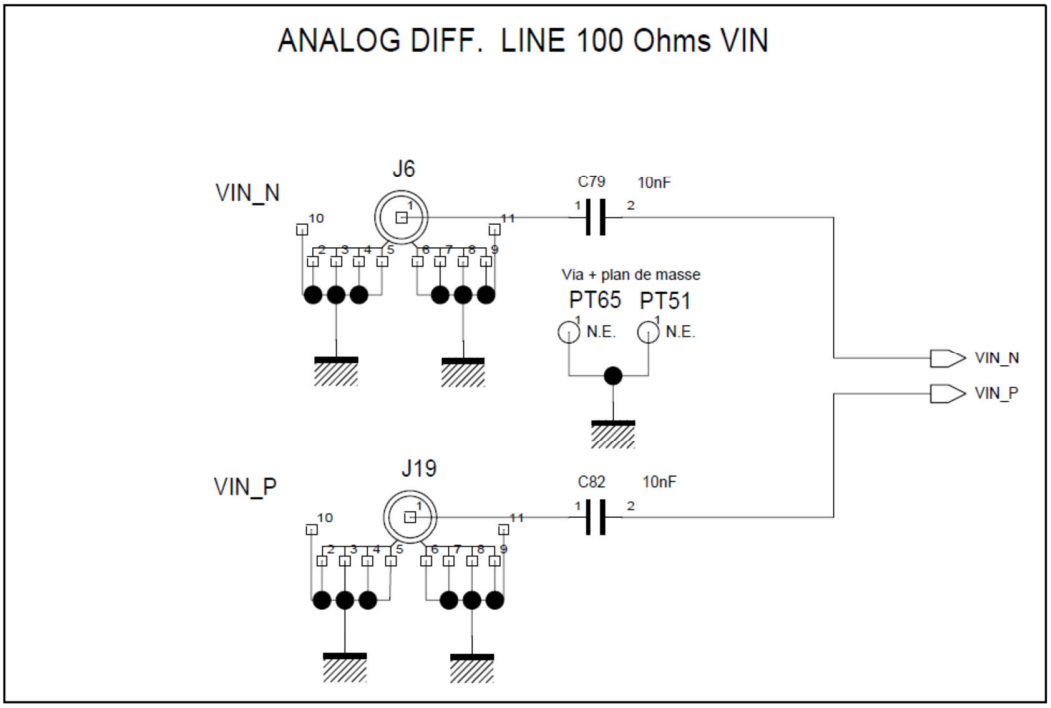
All Hardware modifications are made at user's risk.

3.1 Analog Input

Two SMA connectors are provided to access VIN and VINN. It is mandatory to use a differential signal (A balun can be used to provide differential signal. See example of balun references in Table 2-2 above.

The Analog Input is by default AC coupled (10nF AC coupling capacitors C79 and C82).

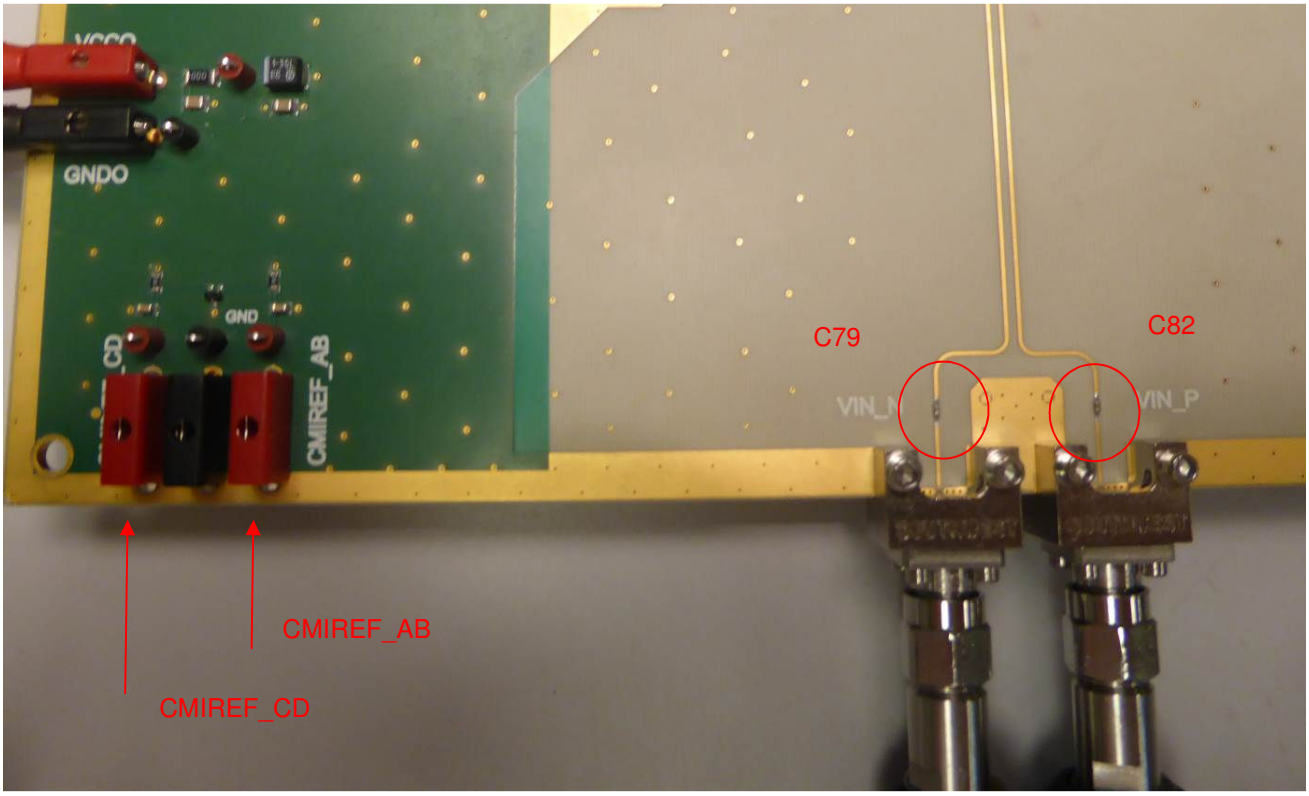
Figure 3-1. Evaluation Board Analog input schematic with AC coupling



It is possible to consider a DC coupled input impedance. In that case it is necessary to remove C79 and C82 capacitors and replace them by 0 ohm resistors. After this hardware modification, it is necessary to apply a common mode either through a T-bias either through output CMIRef which is the image of the internal ADC common mode of the ADC.

The figure 3-2 below shows the location of C79 and C82 capacitors and CMIRef outputs.

Figure 3-2. Photo of Analog input and CMIRef outputs



3.2 Clock Input

Two SMA connectors are provided to access CLK and CLKN. It is mandatory to use a differential signal (A balun can be used to provide differential signal. See example of balun references in Table 2-2 above).

The Clock Input is AC coupled with 10nF AC coupling capacitors.
As for Analog Input, it can be possible to consider a DC coupled impedance. Procedure is the same for Clock as for Analog input and is already described in chapter 3.1.

Figure 3-3. Evaluation Board Clock input schematic

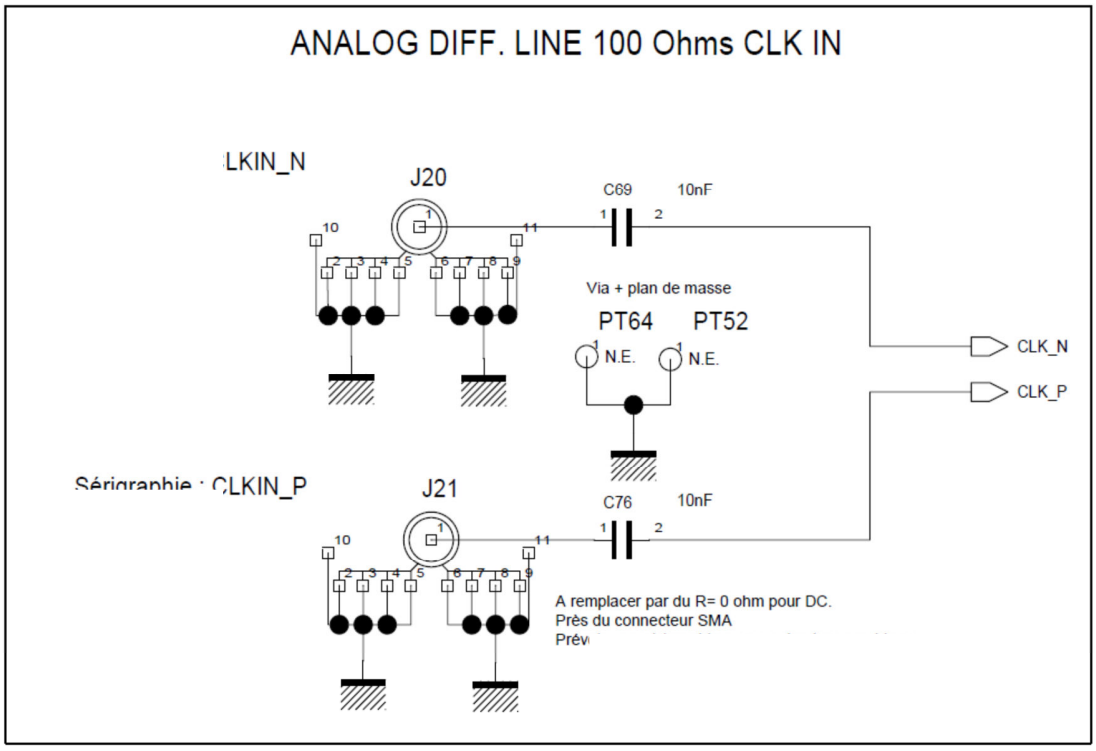
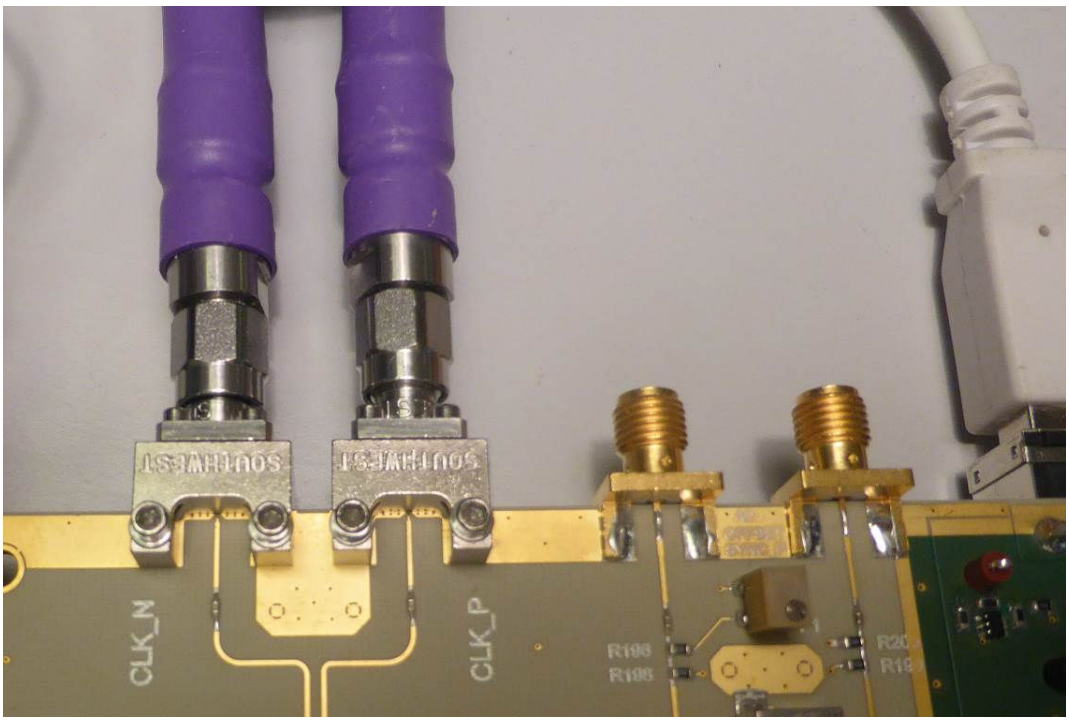


Figure 3-4. Photo of Clock Input is AC coupled with 10nF AC coupling capacitors



3.3 SYNC Signal

There are three ways of doing a SYNC on EV12AS350 - Evaluation Board:

- SYNC signal sent by the FPGA (Driven by SYNC button from GUI) = recommended option
- SYNC signal generated on board by a potentiometer (no need of external signal)
- External SYNC signal via SMA connectors

Figure 3-5. Evaluation Board SYNC input schematic

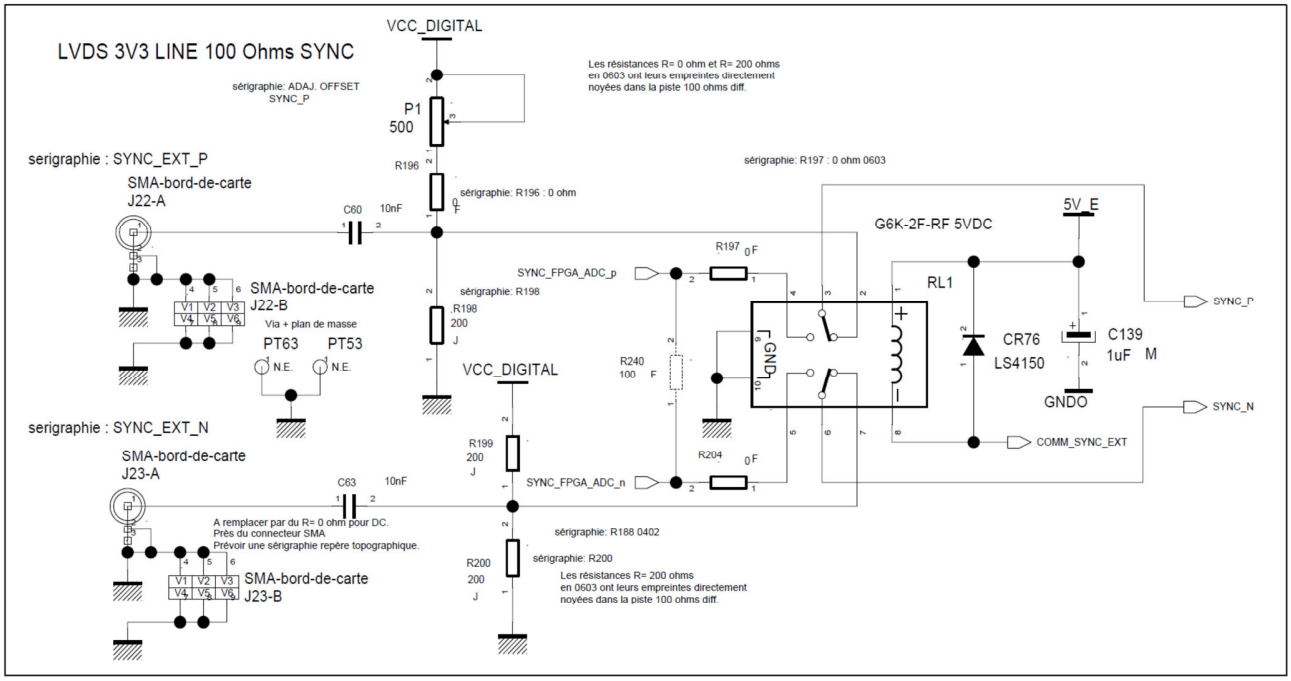
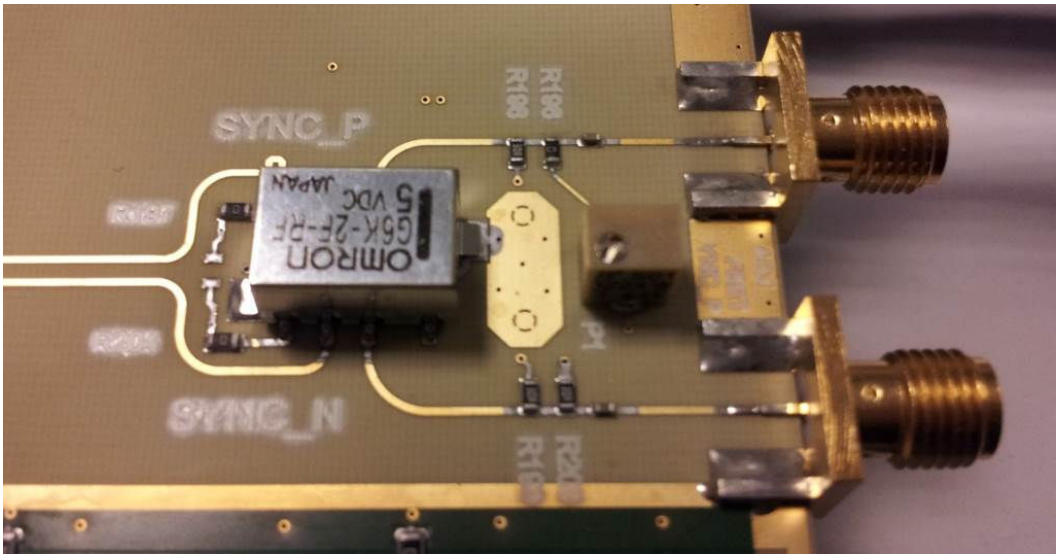


Figure 3-6. Evaluation Board SYNC input photo



3.3.1 SYNC Signal sent by FPGA (GUI driven = default hardware configuration)

When pressing the SYNC button from the GUI, the FPGA generates a pulse that is sent to the ADC via the FX2 microcontroller. This is the hardware configuration by default.
In this configuration it is mandatory to have R197 = 0Ω and R204 = 0Ω (See Figure 3-5).
It is not necessary to remove below resistors and capacitors to get a proper operation:
R196 = 0Ω, R198 = 200Ω, R199 = 200Ω and R200 = 200Ω.
C60 = 10 nF and C63 = 10nF.

This is the recommended option.

3.3.2 SYNC Signal generated on board

A SYNC signal can be generated via a potentiometer (P1 on Figure 3-5). This solution is based on the fact that SYNCP voltage has to be higher than SYNCN voltage in order that the ADC detects a SYNC command.
This option is less accurate than GUI-driven SYNC because of rebound issues.
With this option it is mandatory to have R196 = 0Ω, R198 = 200Ω.
It is not necessary to remove below resistors and capacitors to get a proper operation:
R197 = 0Ω, R204 = 0Ω, R199 = 200Ω and R200 = 200Ω.
C60 = 10 nF and C63 = 10nF.

3.3.3 External SYNC Signal

Two SMA connectors are provided to access SYNC_P and SYNC_N of the ADC (serigraphy SYNC_EXT_N and SYNC_EXT_P). With this option, a pulse generator needs to be connected to SMA in order to apply a LVDS pulse.
It is recommended to remove R196, R198, R199 and R200 to avoid any interference between potentiometer and pulse generator. Additionally, it is necessary to replace C60 and C63 by 0Ω resistors.
Be careful: FPGA needs to drive the SYNC signal between each training phase. This configuration with external SYNC is therefore not recommended.
Note: If FPGA is not powered ON, relay RL1 of figure 3-5 is in mode external SYNC.

3.4 Spare SYNC Signal for FPGA

A spare SYNC differential signal connected to FPGA is provided on the Evaluation Board in order to allow user to develop its own system. This spare signal is accessible through 2 SMA connectors (serigraphy SPARE SYNC_FPGA_P and SPARE SYNC_FPGA_N).

Contact Teledyne e2v hotline Hotline-BDC@Teledyne-e2v.com for more information on this functionality.

3.5 Jumpers configuration

The figures 3-7 and 3-8 below present the required jumpers configuration.
Evaluation Board is delivered with this default configuration that must not be changed.

Figure 3-7. Evaluation Board jumpers configuration (photo)

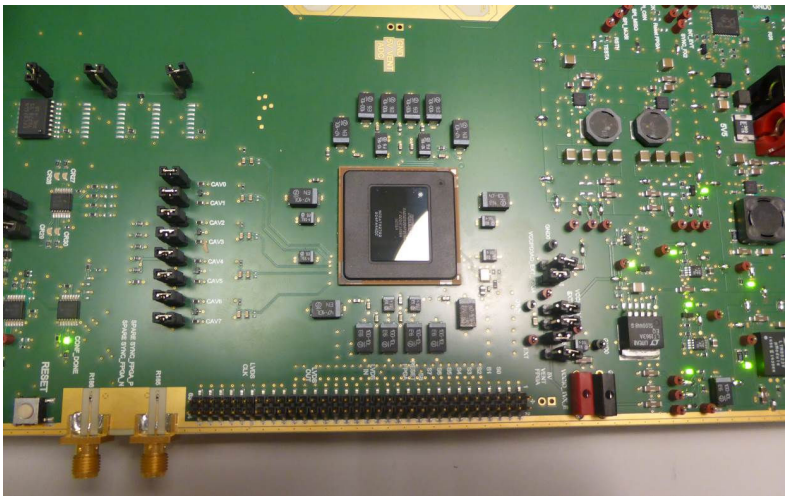
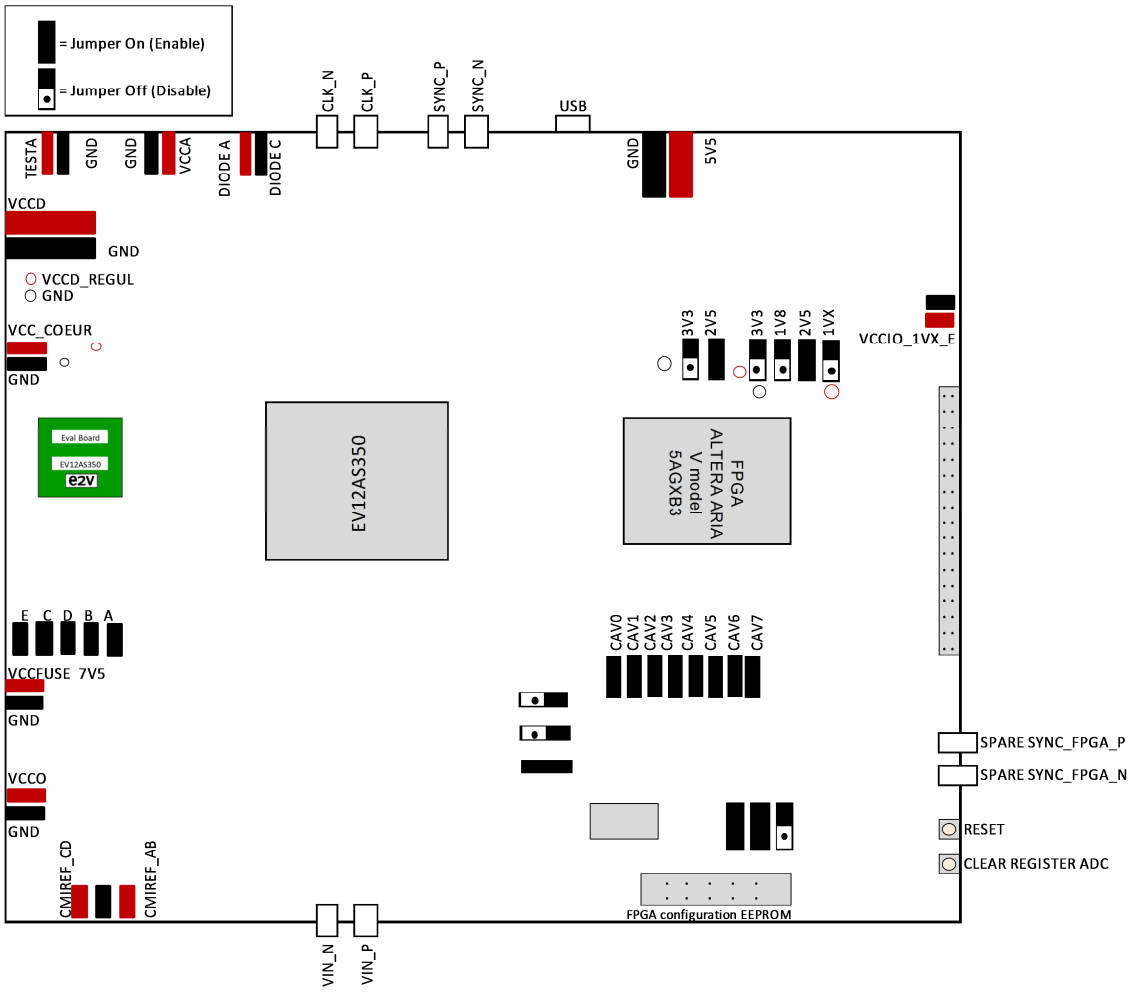


Figure 3-8. Evaluation Board jumpers configuration (synoptic)



Section 4

Software Tools

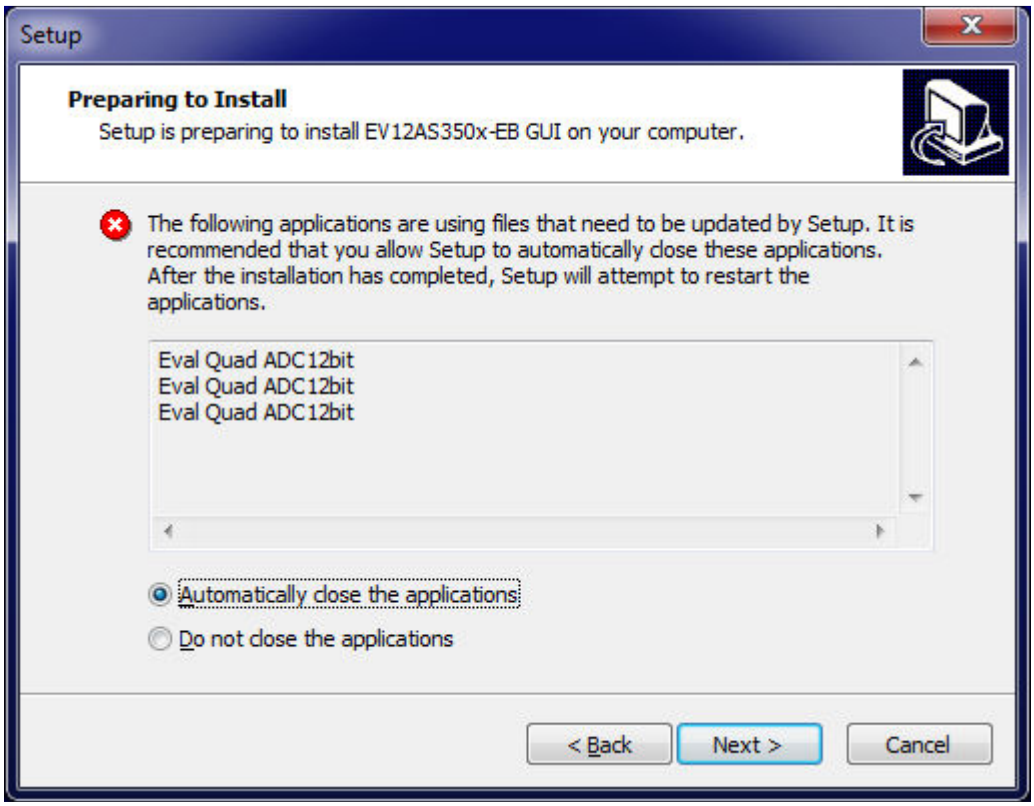
4.1 Introduction

The Evaluation Board requires two software tools to operate:

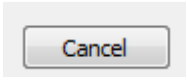
- Graphical User Interface: the user interface software is a Visual C++® compiled graphical interface that does not require a licence to run on a Windows® XP/7® ; Office 2010 and later PC. The software uses intuitive push-buttons and pop-up menus to configure the ADC and do data acquisition. To save acquisition data on Excel files, it is mandatory to have a Microsoft Excel version 2007 or more recent.
- A FPGA code: the FPGA code is provided with the Evaluation Board. Evaluation Board is delivered with FPGA code already downloaded within the FPGA. See Section 6 about FPGA code to have explanations on how to download a new FPGA code version.

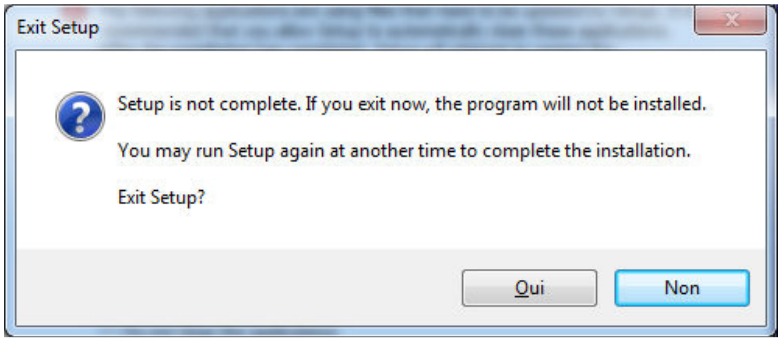
Warning: for the software installation, administrative rights are mandatory.
Warning: if the software is already installed, the window below appears.

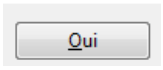
Figure 4-1. Error message window if software is already installed



It is necessary to remove previous versions prior to installing a new version.

Click on 



Click on 

4.2 Getting Started

Install the User interface (EV12AS350-EB GUI) application on your computer by launching the Setup_EV12AS350x-EB_GUI_v1.6.0.exe install).

The screen shown in Figure 4-2 is displayed:

Figure 4-2. Evaluation Board EV12AS350x application “setup wizard”

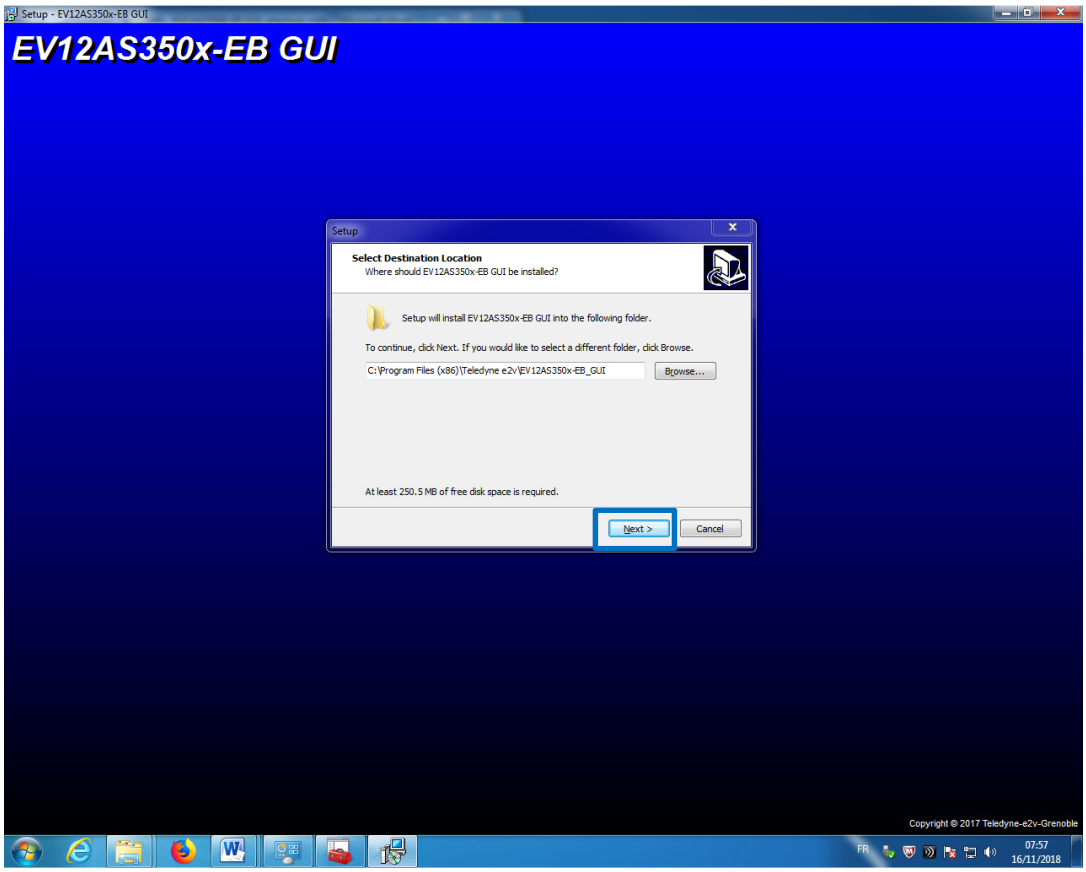
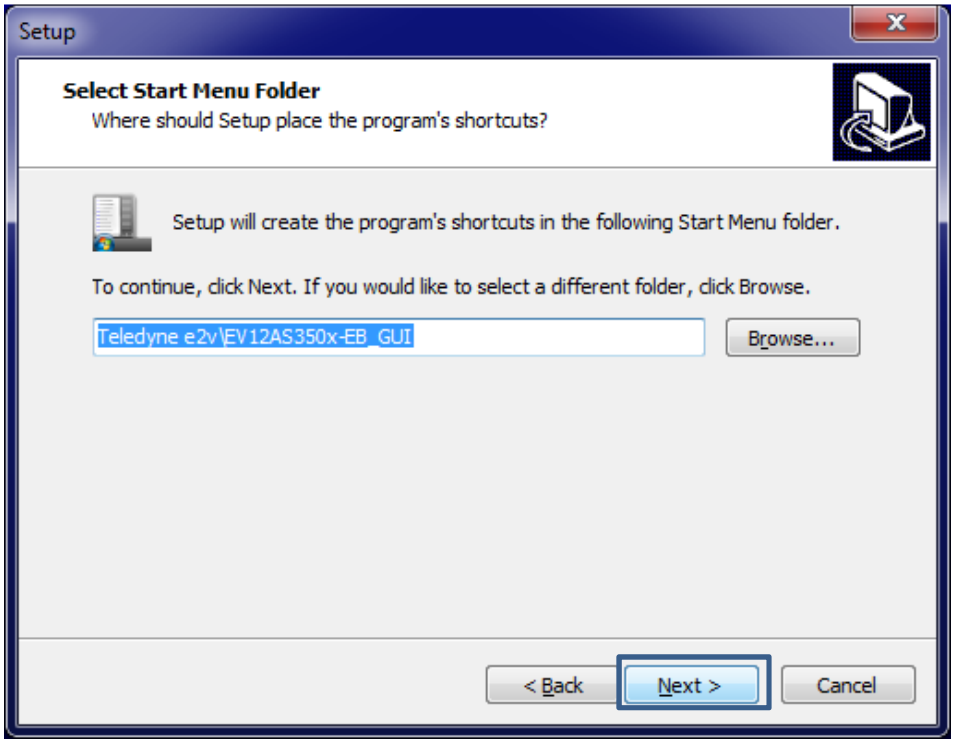
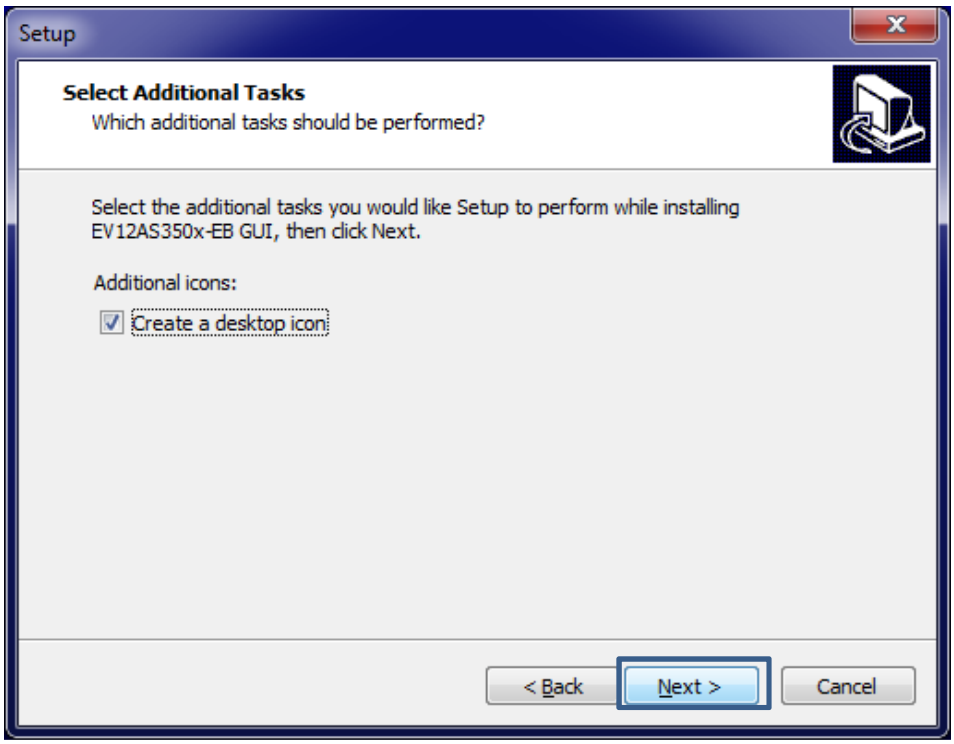


Figure 4-3. Evaluation Board EV12AS350x-EB GUI “Destination Directory” window





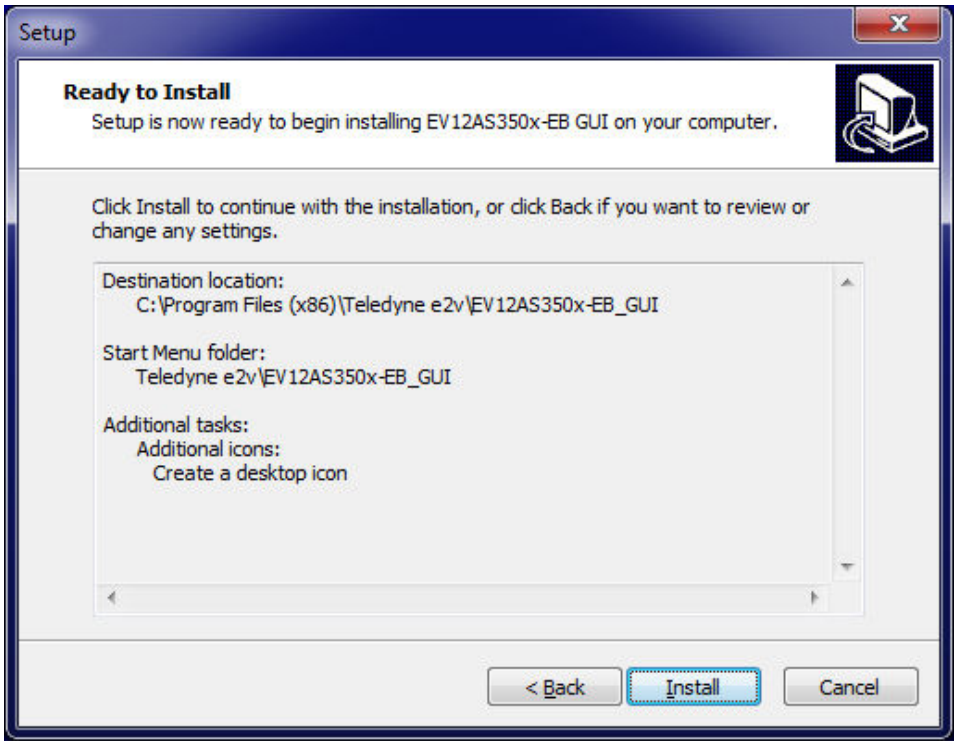
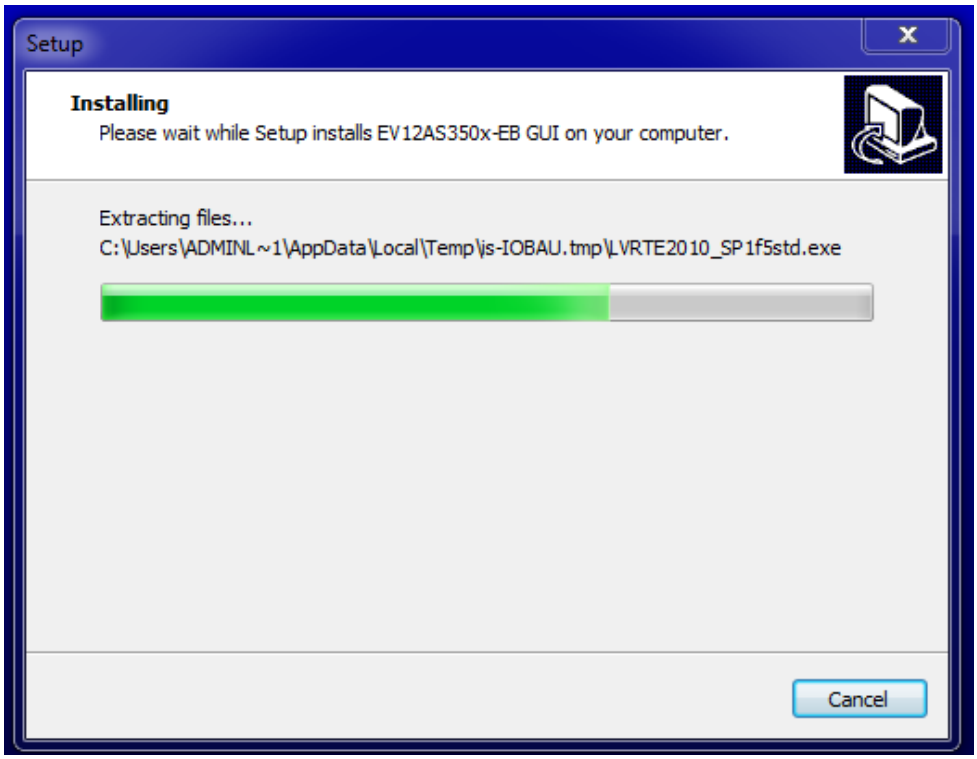


Figure 4-3. Evaluation Board EV12AS350x-EB GUI installation



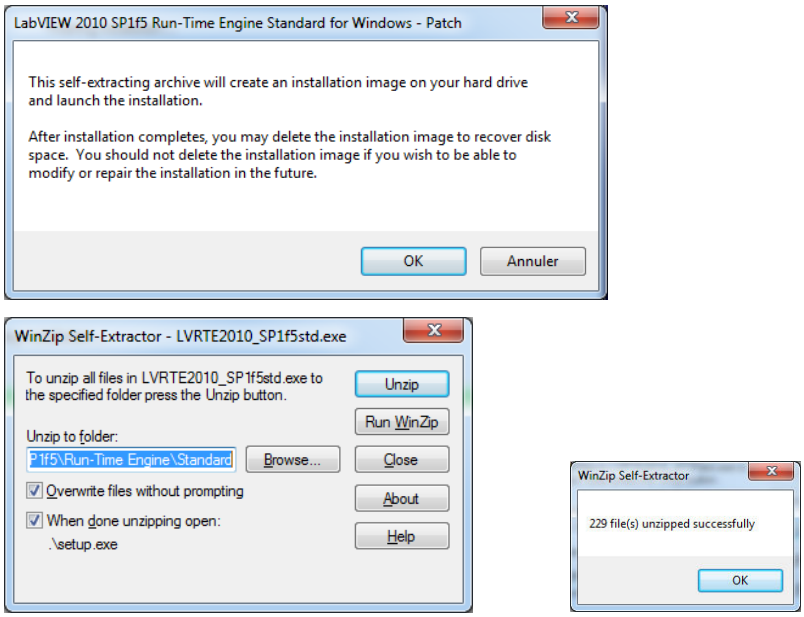


Figure 4-4. EV12AS350x Evaluation Board “Setup Wizard”

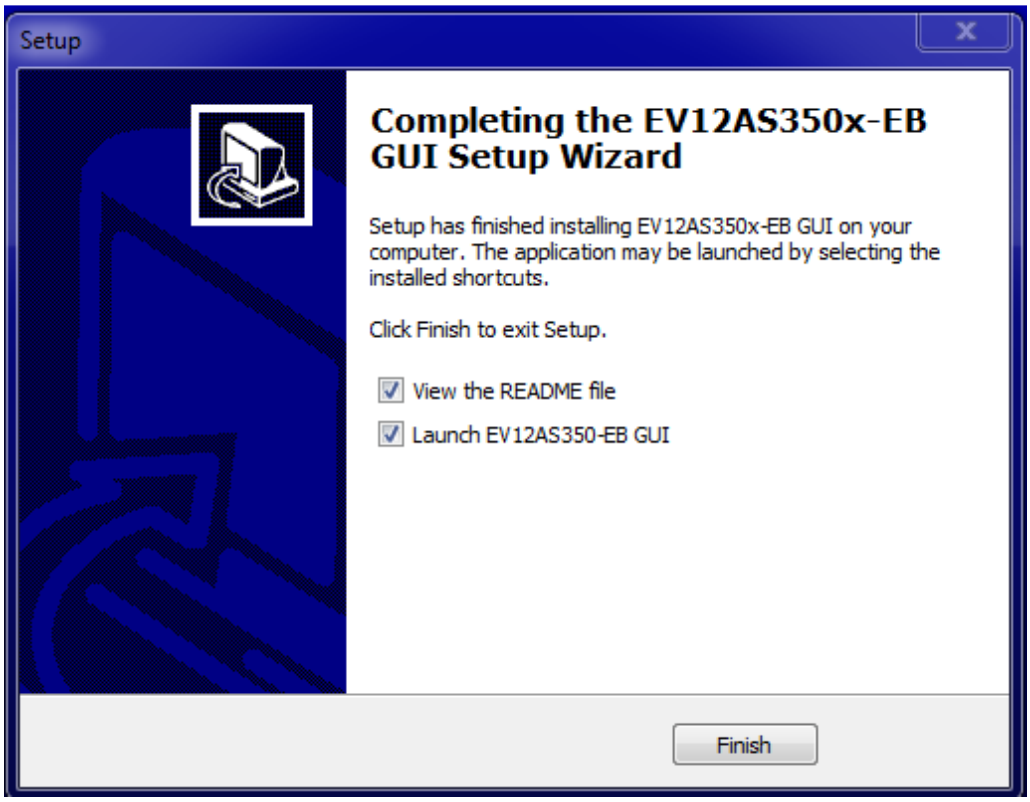


Figure 4-5 EV12AS350x Evaluation Board “README file”

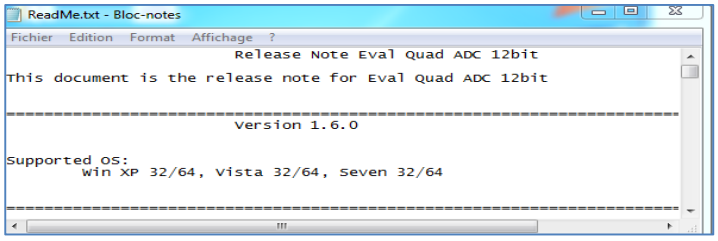
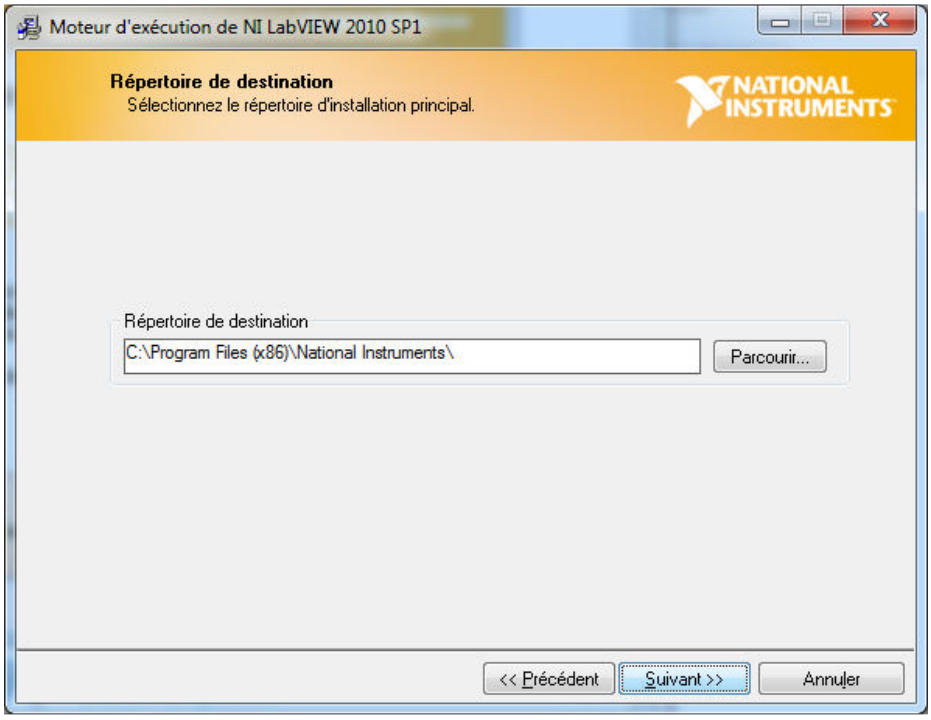
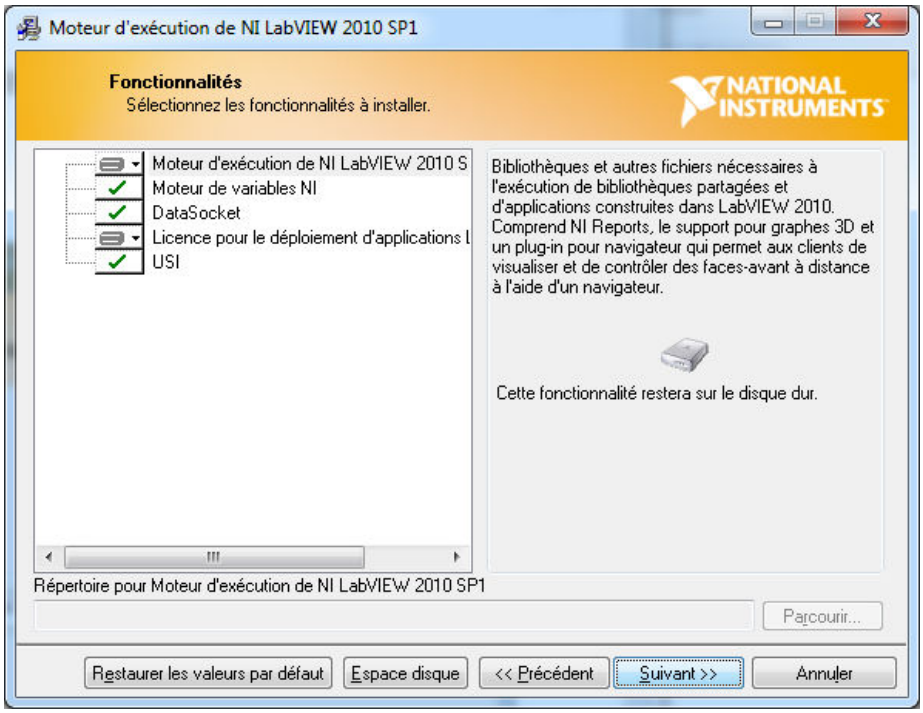


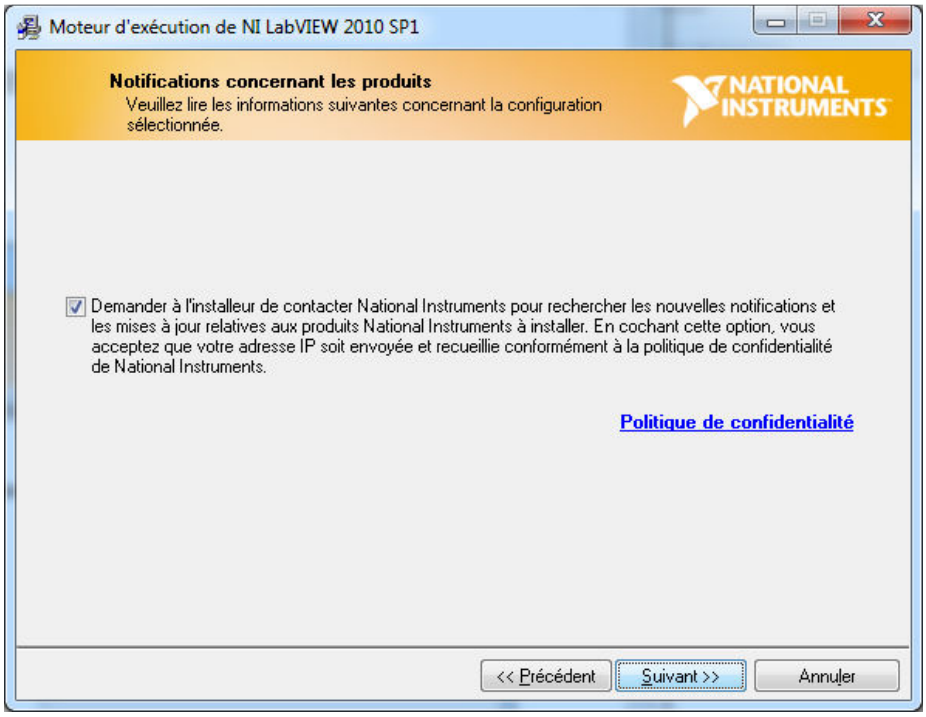
Figure 4-6 EV12AS350x Evaluation Board “Launch EV12AS350-EB GUI”

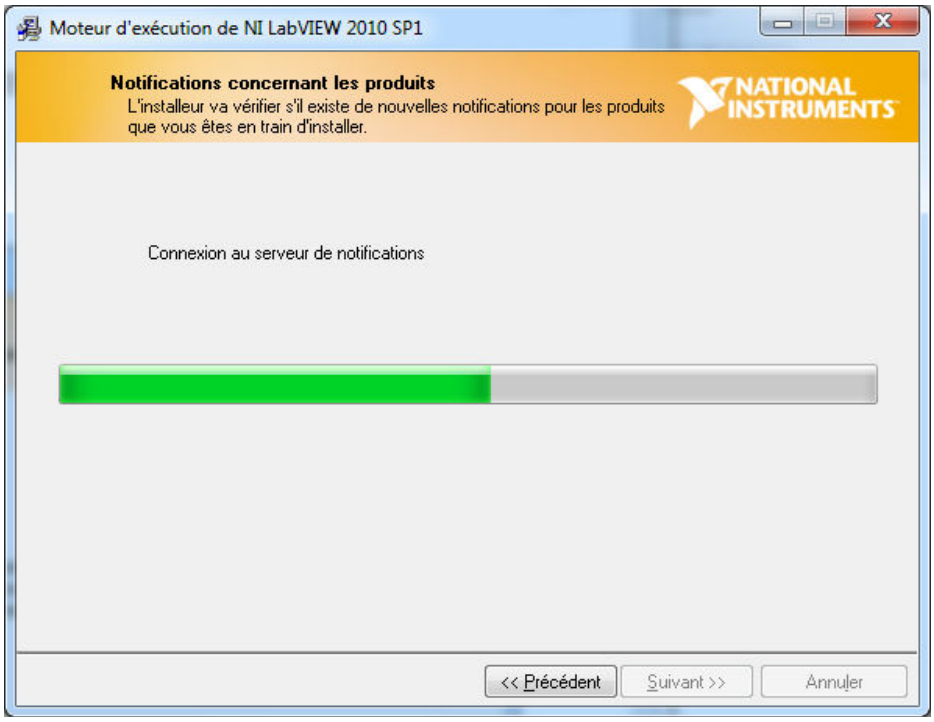
In the following example, LabView is installed on the computer. In this case, all installation steps can be skipped by clicking on ‘Cancel’.

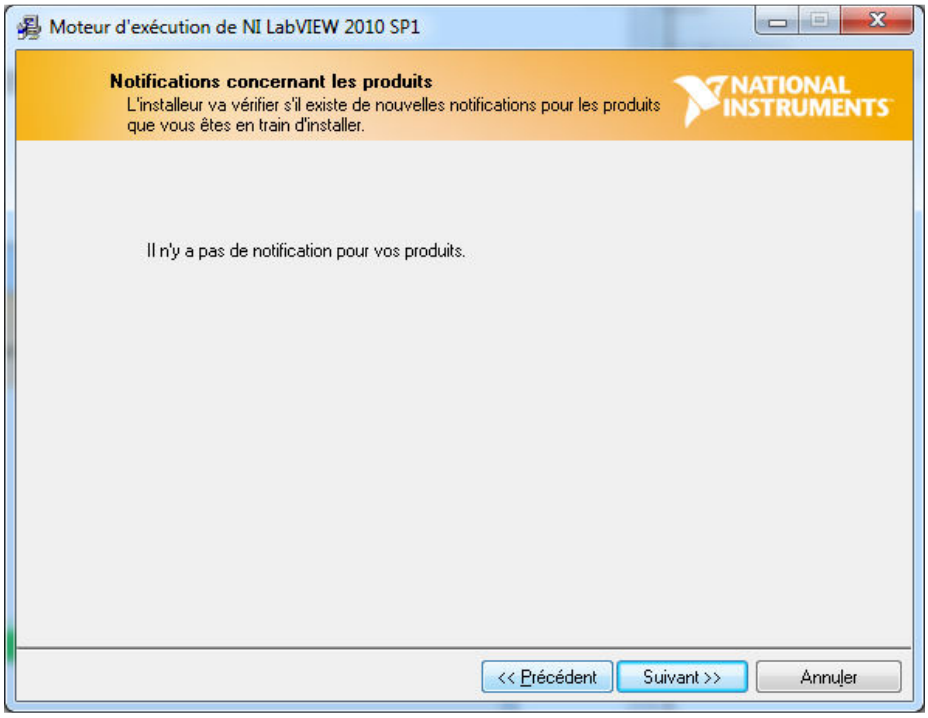
Otherwise, the user just needs to select the applications to be installed and click on ‘next’ until the end of the procedure.

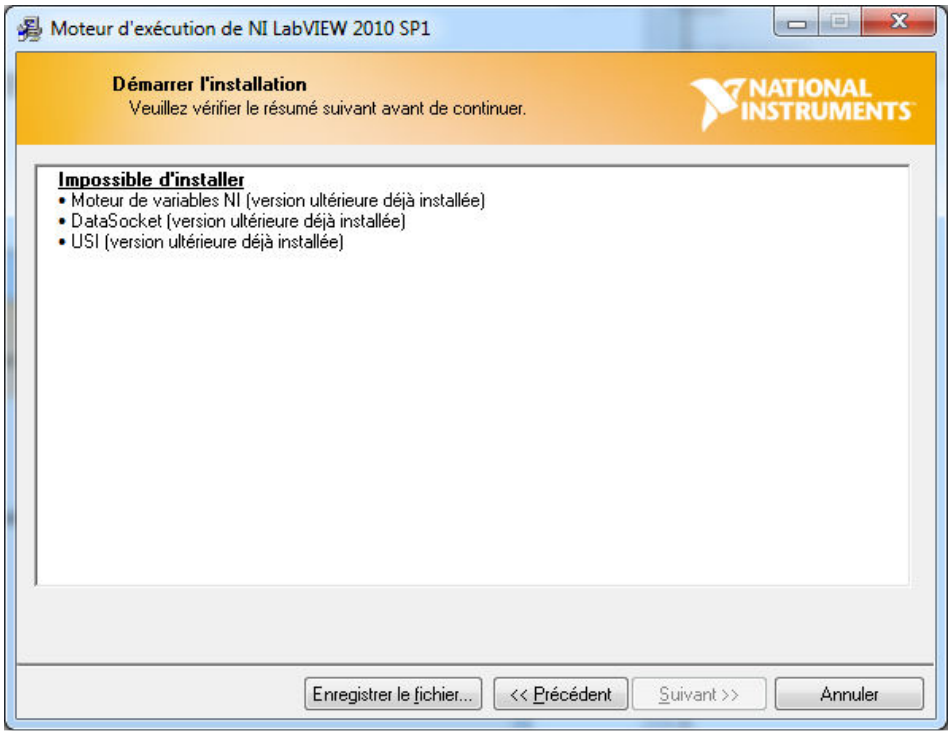


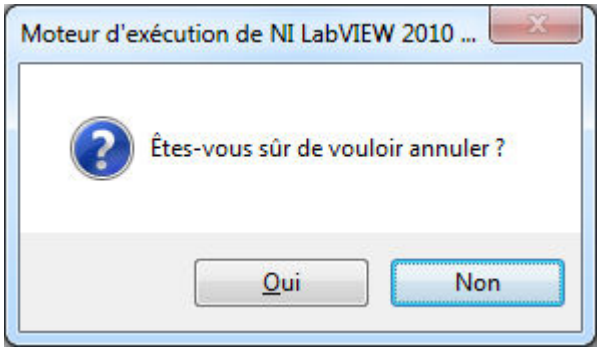

Moteur d'exécution de NI LabVIEW 2010 SP1
Fonctionnalités
Sélectionnez les fonctionnalités à installer.
NATIONAL INSTRUMENTS
Moteur d'exécution de NI LabVIEW 2010 S
Moteur de variables NI
DataSocket
Licence pour le déploiement d'applications l
USI
Bibliothèques et autres fichiers nécessaires à l'exécution de bibliothèques partagées et d'applications construites dans LabVIEW 2010. Comprend NI Reports, le support pour graphes 3D et un plug-in pour navigateur qui permet aux clients de visualiser et de contrôler des faces-avant à distance à l'aide d'un navigateur.
Cette fonctionnalité restera sur le disque dur.
Répertoire pour Moteur d'exécution de NI LabVIEW 2010 SP1
Parcourir...
Restaurer les valeurs par défaut
Espace disque
<< Précédent
Suivant >>
Annuler


Moteur d'exécution de NI LabVIEW 2010 SP1
Notifications concernant les produits
Veuillez lire les informations suivantes concernant la configuration sélectionnée.
NATIONAL INSTRUMENTS
Demander à l'installeur de contacter National Instruments pour rechercher les nouvelles notifications et les mises à jour relatives aux produits National Instruments à installer. En cochant cette option, vous acceptez que votre adresse IP soit envoyée et recueillie conformément à la politique de confidentialité de National Instruments.
Politique de confidentialité
<< Précédent
Suivant >>
Annuler


Moteur d'exécution de NI LabVIEW 2010 SP1
Notifications concernant les produits
L'installeur va vérifier s'il existe de nouvelles notifications pour les produits que vous êtes en train d'installer.
NATIONAL INSTRUMENTS
Connexion au serveur de notifications
<< Précédent
Suivant >>
Annuler

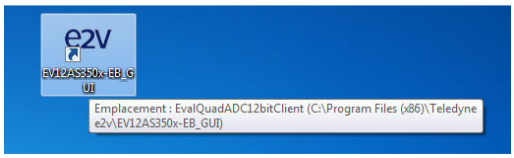

Moteur d'exécution de NI LabVIEW 2010 SP1
Notifications concernant les produits
L'installeur va vérifier s'il existe de nouvelles notifications pour les produits que vous êtes en train d'installer.
NATIONAL INSTRUMENTS
Il n'y a pas de notification pour vos produits.
<< Précédent
Suivant >>
Annuler





Installation is ready

Setup is now completed successfully. You can start application by double clicking on the following icon on your desktop.

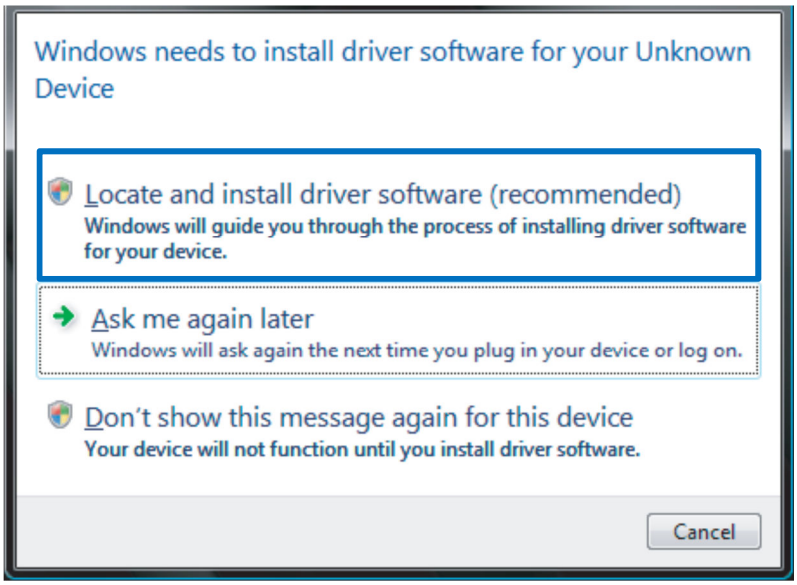


4.3 USB driver installation

After the installation, EV12AS350x Evaluation Board can be powered up and connected to PC with USB cable.
At the first connection a USB driver installation will be launched.

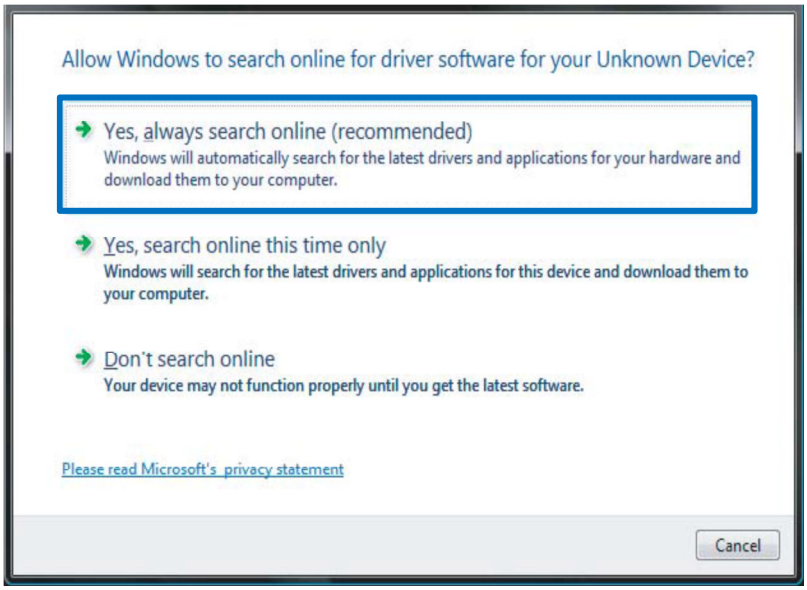
Warning: if the Evaluation Board is connected to another USB connector this installation must be re-started.
The installation is normally fully automatic. If it is not launched automatically, please proceed as described below.
The window shown in Figure 4-7 will be displayed.

Figure 4-7. Install Driver Software



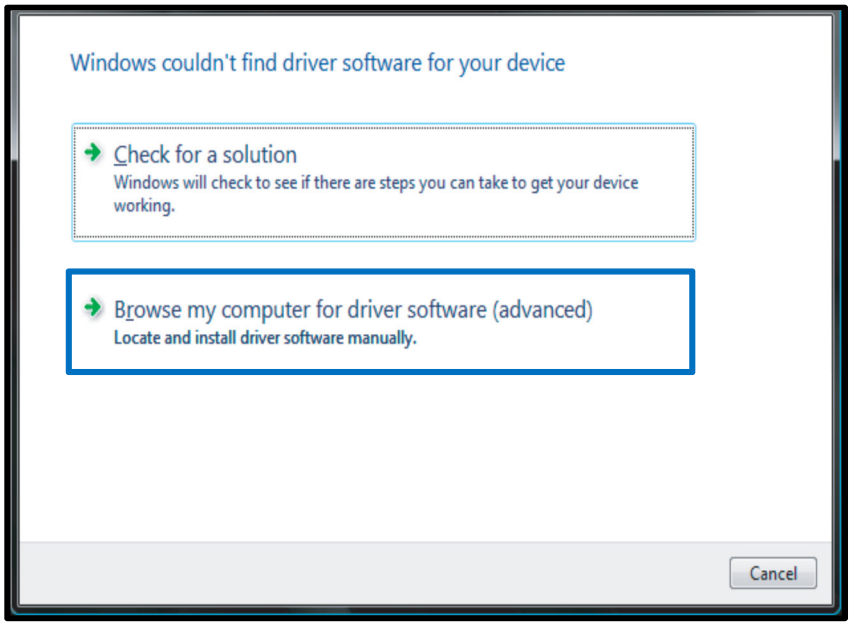
Please choose: Locate and install driver software (recommended)

Figure 4-8. Allow Windows to Search Driver



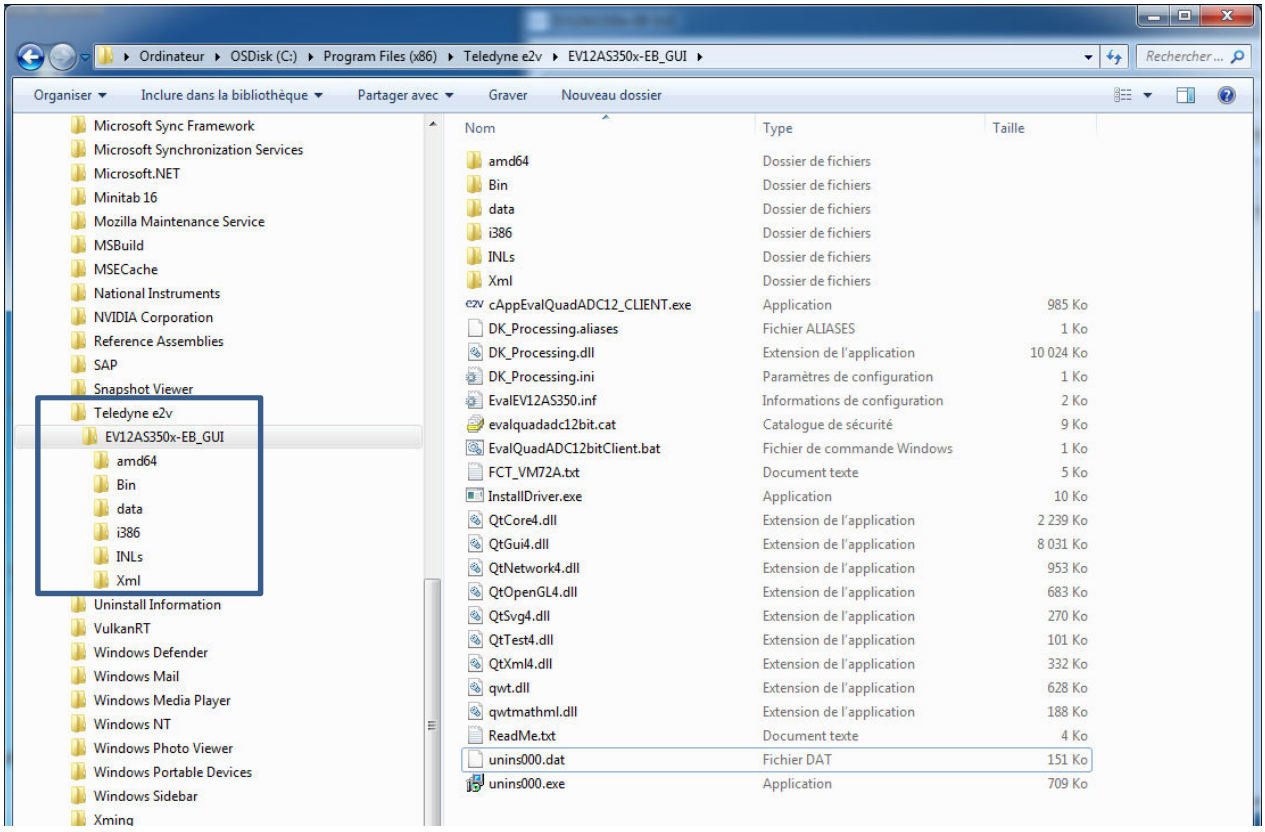
Please choose: Yes, always search online (recommended)

Figure 4-9. Browse the Driver Software



Please choose: Browse my computer for driver software (advanced)

Figure 4-10. Choose the Folder



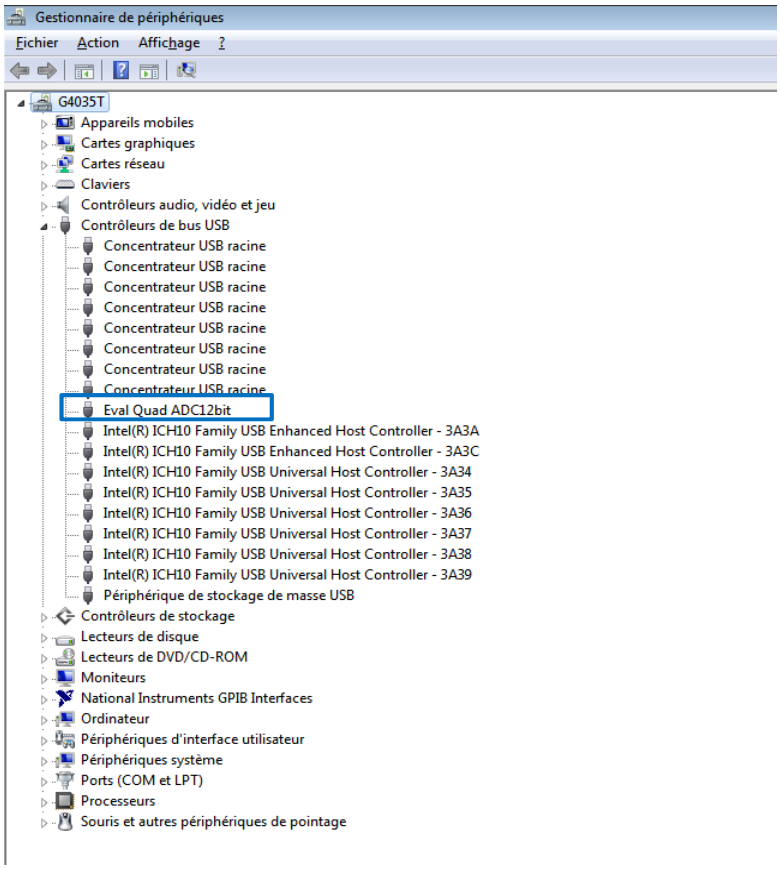
Select C:\Program Files (x86)\Teledyne e2v\EV12AS350x-EB_GUI

Figure 4-11. Warning: Installation

Please choose: Install the driver software anyway.

Please wait during the data transfer.

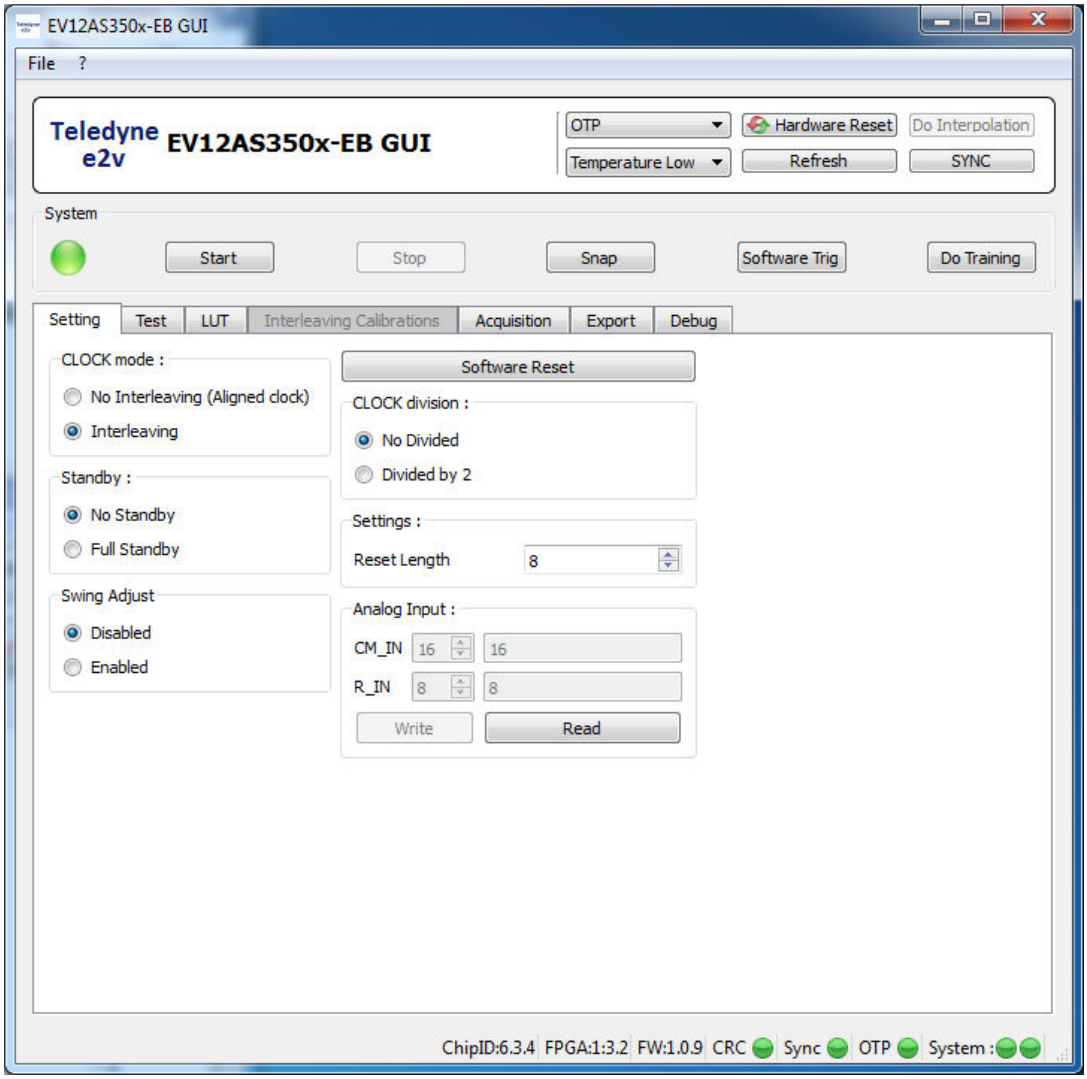
Figure 4-12. END of New Driver Installation



The new driver has been installed.

After the installation, the interface can be launched with the following file:
C:\Program Files (x86)\Teledyne e2v\EV12AS350x-EB_GUI\EvalQuadADC12bitClient.bat.
The window shown in Figure 4-13 will be displayed.

Figure 4-13. EV12AS350x-EB Graphical User Interface (GUI)



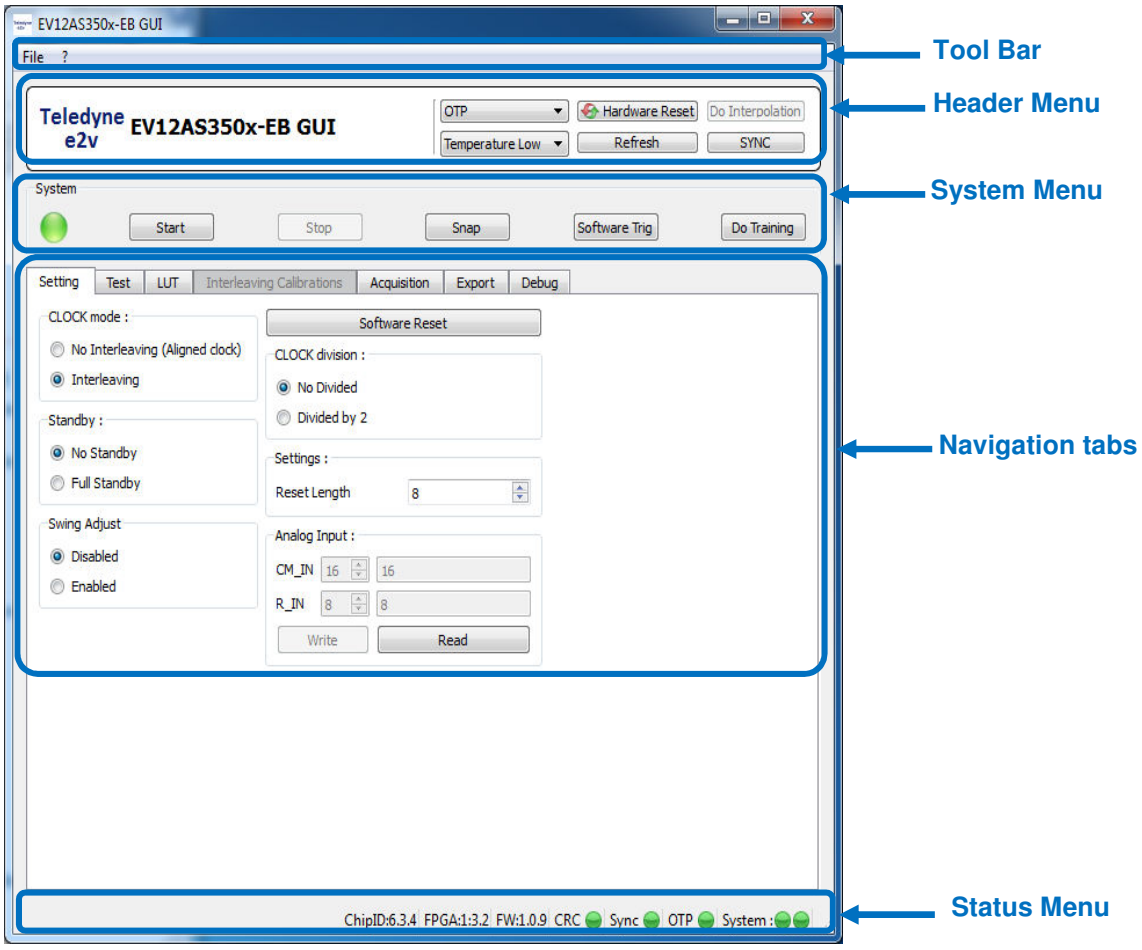
4.4 GUI Overview

The EV12AS350x-EB GUI software included with the Evaluation Board provides a Graphical User Interface to configure the ADC.
Push buttons, popup menus and capture windows allow easy configuration of the ADC, data acquisition and data exportation.

The User Interface window is made of different menus and tabs that are described in the figure 4-14 below.

- Tool bar
- Header menu
- System menu
- Several navigation tabs
  - Settings
  - Test
  - LUT
  - Interleaving calibrations
  - Acquisition
  - Export
  - Debug
- Status Menu

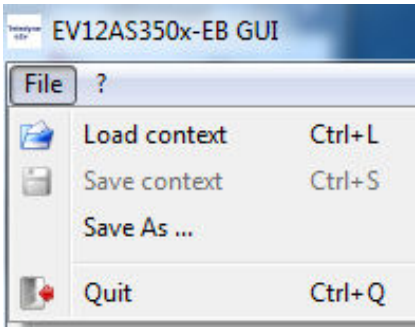
Figure 4-14. EV12AS350x-EB Graphical User Interface (GUI)



4.4.1 Tool bar description

The “**File**” Menu provides the following choices:

Figure 4-15. EV12AS350x-EB File Menu

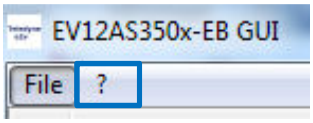


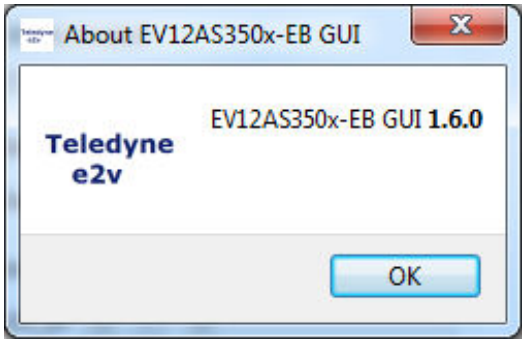
- “**Load context**”: used to load an existing context file (file.ctx) and then,modify ADC calibrations. (ADC calibration context is useful in the only case when the user wants to apply its own calibrations via the SPI mode).
- “**Save As…**”: used to save a context file of ADC calibrations in giving a name to the context file (file.ctx).
- “**Save context**”: used to save a context file (file.ctx) of ADC calibrations (accessible once a file named as already been given using the “Save As…” option).
- “**Quit**”: used to close the Graphical User Interface window.

A context file saves all the configurations accessible via the GUI (Settings, Acquisition…) and can be used to reuse a given configuration without changing manually all the configurations.

The « **?** » Menu enables to display the version of the GUI software.

Figure 4-16. EV12AS350x-EB “?” Menu





4.4.2 Header Menu description

Figure 4-17. User Interface Header Menu

The Header Menu enables:

- ADC initialization via a "**SYNC**": pressing this button generates a SYNC pulse on the ADC (See chapter 3.3.1)
- "**Hardware Reset**"**:** pressing this button generates a reset signal on the SPI of ADC. All changes made on SPI values are erased and SPI values come back to their default values. Pressing this button also switch ADC in OTP mode (default mode)
- The selection between "**OTP**" or "**SPI**" register values (OTP_SPI_SEL register within ADC)
- The configuration of calibrations in OTP mode: choice between one of the two sets of calibration ("**Temperature Low**" or "**Temperature High**")
- "**Do interpolation**": ADC calibrations are interpolated at the temperature of use (in SPI mode)
- "**Refresh**"**:** the GUI is refreshed according to ADC registers

For more information about ADC calibrations (OTP, SPI, Do interpolation …) please refer to chapter 4.5.4.

When OTP is selected:

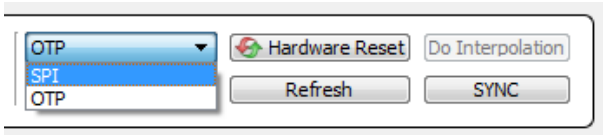
- The two sets of calibration ("**Temperature High**" or "**Temperature Low**") is accessible
- The process of calibrations interpolation (via "**Do interpolation**" procedure) is not accessible

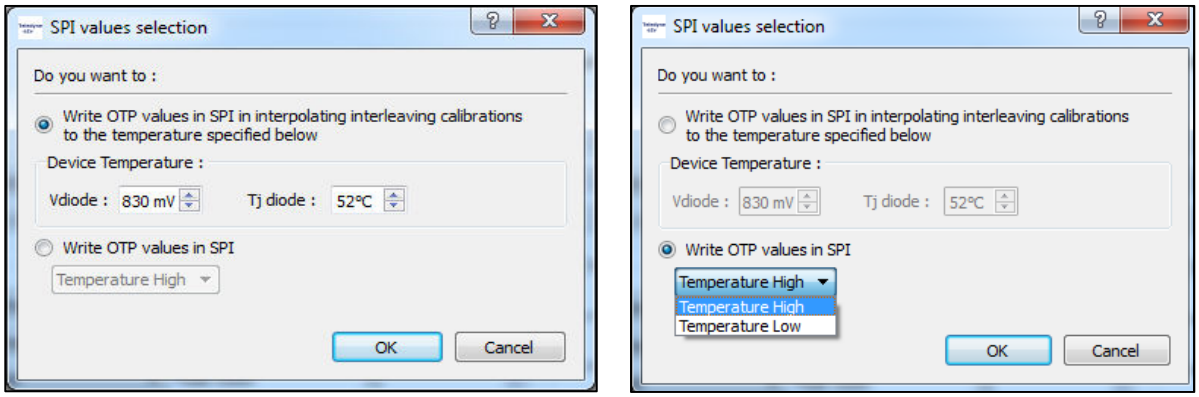
Note: R_IN and CM_IN values (Settings tab) are the values written within OTP and cannot be modified in OTP mode.

When SPI is selected:

- The two sets of calibrations (Temperature Low or Temperature High) are no more accessible
- Pop-up window of Figure 4-18 proposes two choices:
  - Launch a "**Do interpolation**" procedure at the temperature of use. See chapter 0 for more information about calibration interpolation
  - Write OTP calibration values within the SPI registers: The user is asked to select which OTP values need to be written within SPI (OTP Temperature Low or OTP Temperature High)
- The "**Do Interpolation**" procedure can be launched at any time in clicking on "**Do interpolation**" button

Figure 4-18. SPI values selection pop-up window



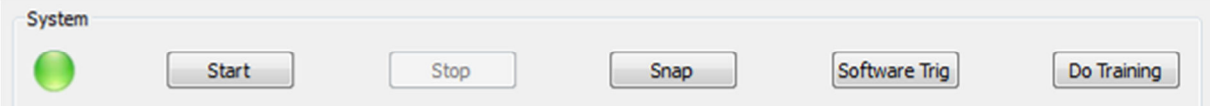


Note: When SPI mode is selected, R_IN and CM_IN values (defined in the Settings tab) are the values from SPI (no more OTP values).

- R_IN and CM_IN have their SPI default values after a hardware or software reset
- R_IN and CM_IN have their previous SPI values if no reset has been done (for instance, if R_IN is modified to value 12, switching to OTP mode will cause the R_IN value to switch to the value defined in OTP. When coming back to SPI mode, R_IN value will come back at the value 12 even if the SPI default value is 8).

4.4.3 System Menu description

Figure 4-19. User Interface System Menu



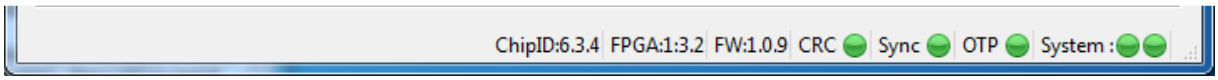
The System Menu enables:

- ADC synchronization with FPGA. Pressing the "**Do Training**" button launches the procedure described in chapter 6.4.
- **Start:** enables to start a continuous acquisition of ADC data output by the FPGA until "Stop" button is pressed.
- **Stop:** Stop an acquisition when a continuous acquisition has been launched via the "Start" button.
- **Snap:** Press this button to start a single acquisition.
- **Software Trig:** Press this button to start a single acquisition when GUI is in trigger mode.

The LED on the left side of the System Menu interface switches to red color when FPGA is currently doing an acquisition. When acquisition is finished, LED switches to green color.

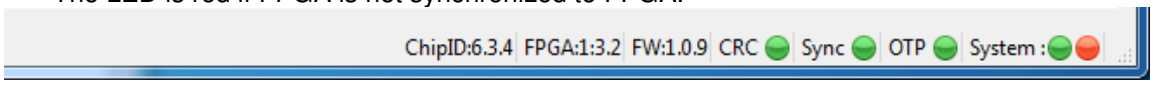
4.4.4 Status Menu description

Figure 4-20. User Interface Status Menu

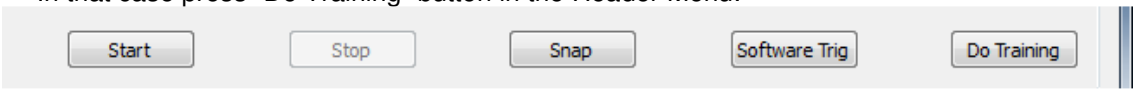


The Status Menu provides information about:

- **Chip ID:** identification of the chip revision: must be 6.3.4 for P/N EV12AS350BTPY
- **FPGA version code**
- **Firmware version code**
- **CRC status:** After each power-up, the value of ADC MASTER_STATUS register is read in order to verify that all OTP CRC are successful. The LED is green if all CRC are successful, red otherwise.
- **SYNC status:** The LED is green if the ADC synchronization is successful. Otherwise, the LED is red.
- **OTP status:** After each power-up, the value of ADC MASTER_STATUS register is read in order to verify that OTP_STATUS is ready and available. The LED is green if OTP is ready and available, red if not ready.
- **System status:**
  - The first LED is green if the PLL within FPGA are OK. In case of issue with PLL, LED is red.
  - The second LED is green if the FPGA is correctly synchronized to the ADC.
    The LED is red if FPGA is not synchronized to FPGA.



In that case press “Do Training” button in the Header Menu.



4.4.5 Navigation tabs description

Refer to chap 4.5 below.
There are the following tabs:

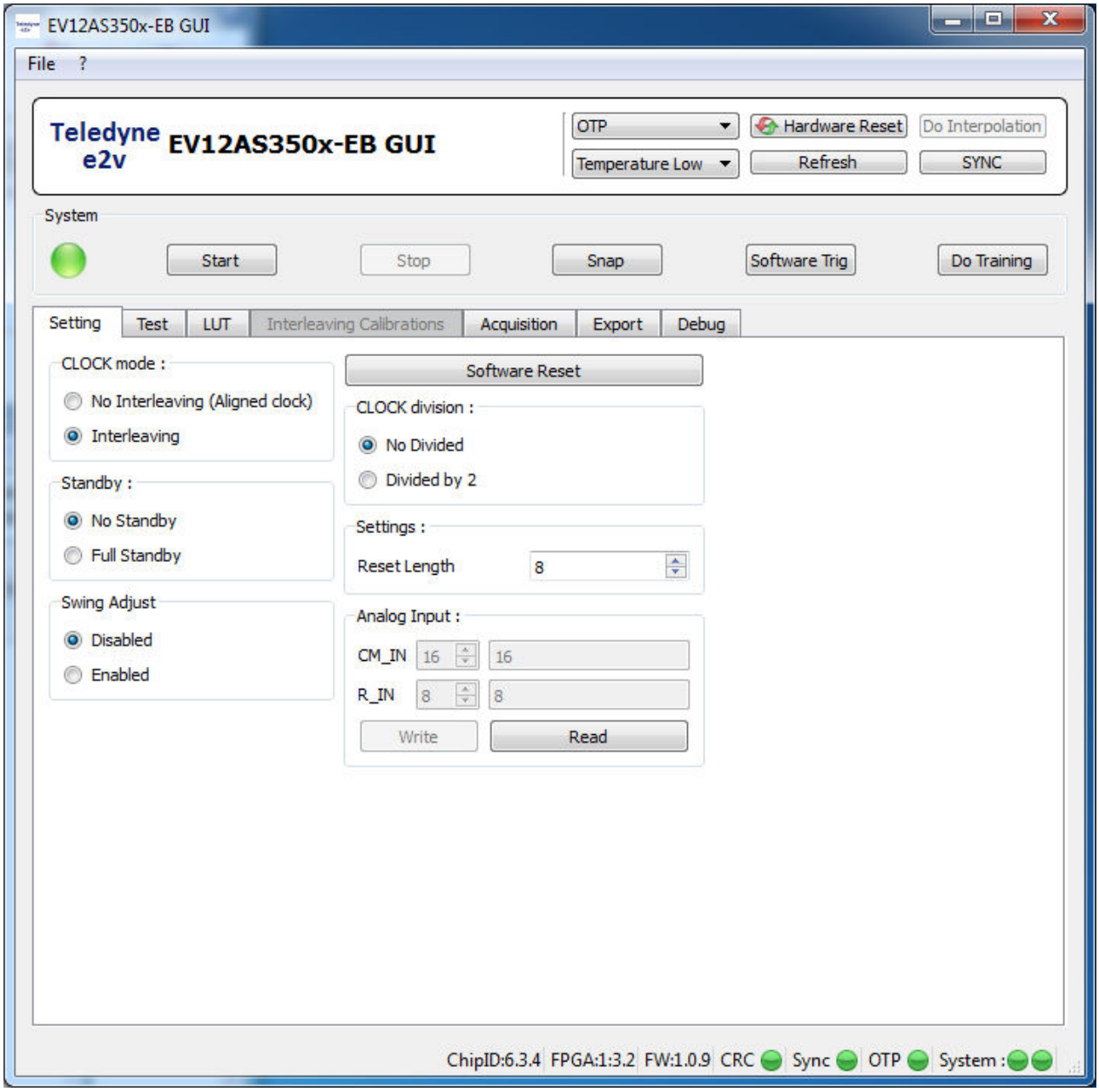
- **Settings:** to configure ADC settings (clock mode, clock division, Standby, Swing Adjust, Analog input common mode and impedance)
- **Test:** to activate ADC test modes (Ramp, Flash and PRBS)
- **LUT:** to apply a Look-Up Table
- **Interleaving calibrations:** if the user wants to define its own interleaving calibrations (in SPI mode only)
- **Acquisition:** to configure the acquisition of ADC output data (4 cores interleaved or aligned with/without averaging, FFT configuration)
- **Export:** to export acquisition data into a file
- **Debug:** to write or read ADC internal registers via its address (advanced mode for debug purpose)

4.5 Operating modes

4.5.1 Settings

This tab is dedicated to the configuration of EV12AS350 ADC.

Figure 4-21 User Interface Settings tab



4.5.1.1. Software reset

Pressing the "**Software Reset**" button set all ADC registers to their default values.

4.5.1.2. CLOCK mode

Two modes are possible:

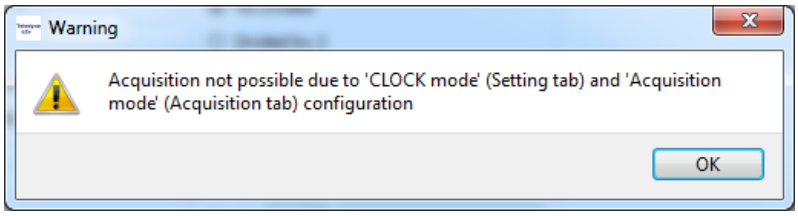
- **No interleaving (Aligned clock)**: Data ready of the ADC cores are aligned.
- **Interleaving:** Data Ready of the ADC cores are delayed by T/4.

This setting corresponds to the ADC register CLK_MODE_SEL bit 0.

Pop-up window of Figure 4-22 below appears in case of selection of the 3 unauthorized configurations listed below:

- CLOCK mode = "**No interleaving"** with "**4 Cores Interleaved**" selection within Acquisition tab.
- CLOCK mode = "**Interleaving"** with "**4 Cores aligned without averaging**" selection within Acquisition tab.
- CLOCK mode = "**Interleaving"** with "**4 Cores aligned with averaging**" selection within Acquisition tab.

Figure 4-22. Pop-up window in case of Clock mode incompatibility



4.5.1.3. Standby

Two modes are possible:

- No Standby : This is the default mode
- Full Standby : Power down mode (for each channel)

This setting corresponds to the ADC register STDBY

4.5.1.4. CLOCK division

Two modes are possible:

- **No divided**: This is the default mode. Each core of EV12AS350 ADC operates at F/4, F being the frequency of clock applied to the EV12AS350 ADC.
- **Divided by 2:** each core of EV12AS350 operates at F/8, F being the frequency of clock applied to the EV12AS350 ADC.

This setting corresponds to the ADC register CLK_MODE_SEL bit 1.

4.5.1.5. Reset length

This function enables to modify the delay of restart of Data Ready after a SYNC.
Reset length is expressed in terms of number of internal clock cycles. GUI value is expressed in decimal.

- Default value is 8.
- Minimum value is 8 internal clock cycles
- Maximum value is 63 internal clock cycles

This setting corresponds to the ADC register RST_LENGTH.

4.5.1.6. Swing Adjust

Two modes are possible:

- **Disabled**: data output swing is not reduced (LVDS output data).
- **Enabled:** this is the default mode of the GUI. Data output swing is reduced

This setting corresponds to the ADC register FULL_SWING_EN.

4.5.1.7. Analog Input

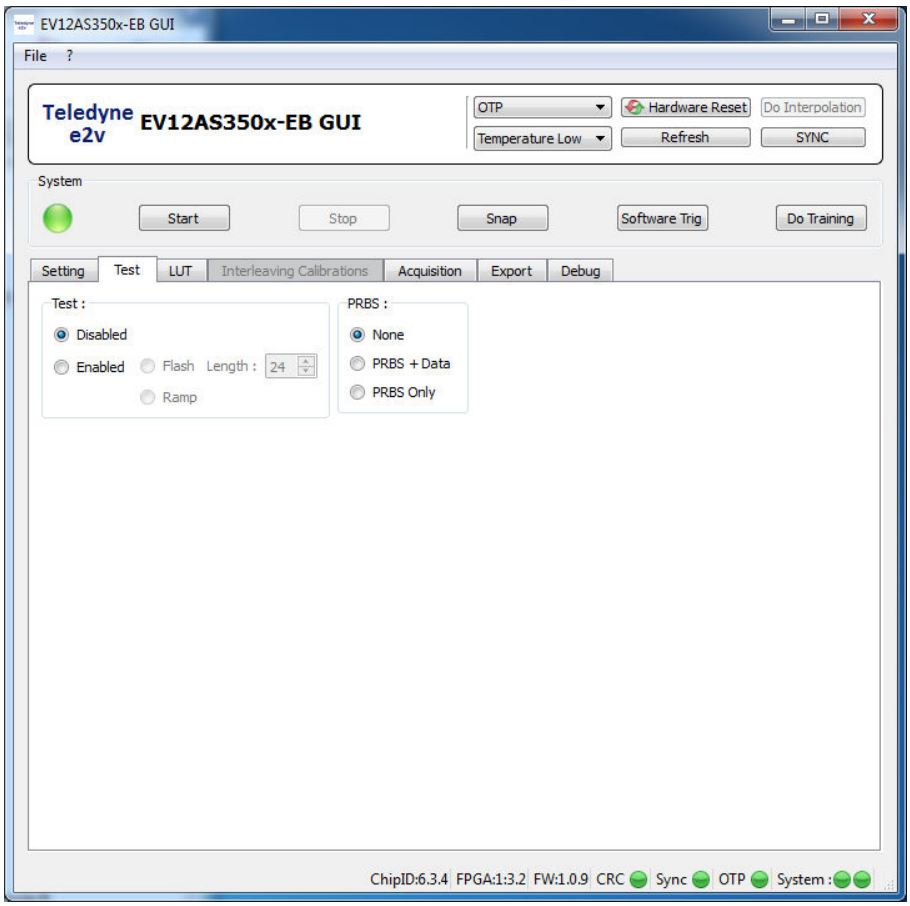
It is possible to modify analog input common mode (**CM_IN**) and analog input impedance (**R_IN**) if SPI is selected in the Header Menu (these settings are not accessible in OTP mode).
These 2 settings correspond to ADC registers R_IN and CM_IN.

Note: If R_IN or CM_IN values are modified (necessarily in SPI mode), and if the user comes back to OTP mode, R_IN and CM_IN will come back to OTP values. Then, if the user switches again to SPI mode, R_IN and CM_IN will recover the previous values when ADC was in SPI mode.

4.5.2 Test

This tab is dedicated to the configuration of EV12AS350 ADC test modes (Flash, Ramp and PRBS).

Figure 4-23. User Interface Test tab



4.5.2.1. Test

Two modes are possible:

- **Disabled:** this is the default mode. Test mode is not active. ADC is in normal mode.
- **Enabled:** test mode is activated. Ramp and Flash are accessible.

This setting corresponds to the ADC register TEST_MODE.

When Test is “Enabled”, before selecting Flash or Ramp mode, SYNC button (Header Menu) needs to be pressed. Then Flash or Ramp mode can be selected.

Flash mode can be selected and the flash length can be adjusted from 2 to 60 internal clock cycles (GUI values are displayed in decimal). This setting corresponds to the ADC register FLASH_LENGTH. Default value is 24 internal clock cycles.
When Test is enabled, Ramp mode can be selected and a ramp is generated at the output of each ADC core.

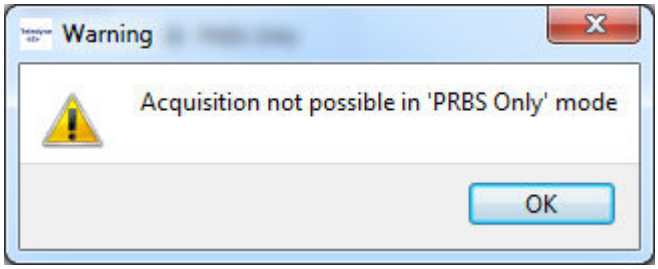
Note: A “Do training procedure” followed by a “SYNC” is mandatory after selecting Ramp or Flash mode in order to re-synchronize EV12AS350 ADC with FPGA.

4.5.2.2. PRBS

A Pseudo Random Bit Sequence (PRBS) can be added on ADC output (encoding within ADC).
Note: It is not necessary to have TEST “Enabled” to activate PRS mode.

- By default there is no PRBS encoding within ADC: “**None**” selection
- It is possible to consider a PRBS encoding on ADC output data: “**PRBS+Data**” selection. In that case, the PRBS decoding is done within FPGA.
- A PRBS sequence can be selected as a test mode: “**PRBS Only**” selection. This mode is not supported by the Evaluation Board (no acquisition in this mode). As a consequence, a pop-up window appears as shown on figure 4-24.

Figure 4-24. Pop-up window “Acquisition not possible in ‘PRBS Only’ mode”

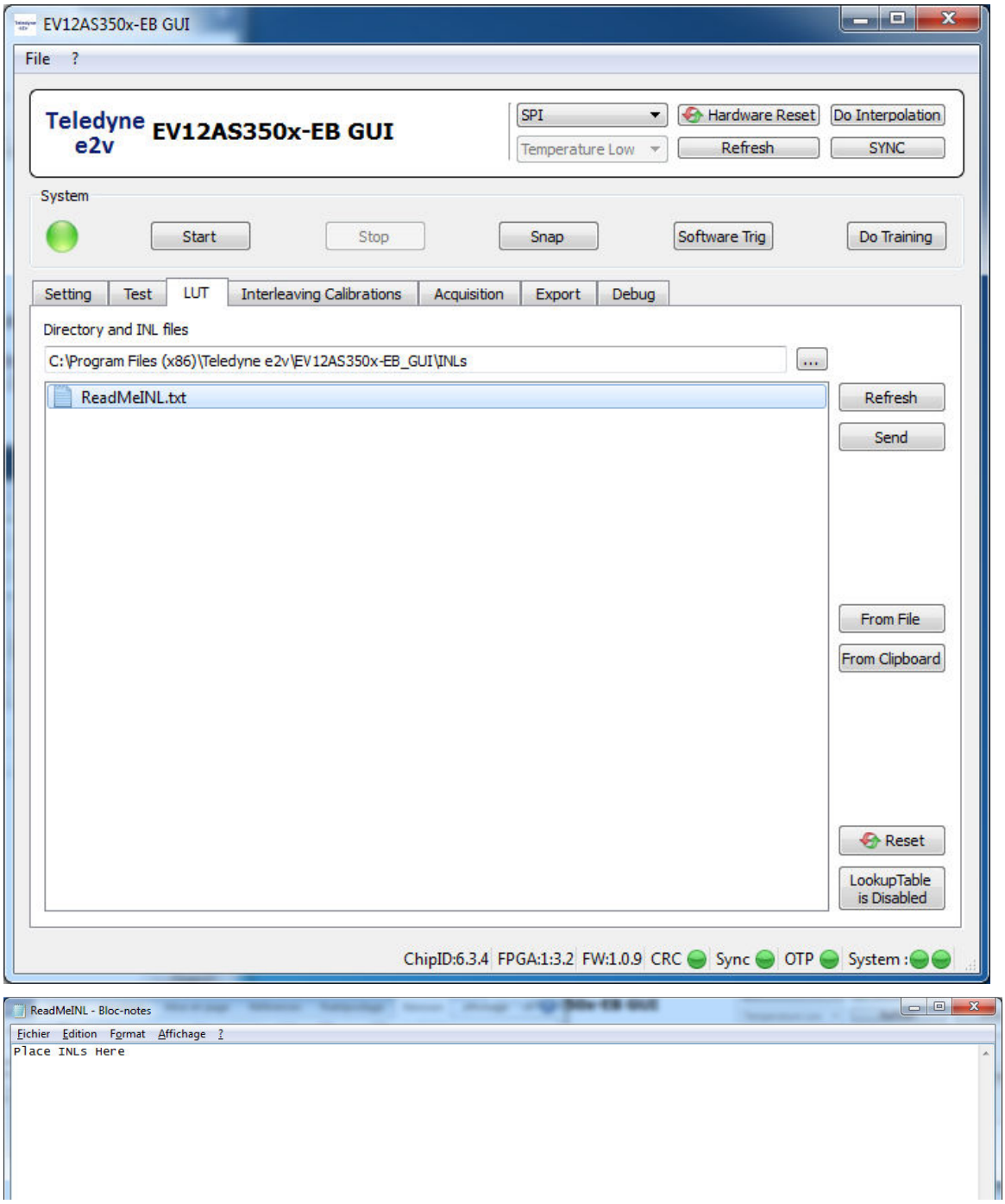


4.5.3 LUT

This tab enables to apply a Look Up Table (LUT) to the ADC.
A LUT can be used to correct the static non-linearity of the ADC.

The principle of LUT file is described below.
When doing an acquisition of code N, this code is modified by the value of the LUT for code N (LUT value for code N is subtracted to code N).
For instance, if the LUT value for code 3208 is 1.536 LSB, when doing the acquisition of code 3208, the value to be considered will be 3208-1.536 = 3206.464 which will be truncated to 3206 (12 bit).

Figure 4-25. LUT tab



4.5.3.1. LUT file format

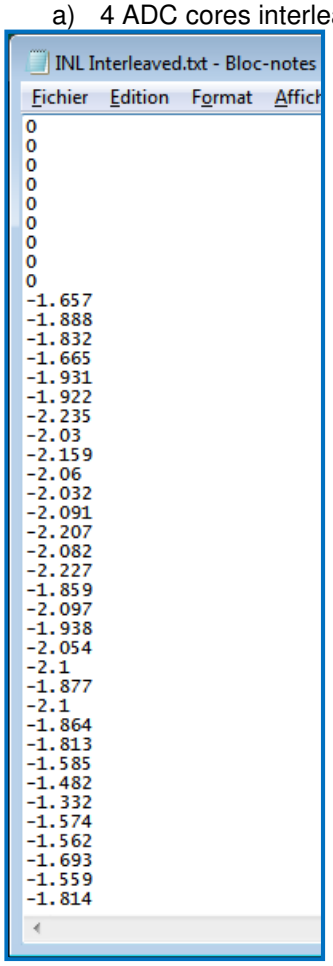
A LUT file can be created by saving ADC INL characteristics in a file that will be used as a correction table. See chapter 4.5.6 to see how to export acquisition data.

Note: ADC INL files are exported in Excel format. In order to be used as a LUT file, it needs to be saved as a text file as shown on figure 4-26. **Be careful, the order of ADC cores is A, B, C, D in the exported INL file and needs to be A, C, B, D in the LUT file!**

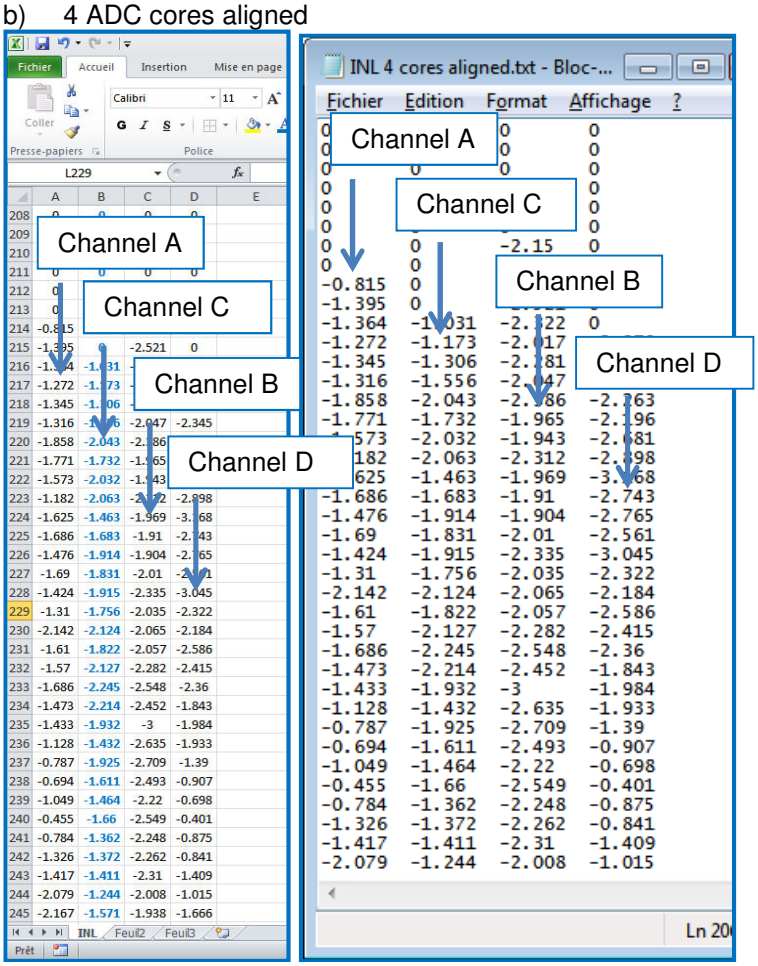
LUT files are text files (file.txt) and their format change if 4 ADC Cores are aligned or interleaved

Figure 4-26. LUT file format

a) 4 ADC cores interleaved



b) 4 ADC cores aligned



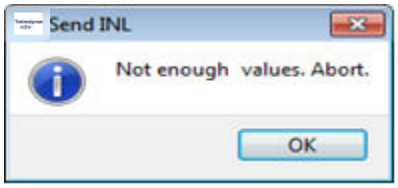
If 4 ADC cores are interleaved, the LUT file contains only one column corresponding to the INL characteristics of the 4 ADC cores interleaved.

If 4 ADC cores are aligned, the LUT file contains 4 columns : each column corresponds to the INL characteristics of an ADC Core :

- 1st column is the LUT for ADC Core A
- 2nd column is the LUT for ADC Core C
- 3rd column is the LUT for ADC Core B
- 4th column is the LUT for ADC Core D

The values in each column are written in decimal and correspond to the correction to be applied on each acquisition.
Each LUT file needs to contains 4096 lines. If the LUT does not include 4096 lines, the following error message is displayed:

Figure 4-27. LUT error message



It is possible to select the directory where LUT files are available by clicking on the button  on the right side of the field “Directory and INL files”
Button “**Refresh**” enables to refresh the display of all available LUT files (file.txt) in the selected directory.

Note: The refresh is done automatically when a file is written within the selected folder.

4.5.3.2. LUT file selection

The LUT can be dowloaded from a file or from clipboard:

a) LUT selection from a file

- Select the directory in which the desired LUT file is saved by clicking on the button  on the right side of the field “**Directory and INL files**”
- Select the desired LUT file

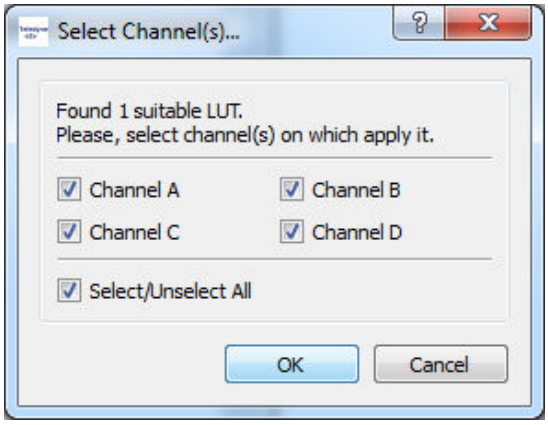
Whatever the method used to select the LUT file is, the GUI will be executed differently depending on the format of the LUT file:

1. If the LUT file contains 4 columns, it directly downloads the LUT into the FPGA. Each column will be applied to the associated ADC Core (case where 4 ADC cores are aligned).
   A message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. 

   The “**Send INL Done**” message disappears after a few seconds.

2. If the LUT contains 1 column, the pop-up window of figure 4-28 appears and asks the user on which channel the LUT has to be applied (case where 4 ADC cores are interleaved).

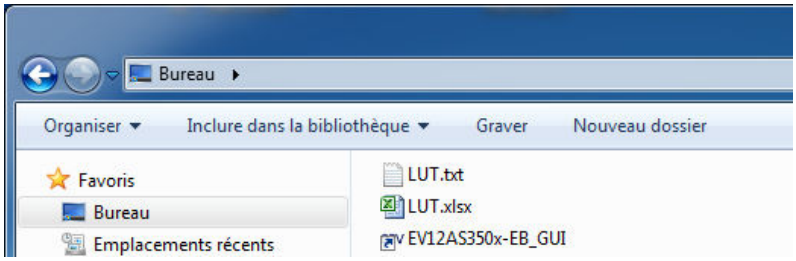
Figure 4-28 LUT channel selection



Select all channels if 4 ADC cores are interleaved.
Then a message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. Send INL Done
The "**Send INL Done**" message disappears after a few seconds.

Note: This selection can also be done by clicking on the "**From File**" button: From File
Clicking on the "**From File**" button opens an explorer window to select your directory and your LUT file as shown on figure 4-29 below.
Once the LUT file is selected it is directly sent to the FPGA (No need to click on "Send" Button).

Figure 4-29. LUT explorer window



b) LUT selection From Clipboard

A LUT can be downloaded from clipboard with the following procedure:

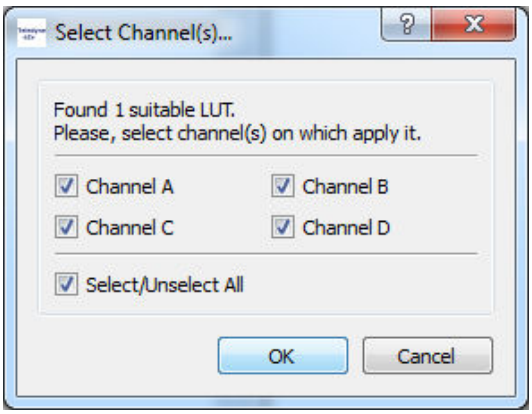
- Open the file including the LUT to be applied
- Select the LUT considered column(s)
- Copy the LUT considered column(s)
- Then click on the "**From Clipboard**" button
  From Clipboard
- The data previously copied has been downloaded in GUI.

Whatever the method used to select the LUT file is, clicking on the "**Send**" button has the following effect:

1. If the LUT file contains 4 columns, it directly downloads the LUT into the FPGA. Each column will be applied to each ADC Core (case where 4 ADC cores are aligned).
   A message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. Send INL Done
   The "**Send INL Done**" message disappears after a few seconds.

2. If the LUT contains 1 column, the pop-up window of figure 4-30 appears to ask the user on which channel the LUT has to be applied (case where 4 ADC cores are interleaved).

Figure 4-30. LUT channel selection



Select all channels if 4 ADC cores are interleaved.
Then a message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. Send INL Done
The "**Send INL Done**" message disappears after a few seconds.

4.5.3.3. Enabling LUT corrections

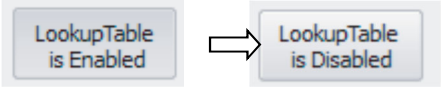
Click on "**Lookup Table is Disabled**" button in order to get the display "**Lookup Table is Enabled**"

The next acquisitions will now apply LUT corrections until LUT is disabled.

4.5.3.4. Stopping LUT corrections

There are two ways of stopping LUT corrections:

1. By clicking on "**Lookup Table is Enabled**" button
   LUT corrections can be stopped when clicking on the "**Lookup Table is Enabled**" button which then displays the text "**Lookup Table is Disabled**"

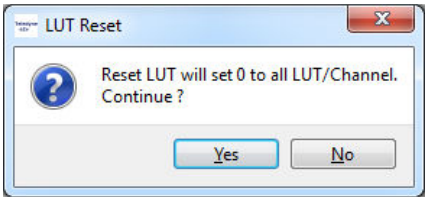


   This action is stopping the LUT corrections, but LUT correction values are still loaded within FPGA. This means that LUT can be reapplied by a simple click on "**Lookup Table is Disabled**" button.

2. By clicking on "**Reset**" button
   LUT corrections can be stopped in clicking on the "**Reset**" button. This action erases LUT values from FPGA.

   After clicking on "**Reset**" button, the pop-up window of figure 4-31 is displayed. Click "**Yes**" to confirm your choice.

Figure 4-31 Stopping LUT table.



4.5.3.5. Example of LUT effects on INL with 4 ADC cores interleaved

Figure 4-32. INL acquisition with 4 cores interleaved **without** LUT

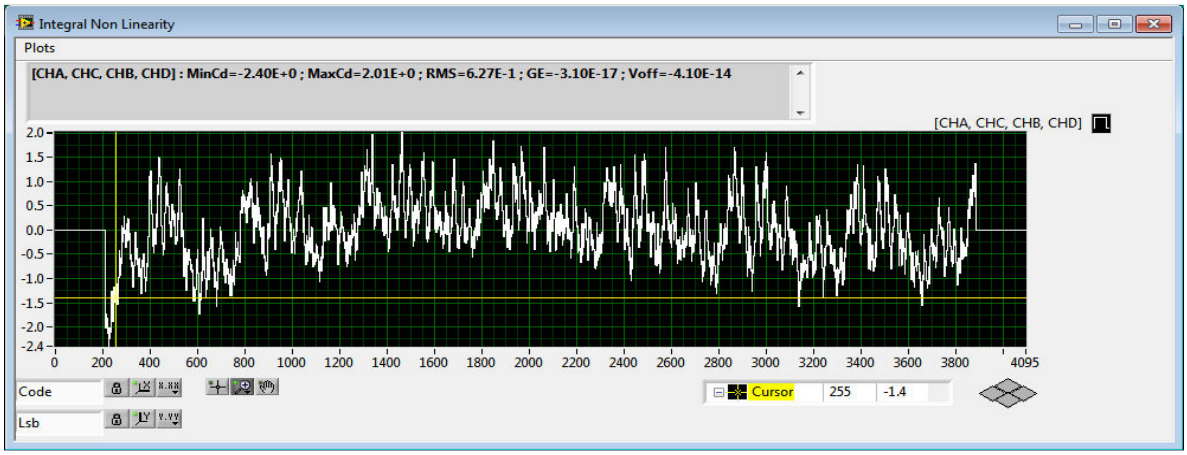
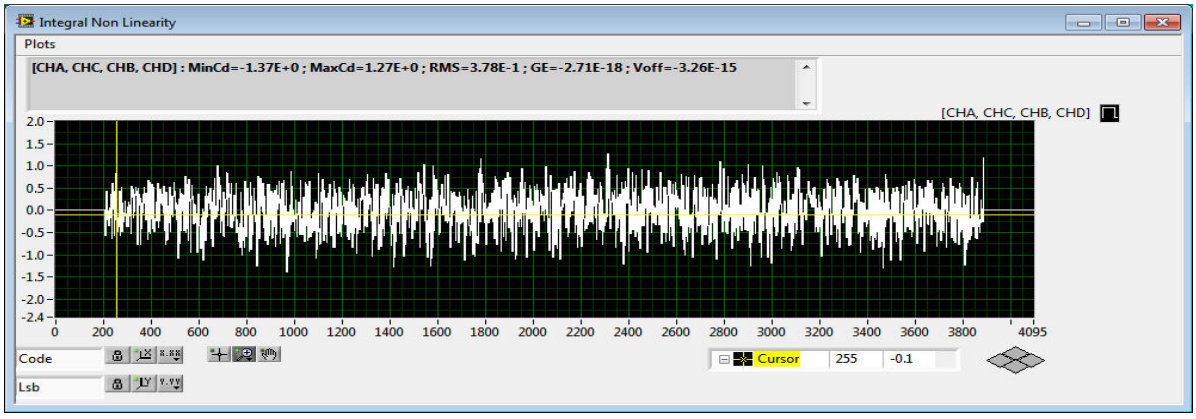


Figure 4-33. INL acquisition with 4 cores interleaved **with** LUT



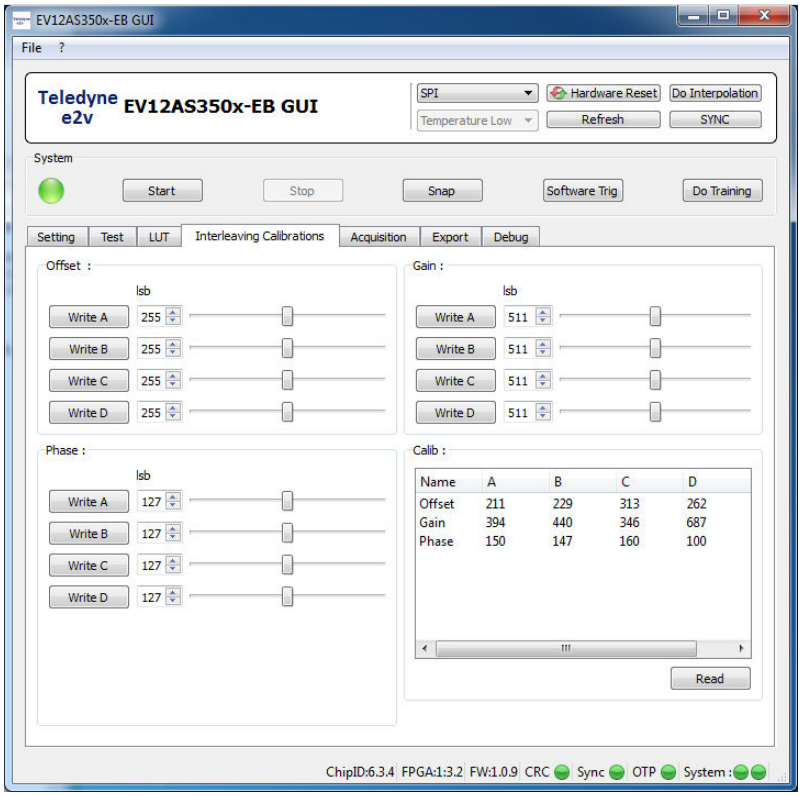
4.5.4 Interleaving calibrations

This tab enables to modify ADC default interleaving calibrations (written within OTP) in order to get an optimum calibration for the considered clock rate and Fin. It is however recommended to use OTP calibrations.

- Interleaving Offset: "**Offset**" menu corresponds to ADC registers x_OFFSET_CAL (x=A, B, C & D)
- Interleaving Gain: "**Gain**" menu corresponds to ADC registers x_Gain_CAL (x=A, B, C & D)
- Interleaving Phase: "**Phase**" menu corresponds to ADC registers x_Phase_CAL (x=A, B, C & D)

This tab is accessible in the only case when SPI is selected in the Header Menu.
The "Calib" Menu displays the calibration value (Offset, Gain and Phase) for each ADC core (A, B, C and D)
Values are displayed in decimal.

Figure 4-34. Interleaving Calibrations tab



Clicking on the "**Read**" button in the Calib Menu refresh the display in reading SPI registers x_OFFSET_CAL (x=A, B, C & D), x_GAIN_CAL (x=A, B, C & D) and x_PHASE_CAL (x=A, B, C & D)
Notes:

- Possible values for Offset adjustment is 0 to 511
- Possible values for Gain adjustment is 0 to 1023
- Possible values for Phase adjustment is 0 to 255

It is possible to modify interleaving calibrations in writing for each ADC core the value to be written (either with the cursor or with the arrow or in writing directly the value). After modifying a value, click on the associated "Write x" button.
It is possible to verify that the modification is well taken into consideration in checking values from the "Calib" Menu after having clicked on the "**Read**" button.

Note: If a "**Do interpolation**" is launched; all modifications done on Interleaving Calibrations are lost.

It is possible to save ADC calibrations and settings in a context file (file.ctx) that can be reloaded. Refer to chapter 4.4.1 for explanation about context files.

4.5.5 Acquisition

This tab enables to configure the acquisition.

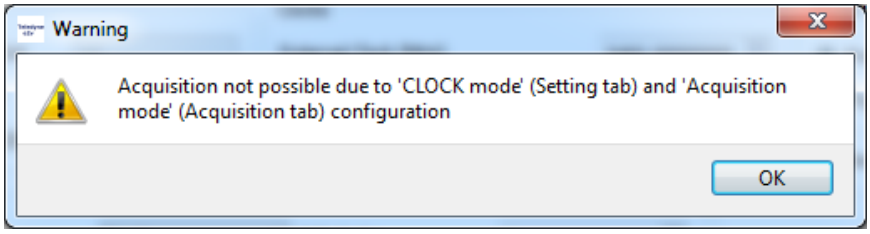
4.5.5.1. Acquisition mode Menu

Figure 4-35. Acquisition tab – Acquisition mode Menu

3 acquisitions modes are possible :

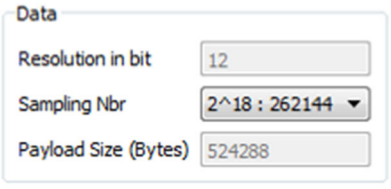
- **4 Cores interleaved**. This option is possible in the only case when **CLOCK mode** is configured in "**Interleaving**" mode within the Settings tab. If it is not the case, pop-up window of Figure 4-36 is displayed.
- **4 Cores aligned without averaging.** This option is possible in the only case when **CLOCK mode** is configured in "**No Interleaving**" mode within the Settings tab. If it is not the case, pop-up window of Figure 4-36 is displayed.
- **4 cores aligned with averaging** (calculated within GUI). This option is possible in the only case when **CLOCK mode** is configured in "**No Interleaving**" mode within the Settings tab. If it is not the case, pop-up window of Figure 4-36 is displayed.

Figure 4-36. Pop-up window in case of Clock mode incompatibility



4.5.5.2. Data Menu

Figure 4-37. Acquisition tab – Data Menu



In this Menu the user indicates the number of bit to be acquired (acquisition on 12-bit) and the number of ADC samples to be acquired. Possible numbers of samples are:

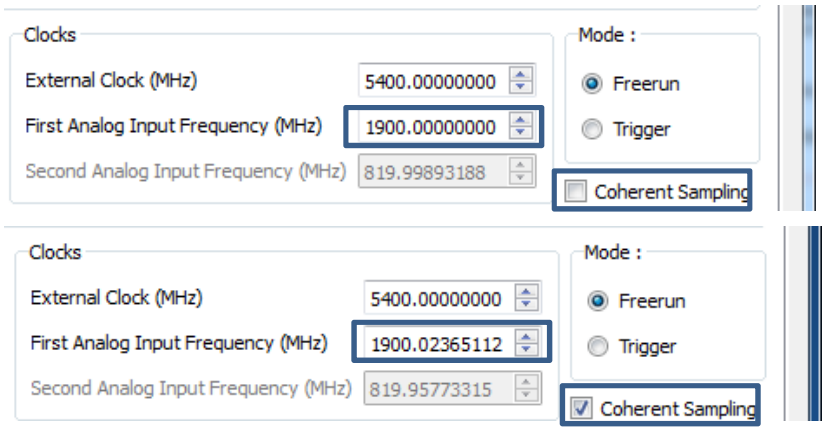
- 2^{18} points = 262 144 samples
- 2^{17} points = 131 072 samples
- 2^{16} points = 65 536 samples

Number of samples displayed corresponds to the total number of samples if 4 ADC cores are interleaved. If 4 Cores are aligned the number of samples per core is 4 times lower than the number displayed in the Sample Nbr field.

Payload size (Bytes) represents the memory size to be allocated on the PC to get the sampled data (each sample is coded on 2 Bytes for USB transfer)

4.5.5.3. Clock Menu

Figure 4-38. Acquisition tab –Clock Menu



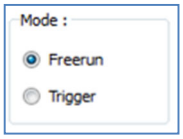
This Menu enables to indicate the considered **External Clock** frequency (in MHz) so that the GUI can calculate ADC output spectrum and identify the different spurs (harmonics, interleaving spurs, intermodulation spurs, clock related spurs …)

First Analog Input Frequency (MHz): In this field the user is asked to complete the first analog input frequency. it is not necessary to fill this field if a single tone is selected in the Processing Menu. Indeed, the GUI uses the highest spur of the ADC output spectrum to detect the fundamental.
Second Analog Input Frequency (MHz): This field is mandatory in the only case when Dual tone is selected. The user is asked to complete the second analog input frequency in this field.

If **Coherent Sampling** option is selected, it automatically slightly modifies the First Analog Input Frequency and the Second Analog Input frequency (if applicable) in order to get a coherent sampling (function of external clock and number of samples).

4.5.5.4. Mode Menu

Figure 4-39 Acquisition tab – Mode Menu

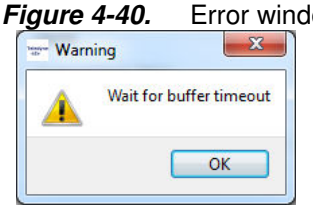


This Menu is used to select between **Freerun** and **Trigger** Acquisition.

- **Freerun** is the mode by default. Acquisition is launched when the "**Snap**" button from the System Menu is pressed. A single acquisition is done.

- **Trigger** can be selected in order to launch the acquisition on an event (hardware of soft event).
    - Soft event:
      It is necessary to first press “Snap” button and then “Software Trig” button in the System Menu.
      If the user is waiting too much time to launch an acquisition, an error window is displayed as shown on Figure 4-40.

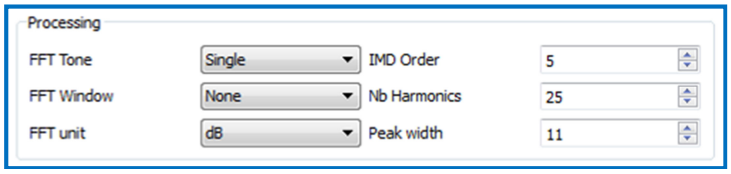
Figure 4-40. Error window if no trigger occurs



    - Hard event:
      It is necessary to first press the “**Snap**” button and then an acquisition is launched when an event (pulse) occurs on signal SPARE SYNC_FPGA_P / SPARE SYNC_FPGA_N.

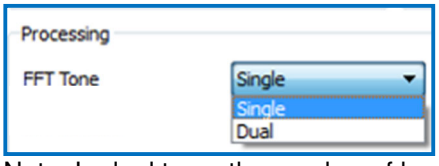
4.5.5.5. Processing Menu

Figure 4-41. Acquisition tab – Processing Menu



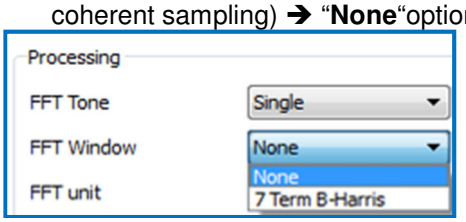
This Menu enables to configure the FFT calculation :

- **FFT Tone**: this field enables to choose between a **Single** Tone or a **Dual** Tone acquisition.

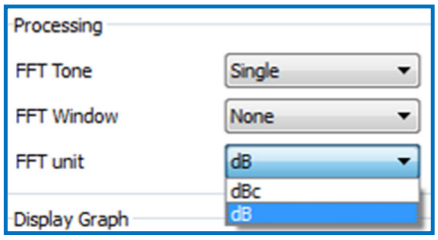


Note: In dual tone, the number of harmonics is limited to 20.

- **FFT Window**: this field is used to apply a FFT windowing option if the sampling is not coherent. A “**7-Term Blackmann-Harris**” window option is proposed. By default no windowing is applied (case of coherent sampling) ➔ “**None**“option.

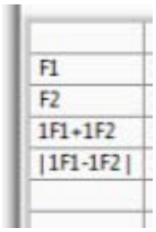


- **FFT Unit**: this field is used to select the FFT unit. By default unit is "**dB**". "**dBc**" option is also possible. Selecting this option implies that the fundamental is set at 0 dBc.

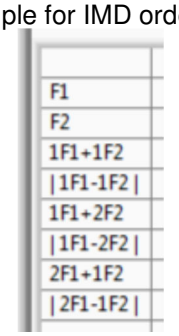


- **IMD Order**: this field is used in the only case when a Dual Tone is selected in the FFT Tone field. It indicates how many intermodulations will be displayed in the "FFT Parameters" window. See display Graph Menu.

Example for IMD Order = 2



Example for IMD order = 5

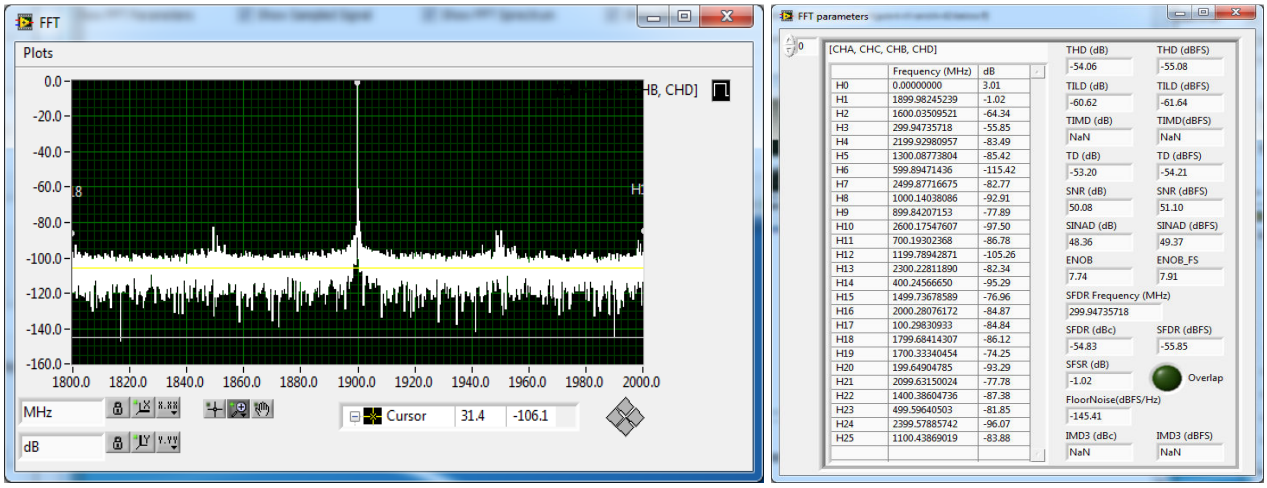


- **Nb Harmonics:** this field is used to indicate how many harmonics will be displayed in the "FFT Parameters" window. It is also used to indicate how many harmonics will be considered in the THD (H2 to Hn) and in the SNR (Hn and higher ranks). By default 25 first harmonics are considered in THD and higher rank harmonics are considered as SNR.
  Note : In dual tone, the number of harmonics is limited to 20.

- **Peak width:** this field is used to configure the detection of the highest spur (for SFDR calculation). Indeed, in case of phase noise on fundamental or DC component, some points need to be excluded when looking for the highest spurs. Peak width default value is 11: it means that when looking for the highest spurs, the 5 points around the fundamental plus the point of the fundamental are excluded .On the same way, the 5 points above the DC component are excluded.
  It is recommended to keep Peak width value at 11. This value can be increased if SFDR is detected in the cone of the fundamental or DC components.
  A peak width value of 1 means that only the highest spur of DC component and highest spur of fundamental are excluded.
  Only odd values are possible for peak width.

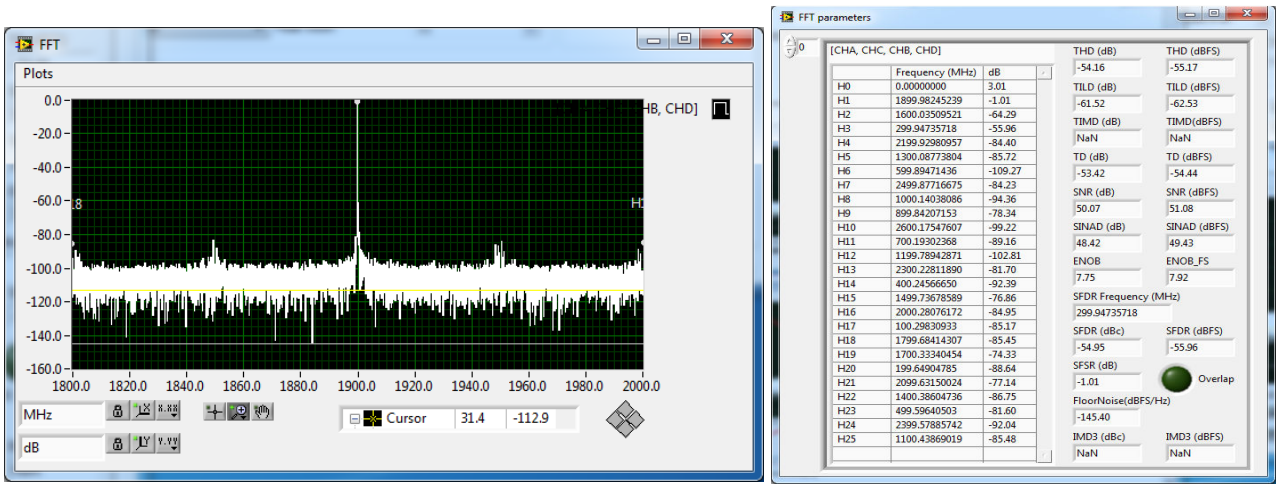
  The peak width effect is illustrated in figure 4-42 and 4-43 below.

Figure 4-42. Example of acquisition with peak width = 1 (Fclk = 5.4GHz, Fin = 1900MHz)



On above figure, SFDR is fund on the fundamental due to the cone. Peak width needs to be increased.

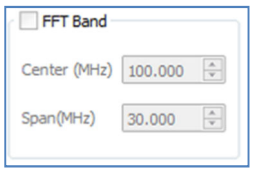
Figure 4-43. Example of acquisition with peak width = 11 (Fclk = 5.4GHz, Fin = 1900MHz)



With Peak width = 11, the points around the fundamental does not interfere in the highest spur identification. SFDR is calculated correctly.

4.5.5.6. FFT Band Menu

Figure 4-44. Acquisition tab – FFT Band Menu



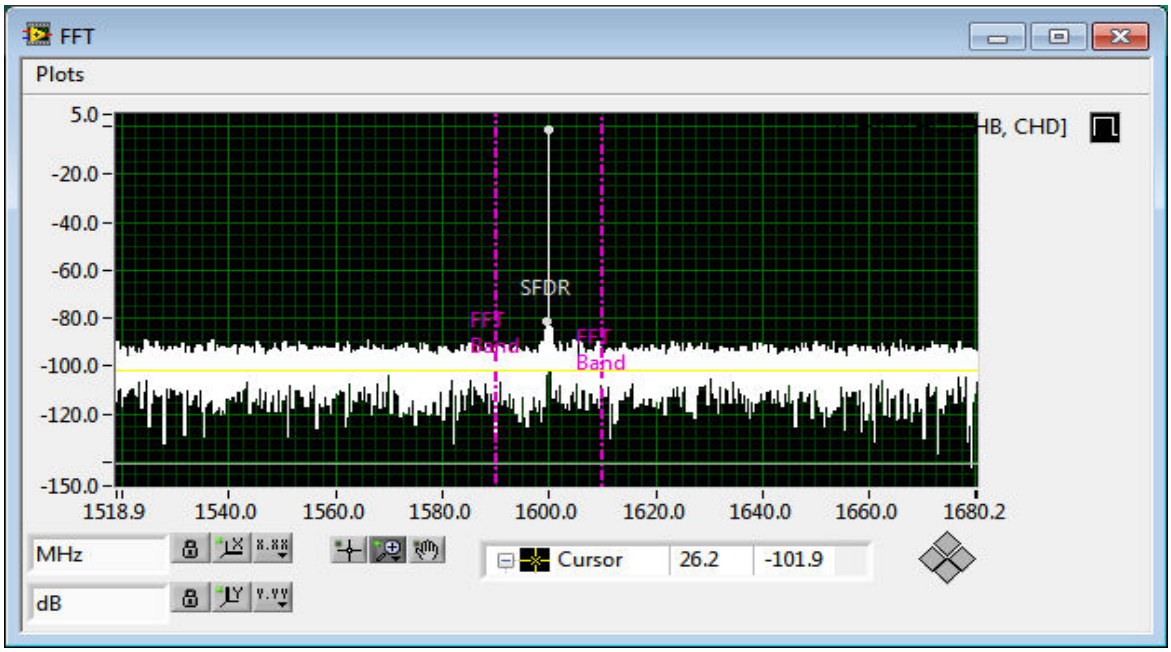
This menu is accessible by selecting the FFT Band field in the top left corner. It enables to calculate FFT parameters on Narrow band. If this option is not selected, the FFT calculation is done over full Nyquist zone.

- **Center (MHz):** this field is used to indicate the center of the narrowband to be considered.
- **Span (MHz):** this field is used to indicate the span of the considered band of interest.

This menu is accessible for both Single Tone and Dual Tone acquisition.
Once Center and Span parameters are configured, it is possible to launch an acquisition. Two purple vertical markers are displayed on FFT spectrum to delimit the band of interest on which FFT calculation are done. See Figure 4-45.

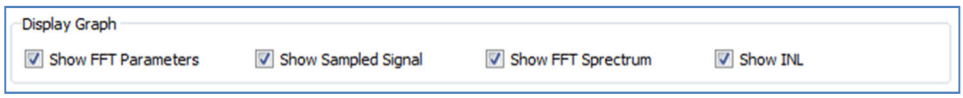
Figure 4-45. Example of FFT band with markers showing the band of interest

Center = 1600MHz & Span=20MHz



4.5.5.7. Display Graph Menu

Figure 4-46. Acquisition tab – Display Graph Menu

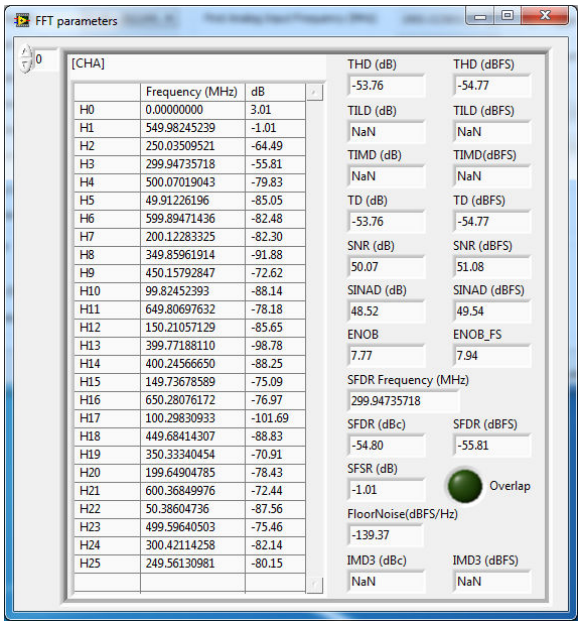


This Menu enables the user to select which graphs need to be displayed after data acquisition.

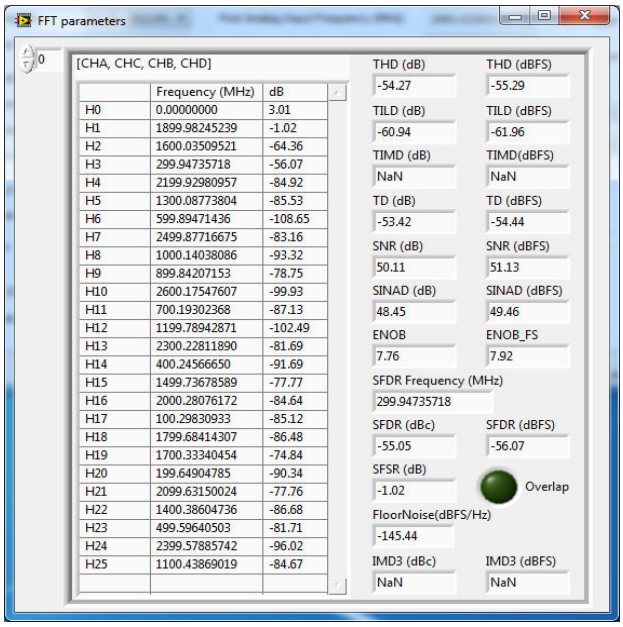
- **Show FFT parameters:** selecting this graph will display FFT parameters (ENOB, SFDR, …) as shown on the example of Figure 4-47. See Section 5 for parameters definition and FFT formula calculations.
- **Show Sampled Signal:** selecting this graph will display the sampled data as shown on the example of Figure 4-48.
- **Show FFT Spectrum:** selecting this graph will display the ADC FFT spectrum with spurs identification as shown on the example of Figure 4-49 and Figure 4-50.
- **Show INL**: selecting this graph will display the ADC INL curve as shown on the example of Figure 4-51.

Figure 4-47 Examples of FFT Parameters window

a) FFT parameter window for ADC core A interleaved



b) FFT parameter window for 4 ADC cores



Notes:

1. See Section 5 for definitions of FFT calculations.

- The Overlap LED is green if everything is OK. The Overlap LED is red if some harmonics are superposed (for instance if Fin=Fclk/4) or if analog input RF generator is OFF or if some interleaving spurs are superposed to harmonics. Refer to chapter 5.2 for more information.
- In mode “4 Cores Aligned”, it is possible to switch from one core to another thanks to the small arrows located on the top left corner of above window ([CHA] corresponds to ADC Channel A, [CHB] to ADC Channel B, ….)
- With 4 Cores interleaved, the only possible choice is [CHA, CHC, CHB, CHD].

Figure 4-48. Examples of Sampled Data

a) Sampled Data for ADC core A, B, C & D interleaved

b) Sampled Data for 4 ADC cores

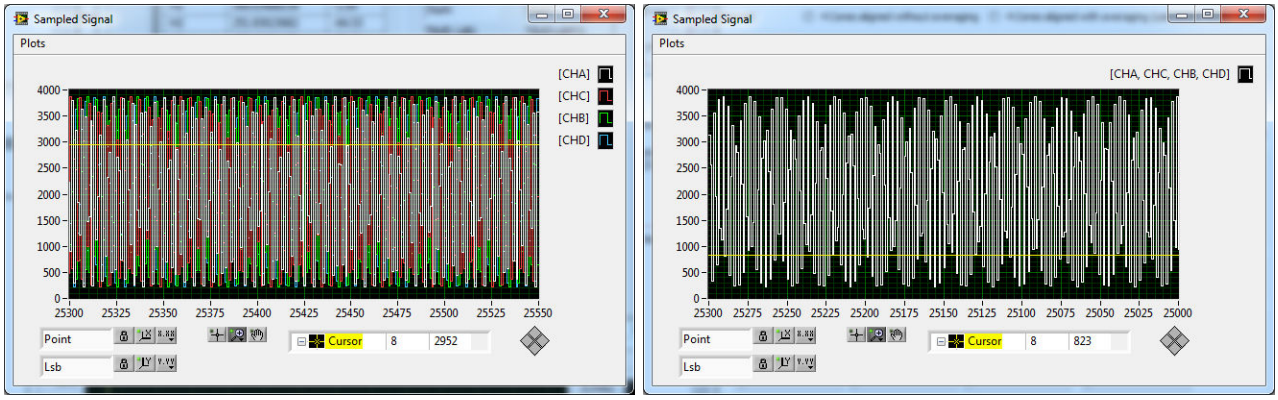
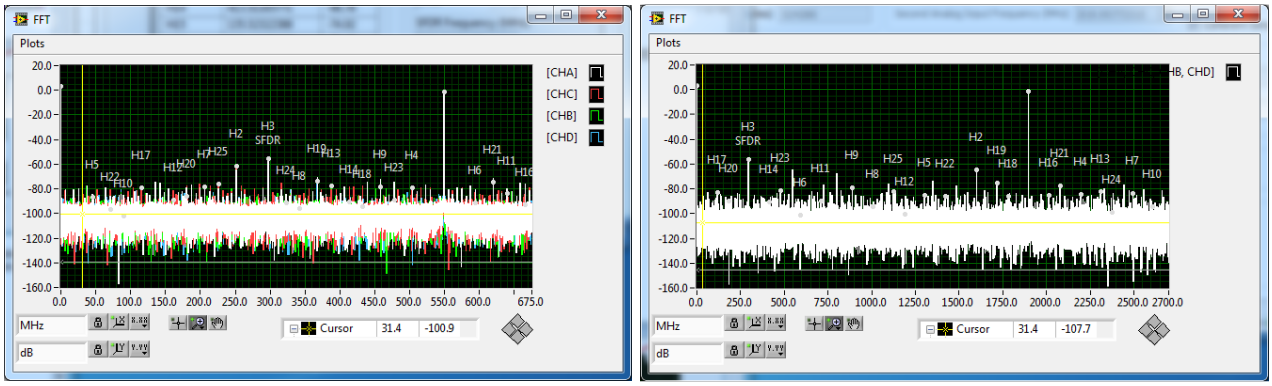


Figure 4-49. Examples of FFT Spectrum

a) FFT Spectrum for ADC core A, B, C & D interleaved

b) FFT spectrum for 4 ADC cores



Note: In mode “4 Cores Aligned”, the 4 FFT spectrum are superposed. For a better readibility it is possible to select which ADC core FFT to be displayed by clicking right on CHA (or CHB or CHC or CHD) as shown on Figure 4-50 below.

Figure 4-50. Example of FFT Spectrum with drawing option selection

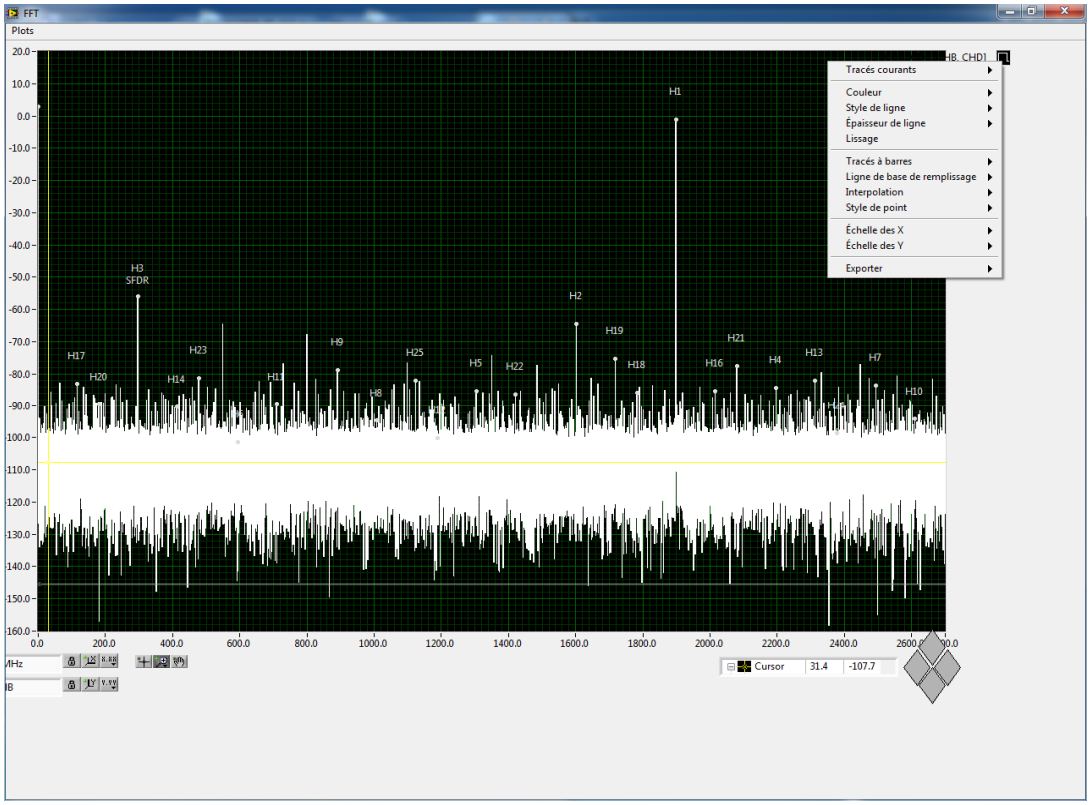
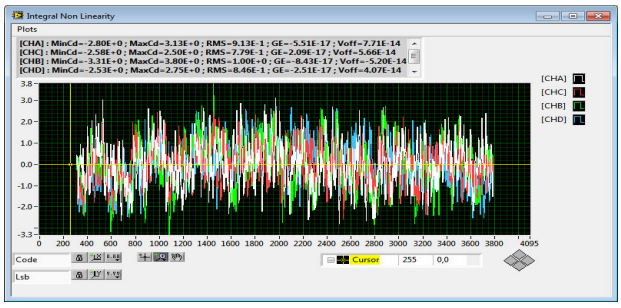


Figure 4-51. Example of INL curve

a) INL for ADC core A, B, C & D



b) INL for 4 ADC cores interleaved

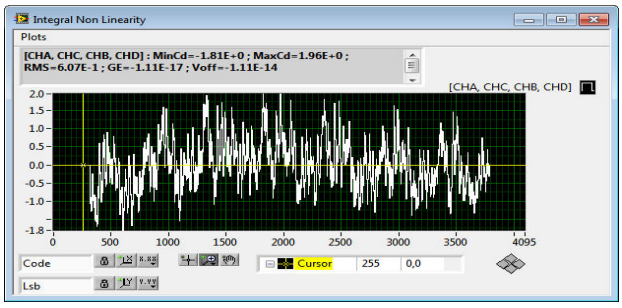


Figure 4-52. Acquisition tab – Checks Menu

This Menu enables to monitor the Parity Bit and Overrange Bit for each ADC Core.
Number of **Parity Check Failed** (among the Sampling Nb) is displayed for each ADC Core. If value is zero, everything is OK.
Number of **Overrange** (among the Sampling Nb) is displayed for each ADC Core. If value is zero everything is OK.

Examples are shown on Figure 4-53 & Figure 4-54

Figure 4-53. Checks Menu with saturation

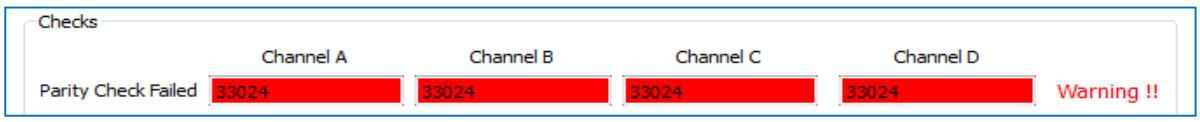
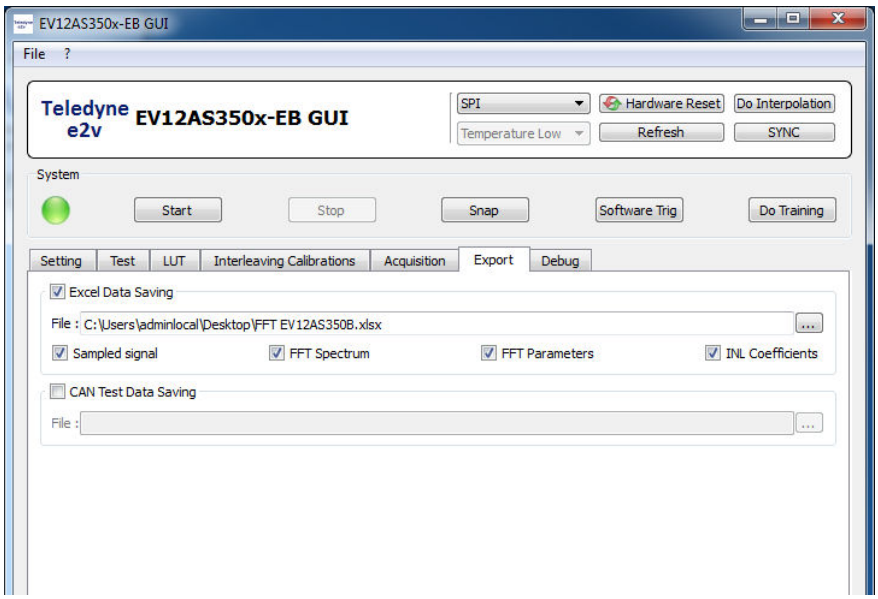


Figure 4-54. Checks Menu with Over-range

4.5.6 Export

Figure 4-55. Export tab



This tab is used to export acquisition Data in a File.

4.5.6.1. Data exportation in Excel file

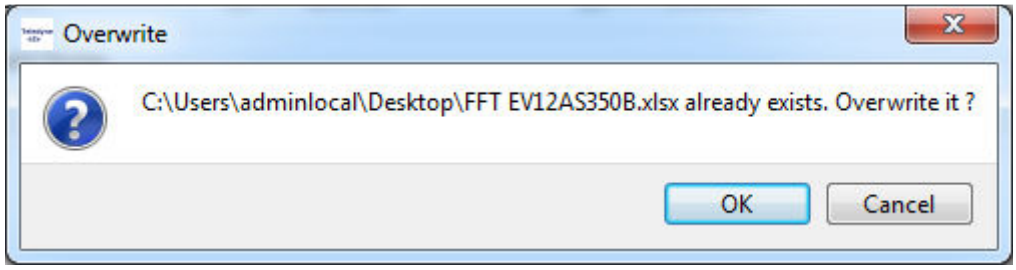
This mode is activated by checking the box in the **Excel Data Saving** Menu as shown on Figure 4-55 above. The procedure to be followed is:

1. Indicate the path of the file
2. Give a name to the file
3. Select the data to be exported in the file (**Sampled Signal**, **FFT Spectrum**, **FFT parameters** and **INL coefficients**)
4. Then click on the "**Snap**" button of the System Menu to launch the acquisition and save the selected data in the Excel File

Notes:

1. If the given file name already exists, the user is asked to confirm he wants to overwrite the existing file as shown on figure below:

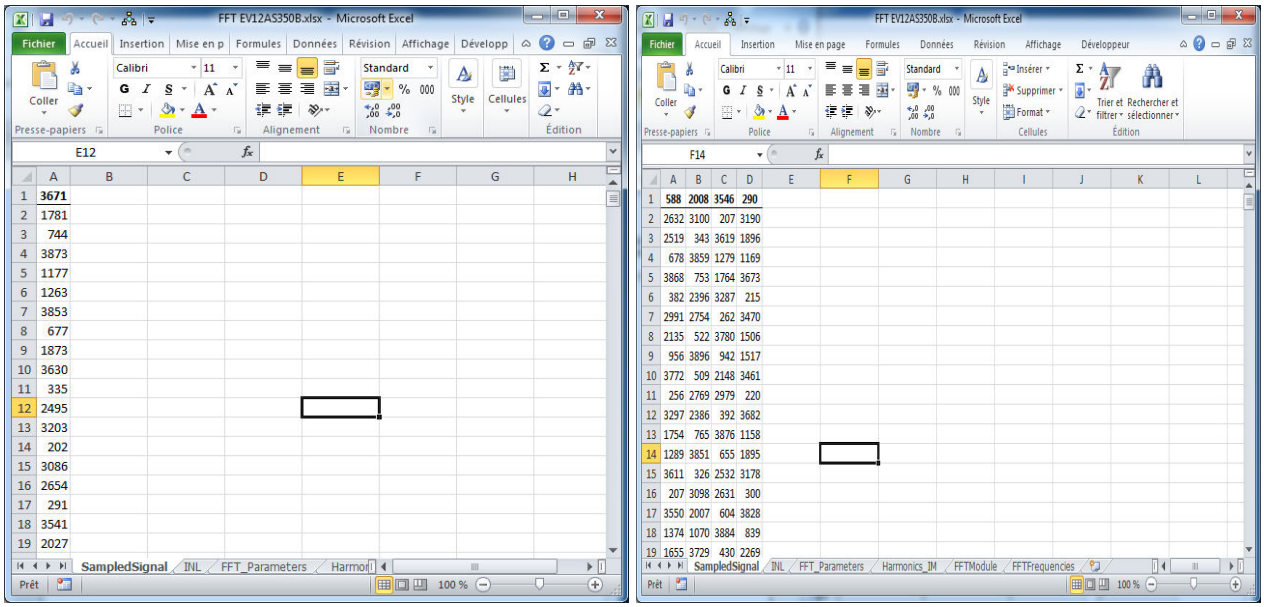
Figure 4-56. Overwrite window



2. When the FFT Spectrum is selected, the harmonics are also saved. Each kind of exported data appears in a different sheet of the Excel file as shown on Figure 4-57 to 4-60. Note that FFT Spectrum is saved in two excel tabs:
    a. FFTModule: for Y axis
    b. FFTFrequencies: for X axis

3. When launching an acquisition in the Freerun mode followed by clicking on the “Start” button from System Menu, only the 1st acquisition is saved even if the user performs successive acquisitions.

Figure 4-57. Example of exported Excel file – SampledSignal tab (When “Sampled Signal” is selected)



Note: When the acquisition is done in « 4 Cores Interleaved » mode, the Sampled Data is displayed on one column. When the acquisition is done in “4 Cores Aligned” mode, the Sampled Data is displayed on 4 columns:

- Column A for ADC Core A
- Column B for ADC Core C
- Column C for ADC Core B
- Column D for ADC Core D

Figure 4-58. Example of exported Excel file – INL tab (When "**INL coefficients**" is selected)

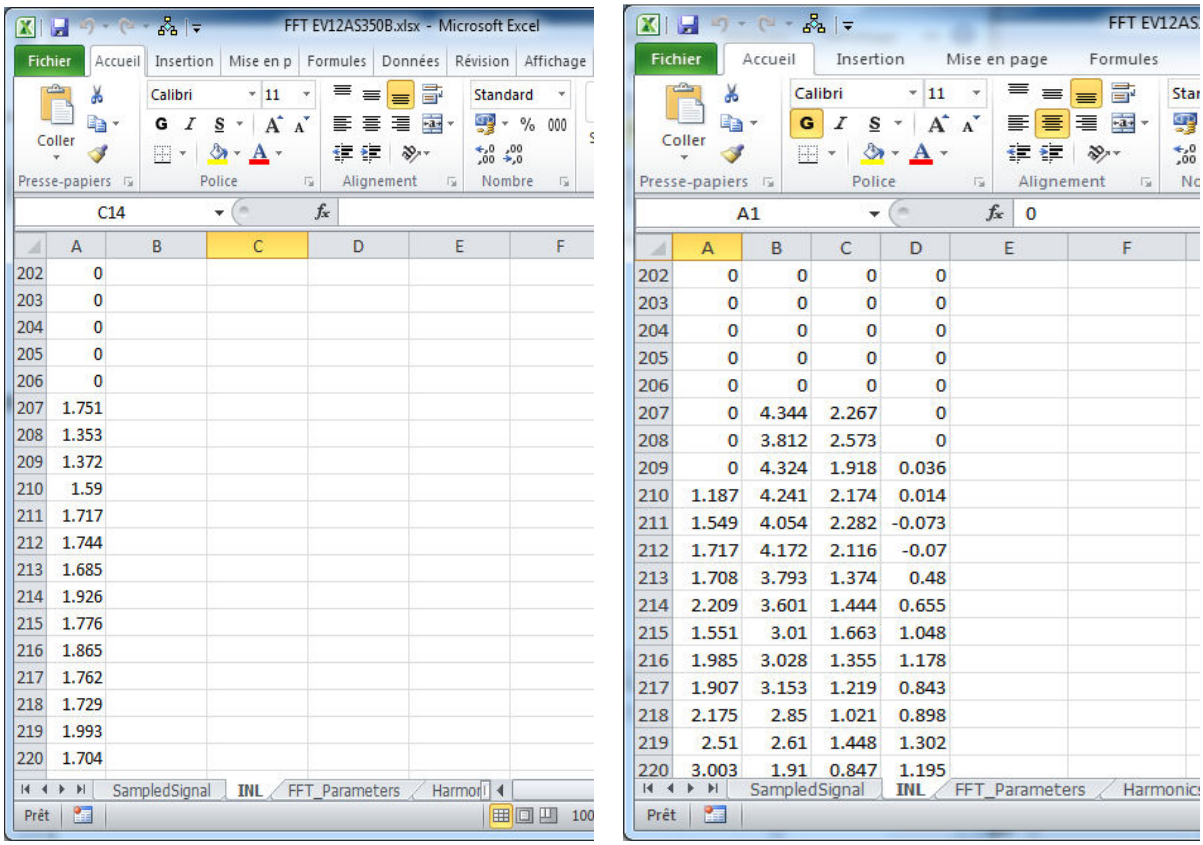
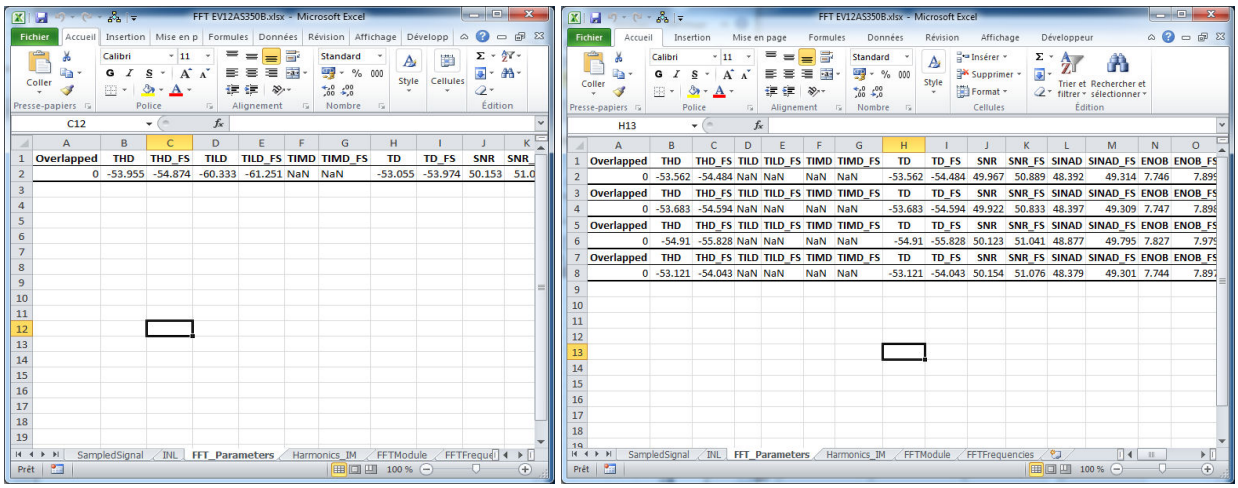
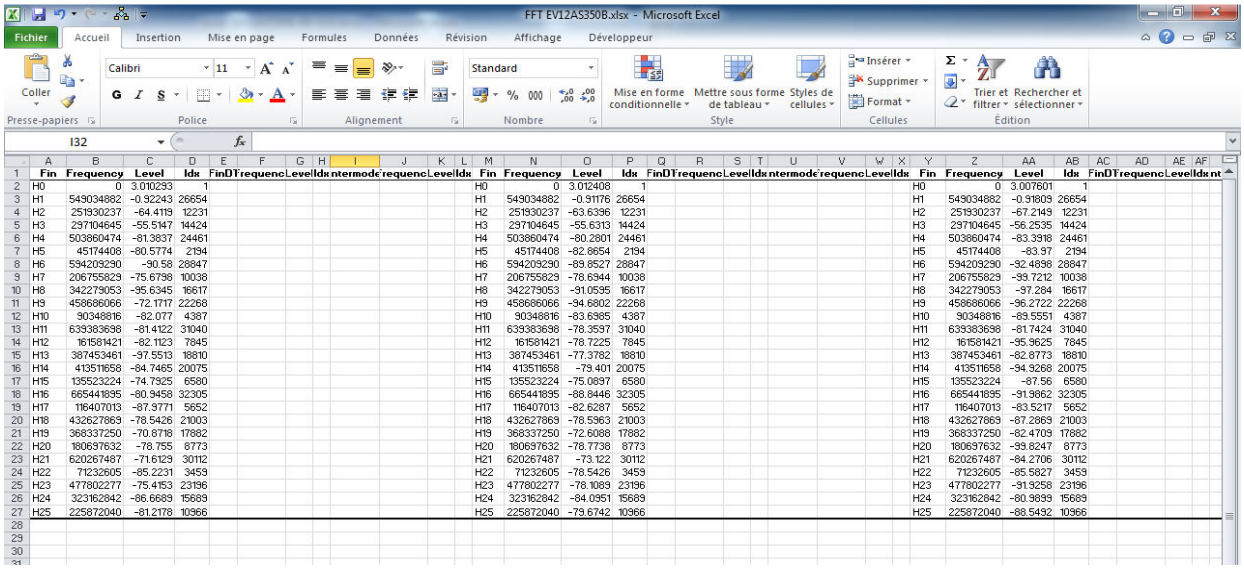


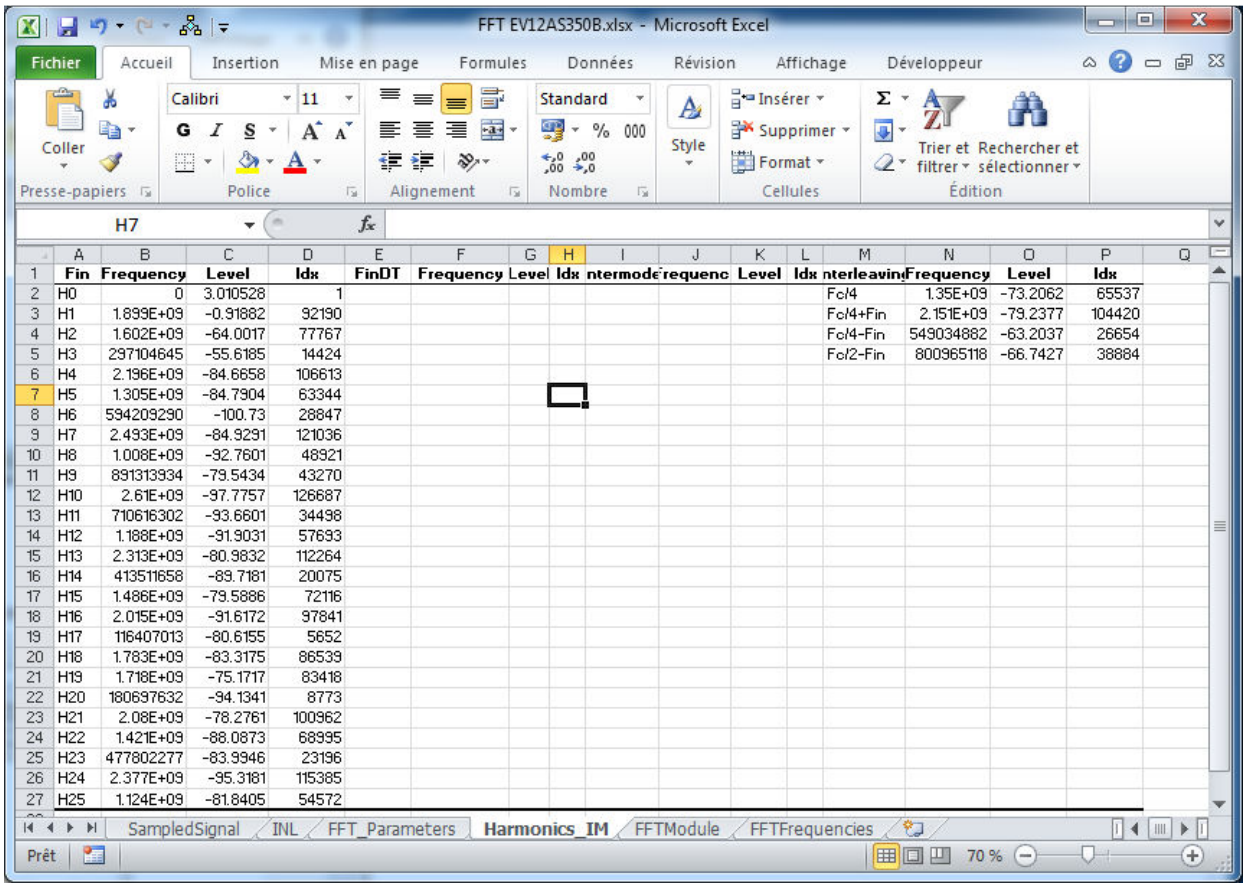
Figure 4-59. Example of exported Excel file – FFT_Parameters tab (When "**FFT Parameter**" is selected)



Note : Values with _FS are referenced to ADC Full Scale. Overlapped = 0 means that there is no harmonic superposition.

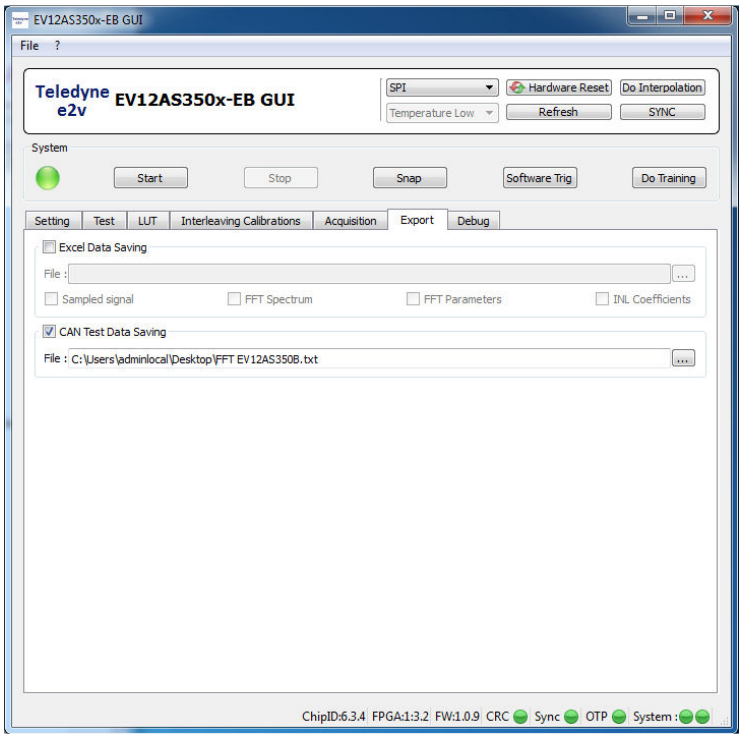
Figure 4-60. Example of exported Excel file – Harmonics_IM tab (When "**FFT Parameter**" is selected)





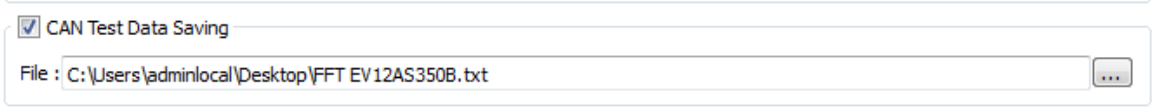
This tab displays all spectral components, including DC component (H0), the fundamental (H1) and interleaving spurs.

4.5.6.2. Data exportation in CAN test



Note : CAN test is a proprietary format.

This mode is activated by checking the box in the **CAN Test Data Saving** Menu.



With this mode, only the sampled signal can be saved.

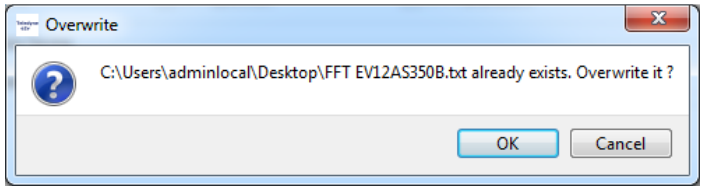
The procedure to be followed to save Sampled Data in a CAN Test file is:

1. Indicate the path of the file
2. Give a name to the file.
3. Then click on the "**Snap**" button of the System Menu to launch the acquisition and save the sampled signal in a text file with CAN Test format, as example shown on Figure 4-62.

Notes:

1. If the given file name already exists, the user is asked to confirm he wants to overwrite the existing file as shown on figure below:

Figure 4-61. Overwrite window



2. When launching an acquisition in the Freerun mode followed by clicking on the "Start" button from System Menu, only the 1st acquisition is saved even if the user is continuing successive acquisitions.

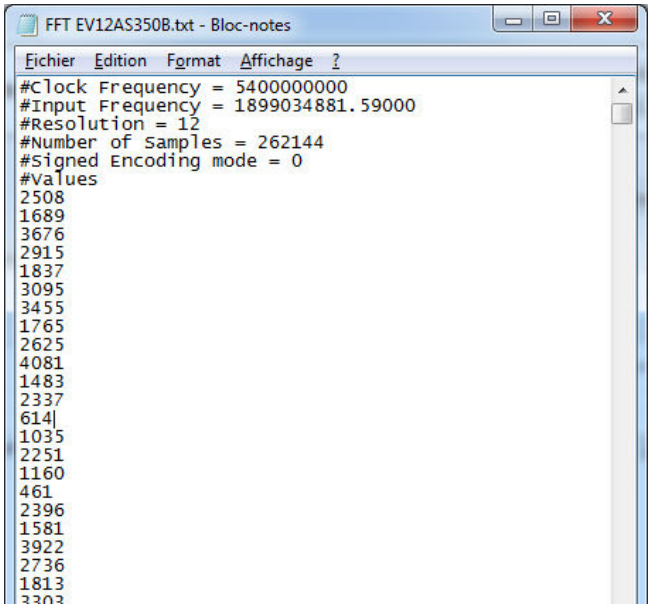
3. Notes concerning CAN Test file

Sampled Data is saved on different lines with the following order: Core A, Core C, Core B and finally Core D.

The header in described below:

- #Clock Frequency = xxx — Frequency of ADC external clock
- #Input Frequency = xxx — Frequency of Analog input signal
- #Resolution = 12 — ADC resolution
- #Number of samples — Number of samples in the sampled signal
- #Signed Encoding Mode = 0 — 0 means a Two complement coding
- # Values — It indicates the end of the header. Following lines are the sampled data

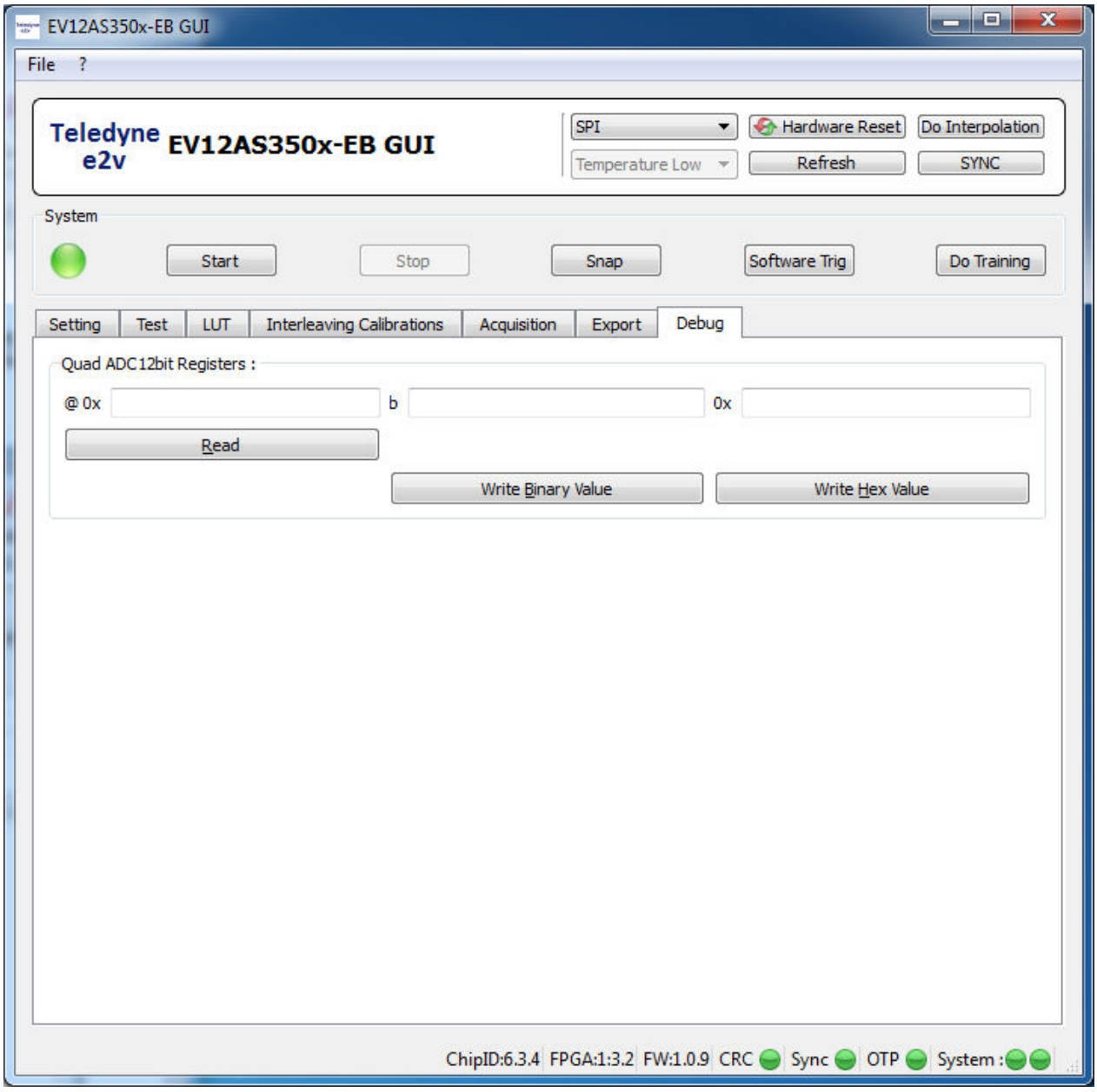
Figure 4-62. Example of exported CAN test file (4 ADC cores interleaved)



4.5.7 Debug

This tab can be used for debug (advanced mode) and is therefore not recommended.
It enables to read or write register values manually
Field **@0x** is used to provide the address (in Hexadecimal) of the register to be read or written.
The two other fields are used to display the read value or to write values at the selected address. Values read/written are displayed in both Binary (**b**) and Hexadecimal format (**0x**).

Figure 4-63. Debug window



Example: OTP_SPI_SELECT is a register of the channel A, B, C, D and the MASTER SPI. It is the same address for channel and MASTER SPI

SPI Instruction (in hexa)

1- Channel A selected :

Write @CHANNEL_SELECT	@0x 00
Write @ OTP_SPI_SEL	FFFF

2- CHANNEL B selected

Write @CHANNEL_SELECT	@0x 01
Write @ OTP_SPI_SEL	FFFF

3- CHANNEL C selected

Write @CHANNEL_SELECT	@0x 02
Write @ OTP_SPI_SEL	FFFF

4- CHANNEL D selected

Write @CHANNEL_SELECT	@0x 03
Write @ OTP_SPI_SEL	FFFF

5- MASTER selected

Write @CHANNEL_SELECT	@0x 07
Write @ OTP_SPI_SEL	FFFF

6- All selected (OTP value)

Write @CHANNEL_SELECT	@0x 04
Write @ OTP_SPI_SEL	0000

7- All selected (SPI value)

Write @CHANNEL_SELECT	@0x 04
Write @ OTP_SPI_SEL	FFFF

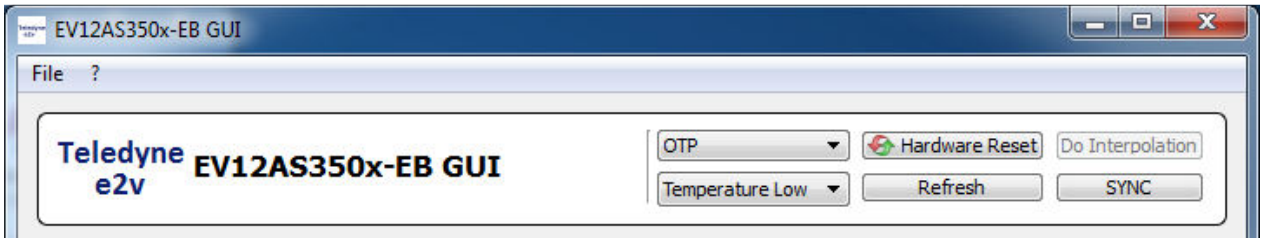
4.5.8 ADC Calibrations / interpolation

Several options are considered for ADC interleaving calibrations:

- OTP mode: Using calibration values defined in OTP Temperature High registers
- OTP mode: Using calibration values defined in OTP Temperature Low registers
- SPI mode: Using user's defined values (calibrations need to be done by the user after each power-up)
- SPI mode: Interpolate calibrations at the temperature of use. This interpolation mode provides the best dynamic performances regarding the level of interleaving spurs. It is therefore the recommended option

The choice between the different options is done via the Header Menu of figure 4-64:

Figure 4-64. User Interface Header Menu



Note that parameters that are not linked to ADC interleaving calibrations (such as CM_IN and R_IN) are not affected by above choice, since it exists only two choices:

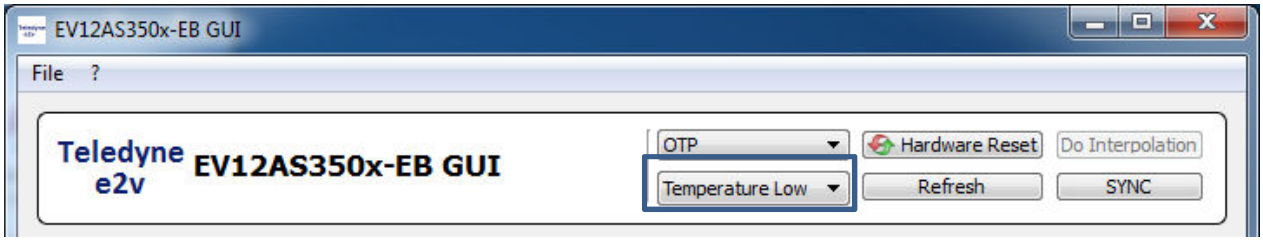
- OTP values (valid whatever the temperature range)
- SPI values (default values or user defined values)

4.5.8.1. OTP Temperature Low calibrations

This configuration is to be used for junction temperature lower than 70°C (ambient and cold temperatures). It corresponds to CAL_SET_SEL register defined in Master SPI of the ADC (CAL_SET_SEL=1).

It is the mode by default when opening the GUI.

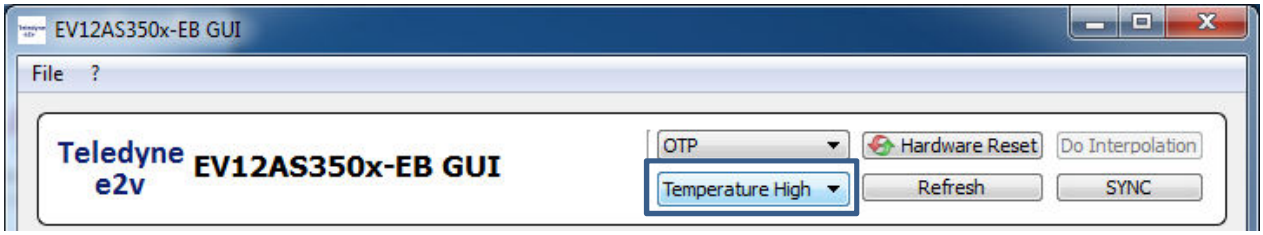
Figure 4-65. Header Menu with "**OTP Temperature Low**" selection



4.5.8.2. OTP Temperature High calibrations

This configuration is to be used for junction temperature higher than 70 °C (hot temperature). It corresponds to CAL_SET_SEL register defined in Master SPI of the ADC (CAL_SET_SEL=0).

Figure 4-66. Header Menu with "**OTP Temperature High**" selection

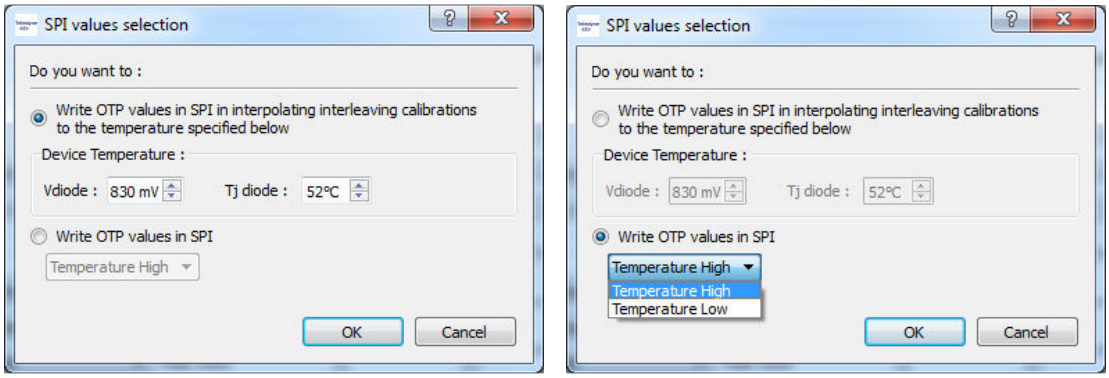


4.5.8.3. SPI User's defined calibrations

With this option the user doesn't use OTP values anymore and write his own calibration values (interleaving calibrations). This is done in the "Interleaving calibrations" tab from the GUI. Please refer to chapter 4.5.4.
This option is an advanced mode and is reserved to expert users.
When the user wants to switch from OTP mode to SPI mode, the user is asked to select between the two choices of figure 4-67 (in order to avoid getting the SPI default values that would lead to high interleaving spurs).

- Launch a "**Do interpolation**" procedure at the temperature of use. See chapter below.
- Write OTP calibration values within the SPI registers: The user is asked to select which OTP values need to be written within SPI (OTP Temperature Low or OTP Temperature High)

Figure 4-67. SPI values selection pop-up window



Note: Interpolation of calibrations at the specified temperature are referenced to diode which is 7°C below hot spot temperature

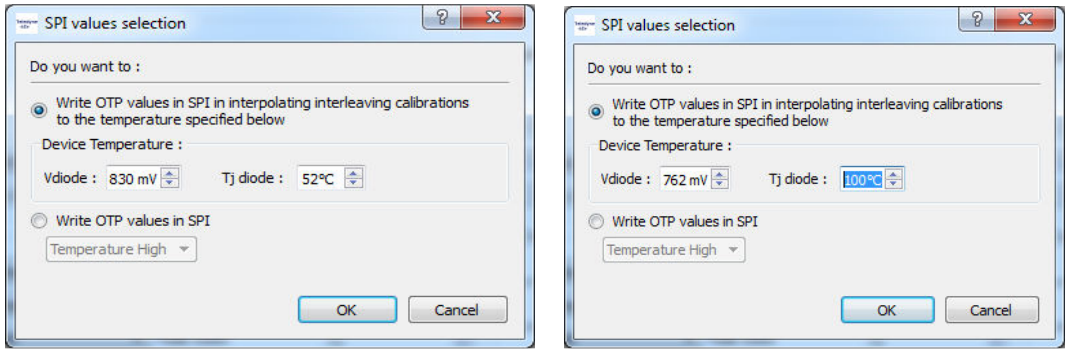
Note: When SPI mode is selected; R_IN and CM_IN values (defined in the Settings tab) are the values from SPI (no more OTP values).

- R_IN and CM_IN have their SPI default values after a hardware or software reset
- R_IN and CM_IN have their previous SPI values if no reset has been done (for instance, if R_IN is modified to value 12, switching to OTP mode will cause the R_IN value to switch to the value defined in OTP. When coming back to SPI mode, R_IN value will come back at the value 12 even if the SPI default value is 8).

4.5.8.4. Interpolated calibration: "Do Calibration"

This option will lead to optimum performances in terms of interleaving spurs.
This option is accessible in SPI mode only. When switching from OTP mode to SPI mode, the user has to select the first choice (interpolation of calibrations at the specified temperature. Reference is the diode which is 7°C below hot spot temperature)

Figure 4-68. SPI values selection pop-up window



Before clicking on "OK", be sure your have well filled the junction temperature (either through junction temperature expressed in°C either by Vdiode expressed in mV).

The principle consists in reading the OTP value dedicated to the calibration at cold temperature, then reading the OTP value dedicated to the calibration at hot temperature and then interpolate the value for the temperature of interest (Tj measured at diode which is 7°C below hot spot temperature) and write it via the SPI.

Interpolation formula is given below:
Equation 1 - Interpolation formula

Register $(V_{diode)} = (R_0\text{-}R_1)/(787\text{-}830) * (V_{diode}\text{-}830) + R_1$

With:
Vdiode = Value of the diode of temperature for the considered temperature in mV.
R_1 = Register when CAL_SET_SEL=1 is selected and R_0=Register when CAL_SET_SEL=0.
Register = each register listed in Table 1 below.

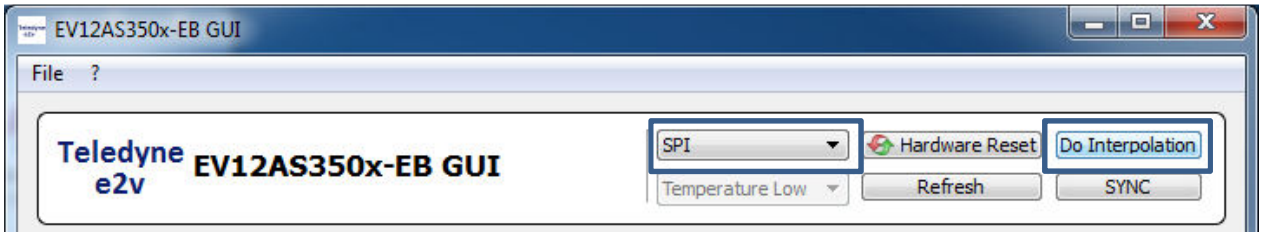
Registers to be interpolated over temperature are listed in Table 1.

Table 1. List of registers to be interpolated over temperature for optimum calibrations.

Registers in Master SPI	Registers in Channel SPI
A_OFFSET_CAL	CAL1
B_OFFSET_CAL	CAL2
C_OFFSET_CAL	CAL3
D_OFFSET_CAL	CAL4
	CAL5
	CAL6
	CAL7
	GAIN_CAL
	INT_GAIN_CAL
	PHASE_ CAL

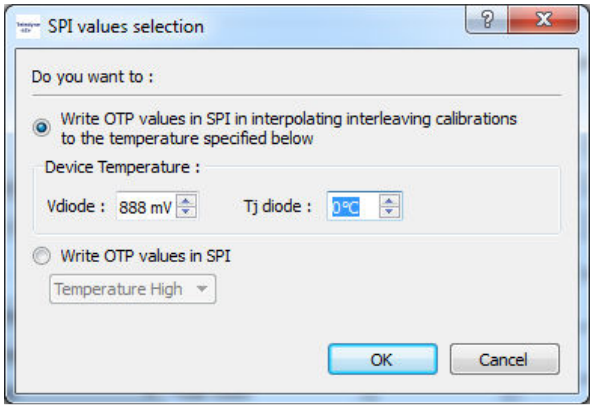
Once ADC is in SPI mode, the interpolation procedure can be launched at any time in pressing the "**Do Interpolaton**" button from the Header Menu.

Figure 4-69. Header Menu in SPI mode – access to "Do Interpolation" button



Pressing the "Do Interpolation" button opens the window of figure 4-69:

Figure 4-70. Do Interpolation window



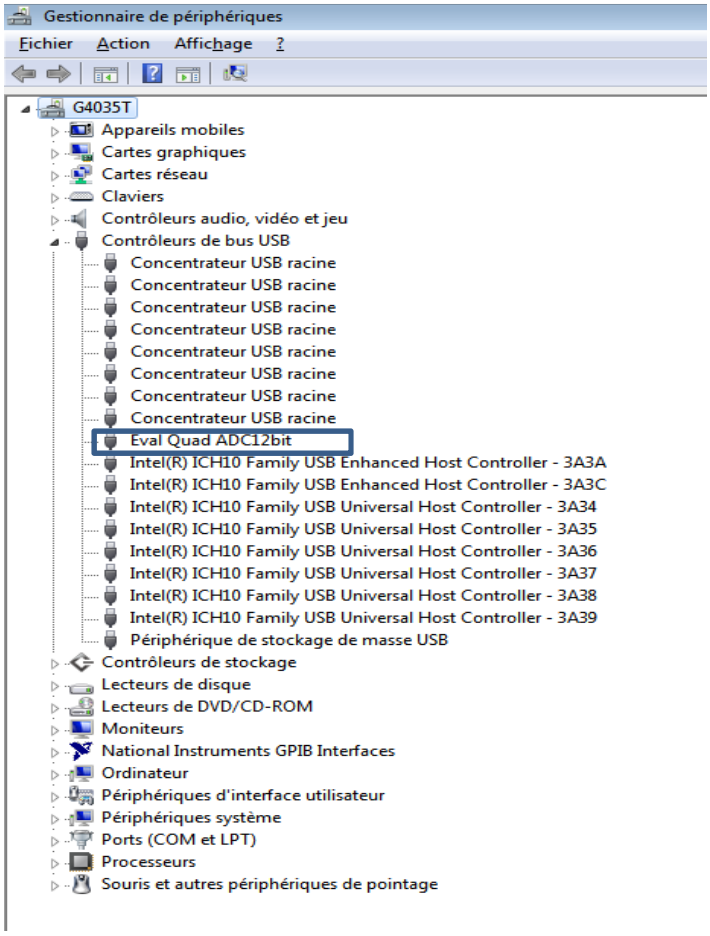
The user indicates the current junction temperature of the DAC (either through junction temperature expressed in°C either by Vdiode expressed in mV).
The junction temperature is referenced to the diode which is 7°C below hot spot temperature.

4.6 Troubleshooting

4.6.1 Software installation

Check that you own rights to write in the directory (administrator rights).
Check for the available disk space.
Check that the USB port is free and properly configured

Figure 4-71. USB Port Driver Configuration

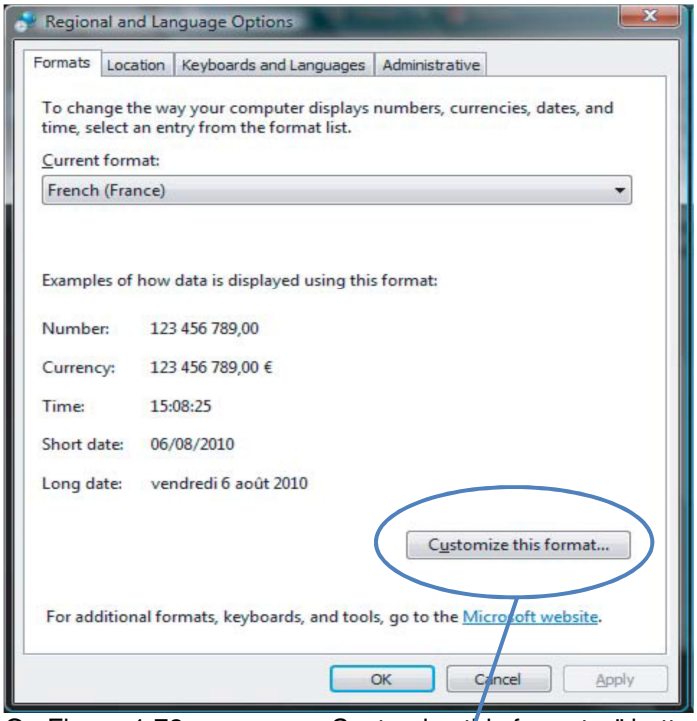


Warning: this installation is done for one USB connector only. If USB connector is changed, USB driver need to be re-installed before use.

4.6.2 Regional and Language options

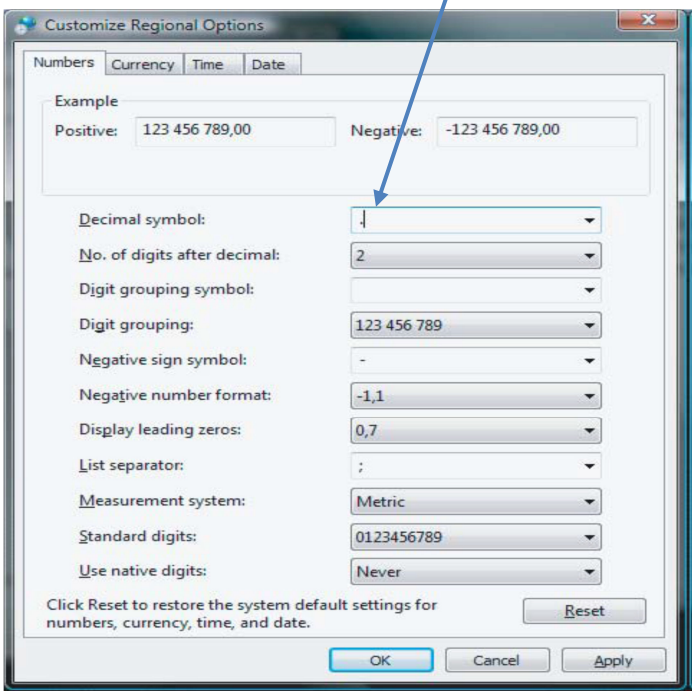
Use a control Regional Setting to check if decimal separator is configured with a dot ".".

Figure 4-72. Regional and Language options



On Figure 4-72, press on « Customize this format…" button to get the window displayed in Figure 4-73.

Figure 4-73. Customize Regional Options



Sheet Numbers: the decimal separator must be configured with a dot "."

4.6.3 Start-up procedure

Check that supplies are properly connected and powered ON.
Check that RF generators are properly connected and powered ON.
Check if USB connector is properly plugged.
Check if jumpers are configured as described in paragraph 3.5.

4.6.4 Measurement

If low dynamic performances and/or high interleaving spurs are obtained:

ADC used in OTP mode:

- Check that the temperature selected (Temperature High or Temperature Low) is suitable to the real junction temperature of the ADC (Temperature Low is recommended for ambient).
- If a Do Interpolation procedure has been launched, verify that the specified junction temperature is close to the real junction temperature of ADC.

ADC used in SPI mode:

- If ADC is used in SPI mode and if a Hardware reset is done, ADC calibrations will come back to their default values, meaning that ADC interleaving calibration is not appropriate.

If level of 2nd harmonic (H2) is high:

- Verify that your cables on Analog input are matched
- Verify that cables are fully tightened with an automatic reset wrench

- The SMA connectors Southwest can be unscrewed. If this is the case check their alignment on the PCB trace before screwing again the SMA connectors

Section 5

FFT calculations

This chapter describes how the different FFT parameters are calculated.
FFT parameters are calculated by using the formula below based on rms spectral components:

$Spectre_i = \sqrt{2}\frac{FFTModule_i}{N}$ (rms value)
With N = number of samples used in the FFT

Output spectrum expressed in dB or dBc are calculated with the following formula:

$$spectre_{dB\ pk} = 20\log\left(\frac{\sqrt{2} * spectre_i}{\frac{2^{Résolution}-1}{2}}\right) \quad ; \quad spectre_{dBc} = 20\log\left(\frac{spectre_i}{Max(spectre_i)}\right)$$

With $2^{Resolution}$, Resolution being the resolution of the ADC (12-bit)

5.1 Nomenclature

Sig Signal power = $\sum_{0}^{N} spectre_i^2$

H0 Power of DC component = $spectre_i^2$ with i =0 = index of the DC component

H1 Power of the fundamental = $spectre_i^2$ with i = index of the fundamental

H2 Power of 2nd harmonic = $spectre_i^2$ with i = index of the 2nd harmonic

Setup.cal/NbrOfHarmonics is the number of harmonics taken into consideration for THD calculation in the GUI.

Harmonics is the index of the harmonic in the spectra

H1i Power of 1st tone harmonics = $\sum_{Harmonics}^{setup.cal.NbrOfHarmonics} spectre_i^2$ (over Nyquist) with i = index of the i[th] harmonic of the first tone.

H2i Power of 2nd tone harmonics = $\sum_{Harmonics}^{setup.cal.NbrOfHarmonics} spectre_i^2$ (over Nyquist) with i = index of the i[th] harmonic of the 2[nd] tone.

H1i_NB Power of 1st tone harmonics in Narrow Band = $\sum_{Harmonics}^{setup.cal.NbrOfHarmonics} spectre_i^2$ (over Narrow Band)

H2i_NB Power of 2nd tone harmonics in Narrow Band = $\sum_{Harmonics}^{setup.cal.NbrOfHarmonics} spectre_i^2$ (over Narrow Band)

IMx Power of an intermodulated spur = $spectre_{i(x)}^2$ over Nyquist with x being the intermodulation iF1 ± jF2 with i & j integer

IMx_NB Power of an intermodulated spur in Narrow band = $spectre_{i\ (x)}^2$ at x index (over Narrow Band)

MaxSpur Level of the highest spur excluding the DC component and the fundamental (1[st] tone and 2[nd] tone if applicable) over the considered band of interest (Nyquist or Narrow Band if applicable)

PmaxSpur Power of the highest spur excluding the DC component and the fundamental (1st tone and 2[nd] tone if applicable) over the considered band of interest (Nyquist or Narrow Band if applicable)

Setup.cal.NbrOfInterleaving is the number of interleaving spurs taken into consideration in the calculation.
In single tone: Fc/2 ± F1, Fc/4 ± F1
In dual tone: Fc/2 ± F1, Fc/4 ± F1, Fc/2 ± F2, Fc/4 ± F2

Pint Power of interleaving spurs = $\sum_{Harmonics}^{setup.cal.NbrOfInterleaving} spectre_i^2$ (over Nyquist)

Pint_NB Power of interleaving spurs in Narrow band = $\sum_{Harmonics}^{setup.cal.NbrOfInterleaving} spectre_i^2$ (over Narrow Band)

5.2 Overlap of spurs

If there is an overlap of an interleaving spur with a harmonic (spurs having the same frequency), it is no more possible to discriminate the contribution of each spur. In that case, no calculation will be done and the overlap LED of the FFT parameter window will switch to RED color.

There is no issue if two spurs of same nature are overlapped (2 harmonics for instance). In that case, the power is taken into account once in the calculations.

5.3 Calculations

5.3.1 Initialisation of calculations

We define the following values;

- Pf : Power of the fundamental (2 tones if Dual tone)
- Mf : Power of the highest fundamental
- Ph : Power of harmonics
- Ph_NB: Power of harmonics in narrow band
- Ps : Power of spurs in narrowband (includes fundamentals, harmonics, intermodulation spurs and interleavings spurs if any but not DC component)
- Pn : Power of Noise (ie all spurs excluding DC component, fundamentals, harmonics, intermodulation spurs and interleaving spurs if any)
- Nb : Number of point for noise

The following calculations need to be done:

- $Pf = H1$
- $M_f = H1$
- $Ph = H1i$
- $Ph\_NB = H1i\_NB$
- $Nb = N_{Sig} - N_{H0} - N_{H1} - N_{H1i}$

5.3.2 Acquisition in Single or Dual tone?

Acquisition in Single or Dual tone?	
Single tone	**Dual tone**
$Pn = Sig - H0 - Pf - Ph$ $Ps = Ph\_NB$	$Pf = Pf + H2$ $M_f = Max(M_f; H2)$ $Ph = Ph + H2i$ $Ph\_NB = Ph\_NB + H2i\_NB$ $IM = \sum_{\substack{0<i,j<IMDOrder-1 \\ 2<i+j<IMDOrder}} IM_{iF1+jF2} + IM_{\lvert iF1-jF2\rvert}$ (Intermode Nyquist) $IM\_NB = \sum_{\substack{0<i,j<IMDOrder-1 \\ 2<i+j<IMDOrder}} IM\_NB_{iF1+jF2} + IM\_NB_{\lvert iF1-jF2\rvert}$ (Intermode bande étroite) $Pn = Sig - H0 - Pf - Ph - IM$ $Ps = Ph\_NB + IM\_NB$ $N_b = N_b - N_{H2} - N_{H2i} - N_{IM}$ $TIMD_{dBc} = 10\log\left(\frac{IM\_NB}{\mathrm{Pf}}\right)$ if IM_NB is different from 0 $IMD3(-)_{dBc} = 10\log\left(\frac{Mf}{max(Spur(2F1-F2); Spur(1F1-2F2))}\right)$ (For Narrow band, if one of the two IMD3 (-) spurs is not within the band, then it needs not to be taken into consideration. If no IMD3(-) spur is detected within the narrowband, IMD3 is not calculated)

5.3.3 Acquisition with 4 ADC cores aligned or interleaved?

Acquisition with 4 ADC cores interleaved?	
4 cores aligned	**4 cores interleaved**
Do nothing	$P_n = P_n - S_{int}$ $N_b = N_b - N_{int}$ With N_{int} the number of interleaving spurs Nint = 4 in single tone and 7 in Dual tones $Ps = Ph\_NB + S_{int}\_NB$ $TILD_{dBc} = 10\log\left(\frac{S_{int}\_NB}{Pf}\right)$ if Sint_NB different from 0

5.3.4 Performances calculation in dBc

- $SNR_{dBc} = 10\log\left(\frac{Pf}{Pn}\right)$
- With Narrow Band : $SNR_{dBc} = SNR_{dBc} + 10\log\left(\frac{\frac{Fc}{2}}{Bandwidth\ of\ Interest}\right)$ because we consider that thermal noise is dominant compared to jitter
- $THD_{dBc} = 10\log\left(\frac{Ph\_NB}{Pf}\right)$ If Ph_NB different from 0
- $TD_{dBc} = 10\log\left(\frac{Ps}{Pf}\right)$ If Ps different from 0
- $SINAD_{dBc} = -10\log\left(10^{-\frac{SNR_{dBc}}{10}} + 10^{\frac{TD_{dBc}}{10}}\right)$ Remove TD term if it was not possible to calculate it
- $ENOB_{dBc} = \frac{SINAD_{dBc} - 10\log(1.5)}{6.02}$
- $SFSR_{dBc} = 10\log\left(\frac{Mf}{(\frac{2^{Resolution}-1}{2\sqrt{2}})^2}\right)$
- $SFDR_{dBc} = 10\log\left(\frac{PmaxSpur}{Mf}\right)$

5.3.5 Performances calculation in dBFS

- $AverageNoise = 10\log(\frac{2*Pb}{N_b(\frac{Fc}{N})*(\frac{2^{Resolution}-1}{2\sqrt{2}})^2})$ (Noise floor)
- $SNR_{dBFS} = SNR_{dBc} - SFSR_{dBc} - 10\log\left(\frac{Pf}{Mf}\right)$
- $THD_{dBFS} = THD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$
- $TD_{dBFS} = TD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$
- $SINAD_{dBFS} = -10\log\left(10^{-\frac{SNR_{dBFS}}{10}} + 10^{\frac{TD_{dBFS}}{10}}\right)$
- $ENOB_{dBFS} = \frac{SINAD_{dBFS} - 10\log(1.5)}{6.02}$
- $SFDR_{dBFS} = SFDR_{dBc} + SFSR_{dBc}$
- $TIMD_{dBFS} = TIMD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$
- $TILD_{dBFS} = TILD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$
- $IMD3(-)_{dBFS} = IMD3(-)_{dBc} - SFSR_{dBc}$

Section 6

FPGA Code

FPGA code was developed to be used with a FPGA ALTERA ARIA V model 5AGXB3 (model used on the Evaluation Board).

6.1 FPGA functionalities

FPGA enables:

- Synchronization of FPGA _ ADC interface via its reset sequence and external SYNC (training)
- Acquisition of ADC data (sample and control bit) at 3.5GSps per port with a memory 256Ks
- To descramble the data for test mode PRBS and data
- To launch an acquisition directly (free run mode) or triggered by an event
- To transmit the acquisition data toward USB and restart the acquisition

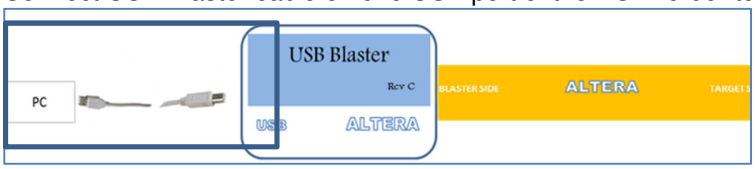
Limitation: FPGA does not support ADC clock frequency variation during the functioning.

6.2 FPGA programming

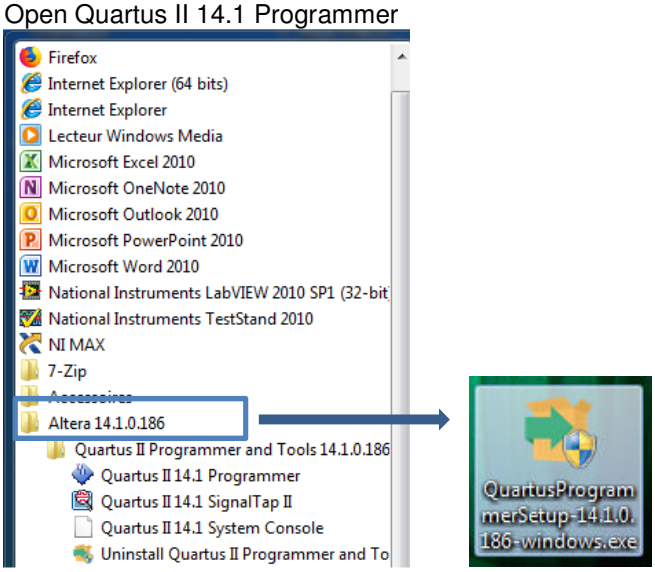
The FPGA programming can be done with Quartus Programmer. The file .pod is delivered on the CD-ROM of the Evaluation Board.
\FPGA\FPGA-v3.2\bin\fpga_top.pof

Below is the procedure to load the pof file into EEPROM.
Note: EV12AS350 Evaluation Board is delivered with FPGA code already loaded in the EEPROM. The procedure below is necessary in the only case when the user wants to download a new FPGA code.

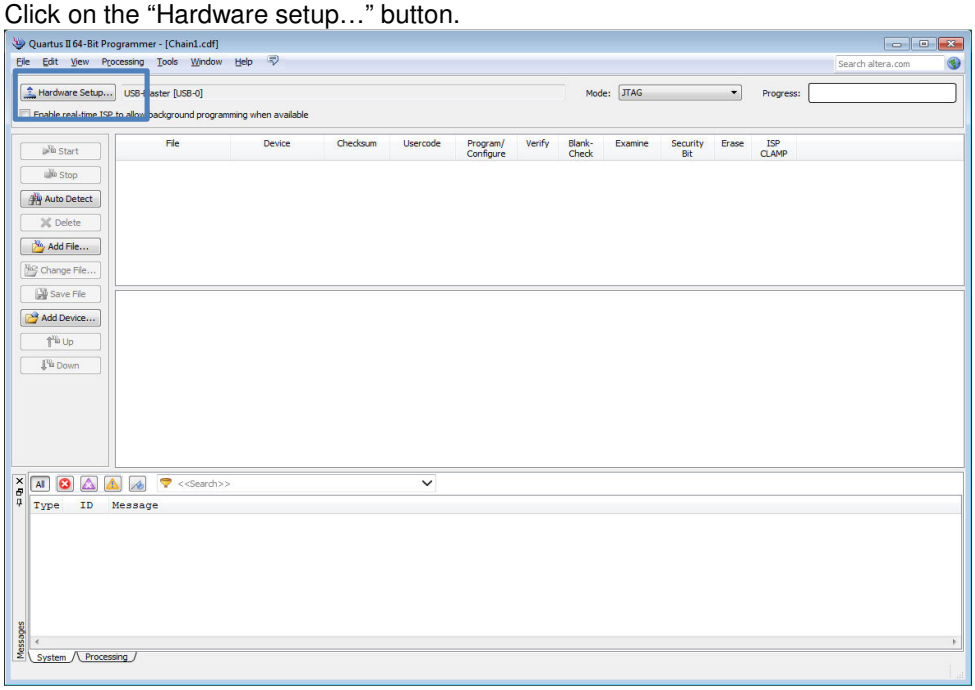
1. Connect USB Blaster cable on one USB port of the PC in order to be recognized by the software.



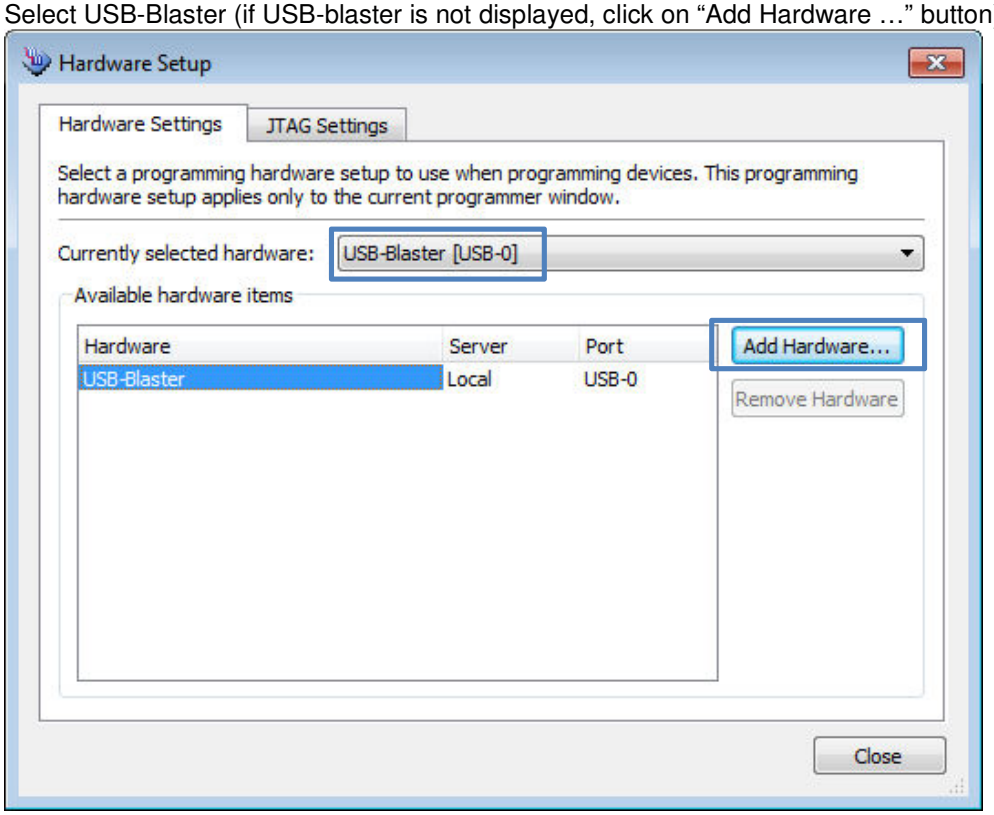
2. Open Quartus II 14.1 Programmer



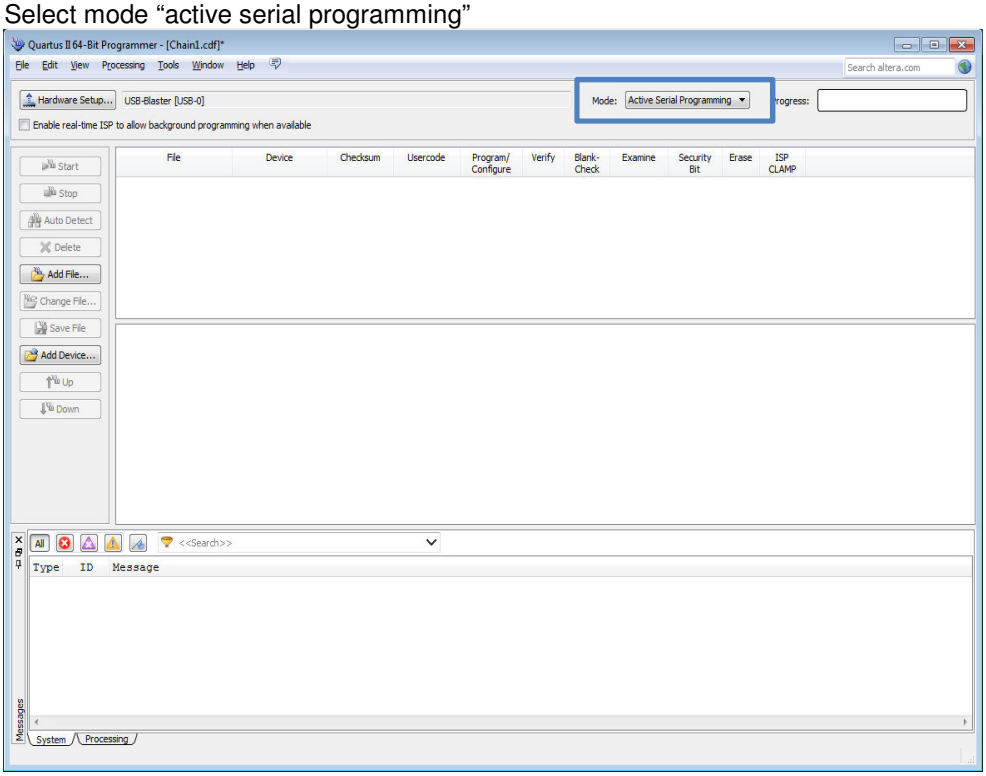
3. Click on the “Hardware setup…” button.



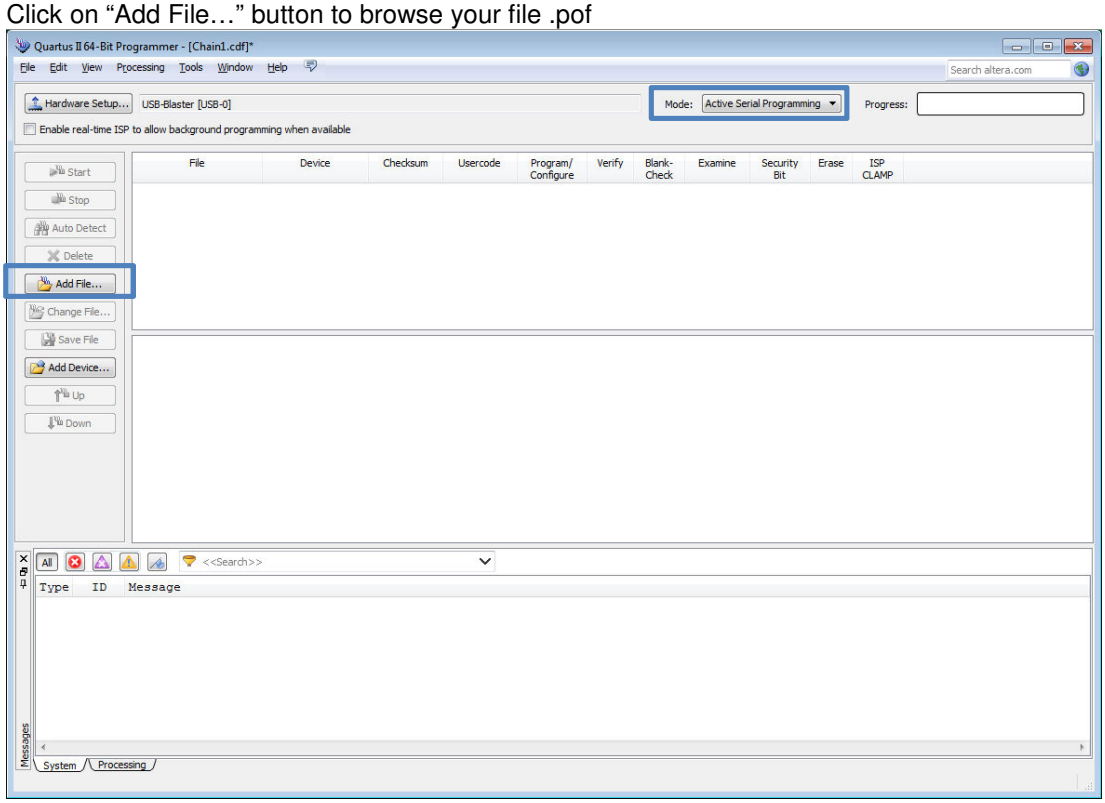
4. Select USB-Blaster (if USB-blaster is not displayed, click on “Add Hardware …” button)

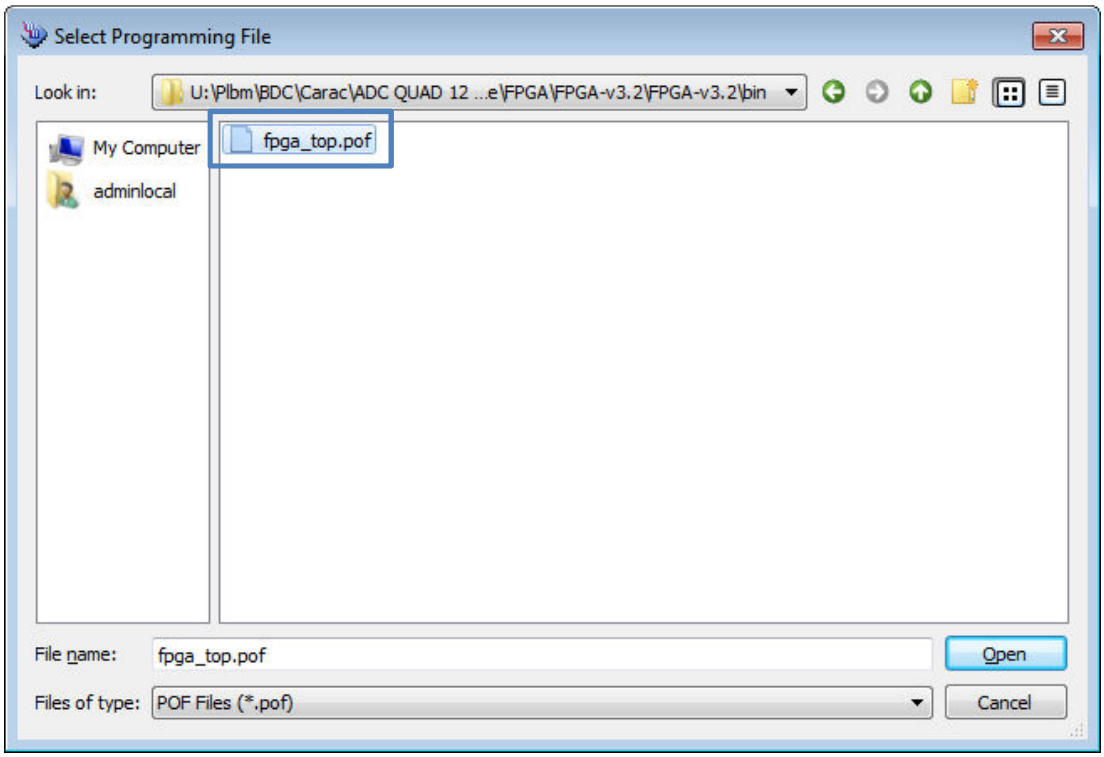


5. Select mode “active serial programming”

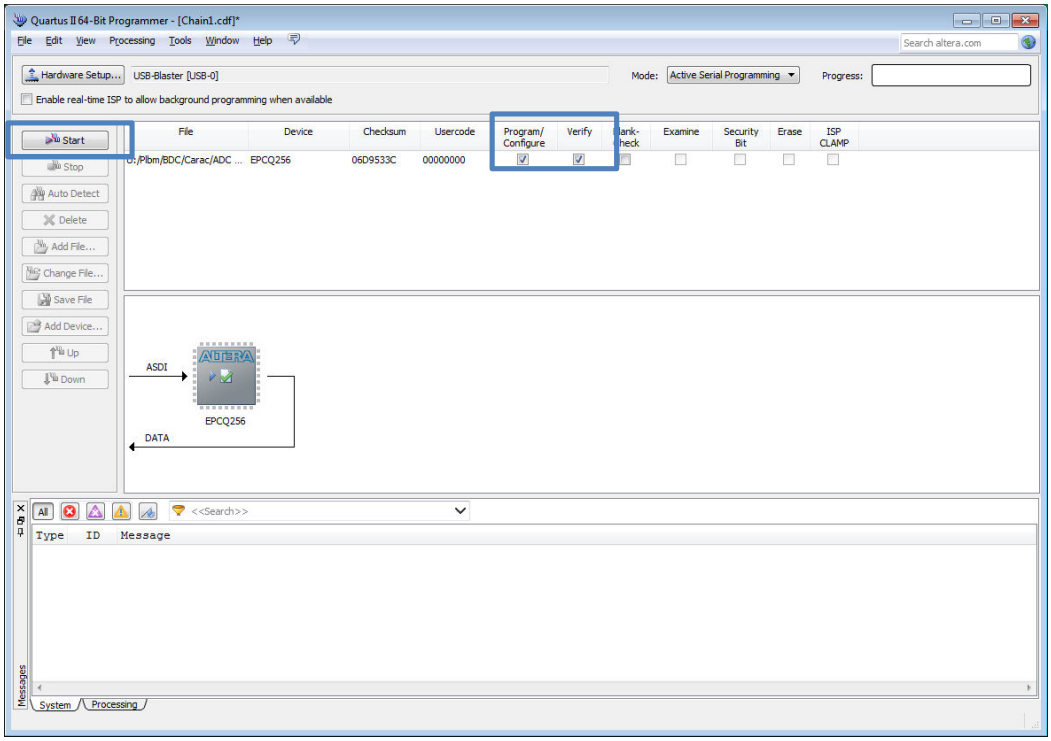


6. Click on “Add File…” button to browse your file .pof





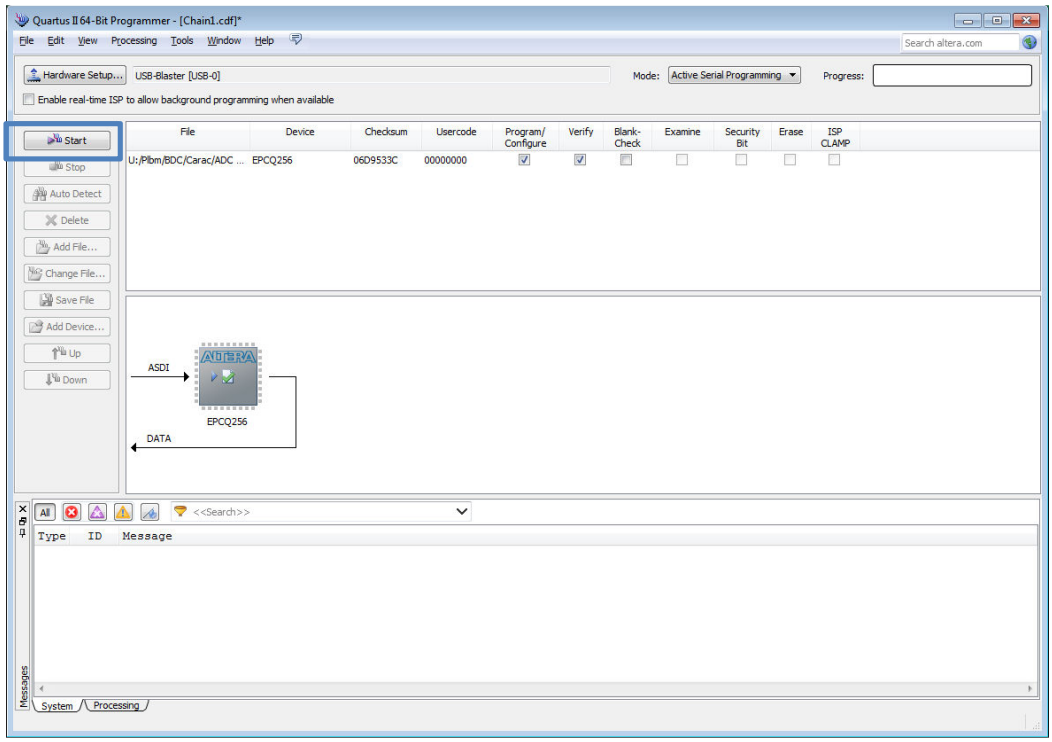
7. Click on “Program/Configure and Verify

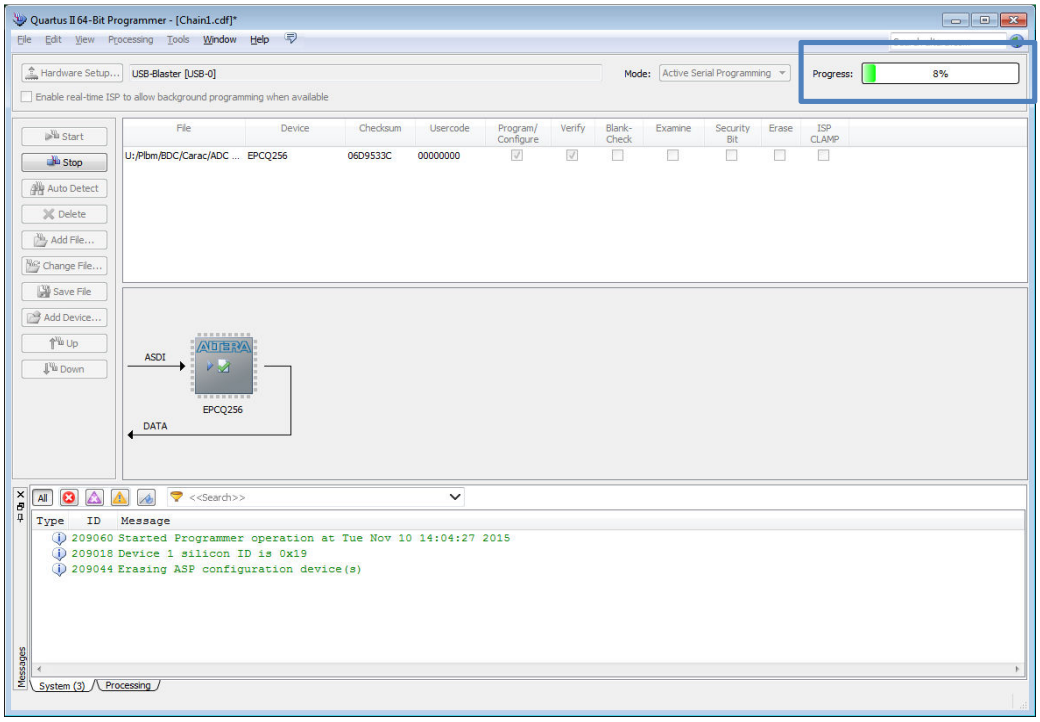


8. Connect USB Blaster on JTAG connector of the Evaluation Board

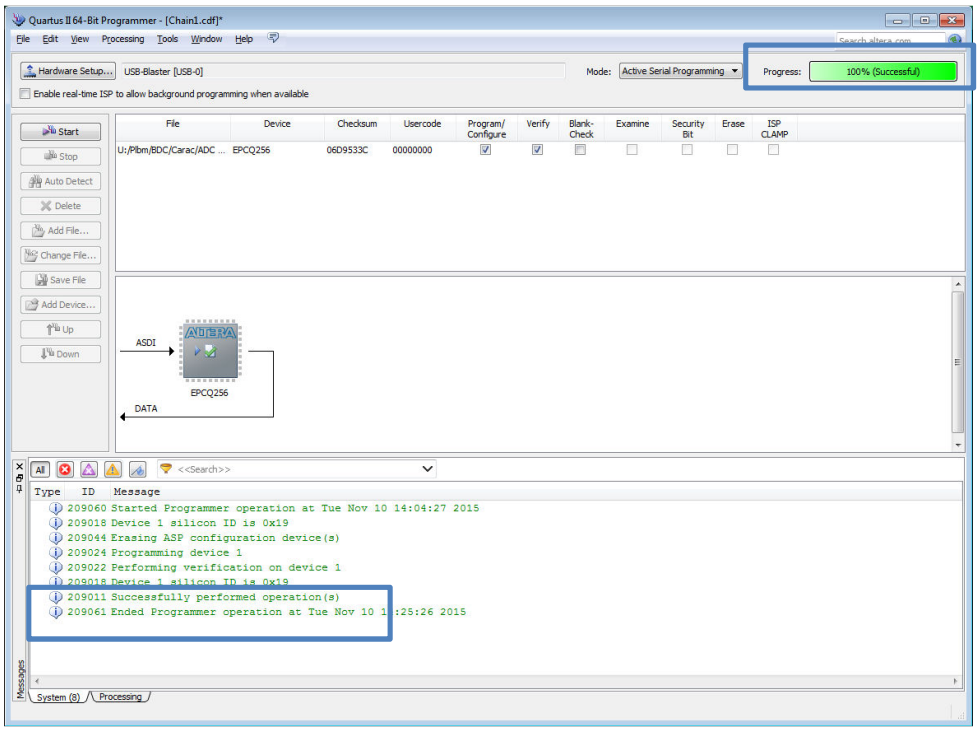
9. Power ON FPGA (5V5 supply)

10. Click on start





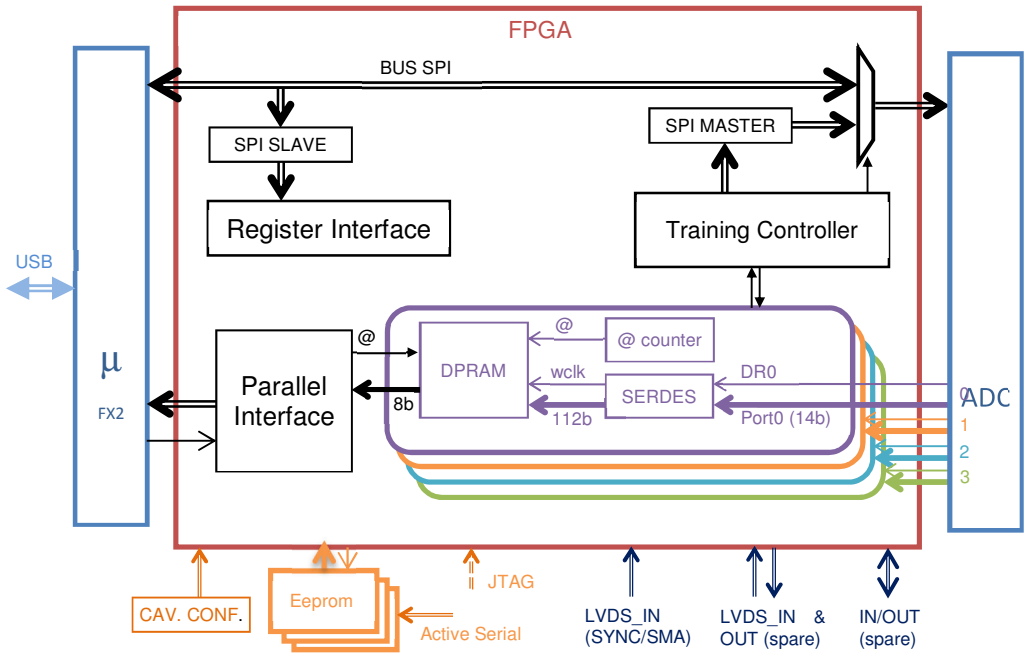
Once programming and verification are completed, the progress status displays 100% (successful). A message is also displayed in the bottom of the window.



6.3 FPGA VHDL code

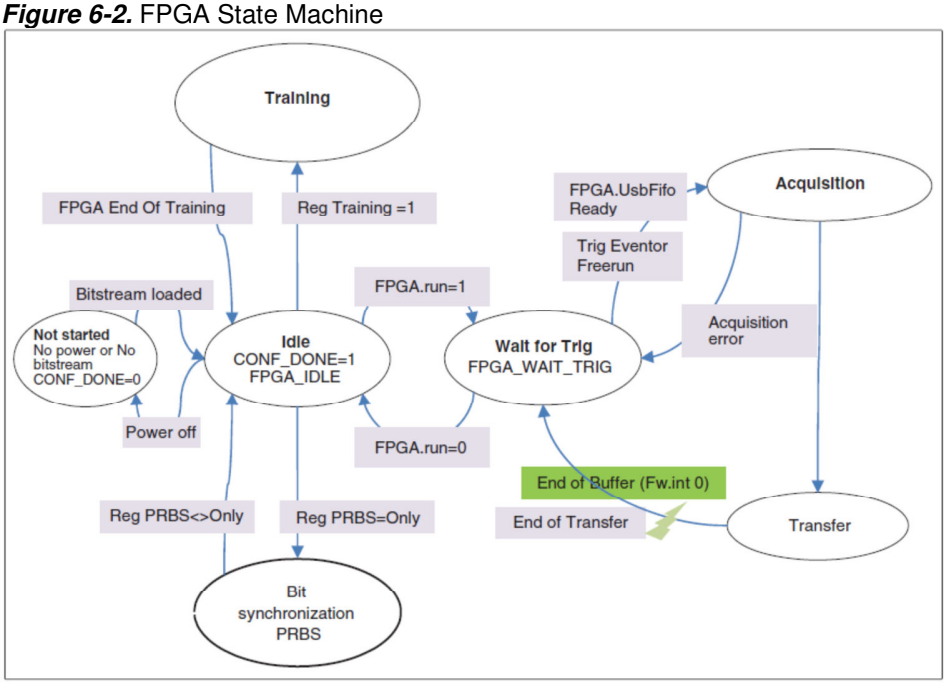
The Top level architecture of VDHL code is described below:

Figure 6-1. VHDL Top Level Simplified Block Diagram



FPGA State Machine is described below.

Figure 6-2. FPGA State Machine



The chosen configuration mode to program FPGA is Active Serial x4.

Arria V GX B3 Bitstream size is 138 416 696 bits.

The EEPROM memory is EPCQ256 with 268 435 456 bits (several EEPROM can be mounted to select different configurations).

Data is written into EEPROM by Active Serial Mode.

6.4 FPGA Training procedure

FPGA Training procedure is described below:

- IDLE
- SAVE CONTEXT
  - Read CHANNEL_SEL Register and store value
  - Write CHANNEL_SEL Register to 0 to select Channel A
  - Read TEST_MODE Register and store value
  - Read FLASH_LENGTH Register and store value
- INIT
  - Write CHANNEL_SEL Register to 4 to select all channels
  - Write FLASH_LENGTH Register to 23
  - Enable Test Mode
  - Do SYNC
- SET FLASH 23
  - Write TEST_MODE Register to 5 to select Flash Mode
- WAIT LOCK
  - Wait that all PLL and DPA are locked
  - Lock DPA values
- ALIGN BY PORT
  - Fill the whole buffer with incoming data
  - Search an address where all bits of the port are 0
  - Increment address
- **For each increment make a bitslip action for each 1 until all bits of the port are 1**
- SET RAMP
  - **Write TEST_MODE** Register to 9 to select Ramp Mode
- ALIGN ALL PORTS
  - Fill the whole buffer with incoming data
  - Read a data on each port at the same address, if it is too close to 0 read another data at another address until the data is enough far to 0
  - Freeze address counter of the earliest ports until the distance with the latest is less or equal to 4.
  - Apply bitslip on all bits of the earliest port until the gap between all ports is null
- CHECK RESULT
  - Fill the whole buffer with incoming data
  - Read all ports at a random address and check if the data is the same

- RESTORE CONTEXT
  - Restore FLASH_LENGTH Register
  - Restore TEST_MODE Register
  - Restore CHANNEL_SEL Register

- return to IDLE state

Section 7

Ordering Information

Table 1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AS350BTPY-EB	EBGA380 RoHS	Ambient	Prototype	Evaluation board mounted with EVP12AS350BTPY ADC