# EV12AS350BTPY-EB Evaluation Board 12-bit ADC 5.4GSps USER GUIDE





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# Section 1

# **General Overview**

The EV12AS350BTPY-EB Evaluation Board enables the easy evaluation of the characteristics and performance of EV12AS350 12-bit ADC. The Evaluation Board is plug\_and\_play and needs little external equipment.

The Evaluation Board is delivered with software which allows acquisition of data using the FPGA and Graphical User Interface (GUI). The FPGA VHDL data acquisition code is supplied with the Evaluation Board.

### 1.1 Disclaimer

Whilst Teledyne e2v thas taken care to ensure the accuracy of the information contained herein it accepts no responsibility for the consequences of any use thereof and also reserves the right to change the specification of goods without notice. Teledyne e2v accepts no liability beyond the set out in its standard conditions of sale in respect of infringement of third party patents arising from the use of tubes or other devices in accordance with information contained herein.



General Overview

# 1.2 EV12AS350 ADC

The EV12AS350B-EB Evaluation Board is based on Teledyne e2v EV12AS350 12-bit 5.4Gsps ADC whose block diagram is given on figure 1-1.





The ADC is made up of four identical 12-bit ADC cores where all four ADCs are all interleaved together.

All four ADCs are clocked by the same external input clock signal delayed with the appropriate phase.

The Clock Circuit is common to all four ADCs. This block receives an external 5.4 GHz clock (maximum frequency) and preferably a low jitter sinewave signal. In this block, the external clock signal is then divided by 4 in order to generate the internal sampling clocks.

The in-phase 1.35 GHz clock is sent to ADC A while the inverted 1.35 GHz clock is sent to ADC B; the in-phase 1.35 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1.35 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 5.4 Gsps.

Note: This document should be used in conjunction with the other documentation relating to this product, Datasheet, Application notes ... etc. Several adjustments for the sampling delay and the phase are tuned during initial manufacturing test in this clock circuit to ensure a proper phase relation between the different clocks generated internally from the 5.4 GHz clock.







Please refer to datasheet 1209A for more information on EV12AS350B 12-bit ADC.

### 1.3 Evaluation Board

The Evaluation Board is based on an EV12AS350B ADC with a FPGA Altera Arria V.

The Evaluation Board includes:

- PCB with a soldered EV12AS350B ADC and a FPGA Altera Arria V model 5AGXB3
- USB cable for the communication between the board and the PC (ADC settings and configuration, settings for data acquisition and data transmission)
- Analog input with two SMA connectors (differential input)
- Clock input with two SMA connectors (differential input)
- CD-ROM with GUI

```
Figure 1-3. Architecture of EV12AS350 - Evaluation Board
```







Acquisition and formatting of ADC digital output data are done within the FPGA.

A USB driver on the ADC Evaluation Board allows for transmission of the data to the computer that performs the display and processing of ADC output data (FFT).

Software and Graphical User Interface are provided with the Evaluation Board.

The provided software operates using Labview® RunTime (no license required).

FX2 microcontroller is used:

- To do the reset sequence (SYNC) of the ADC
- To detect the ADC
- To control and configure ADC settings via its SPI which is driven by the FPGA
- To control the FPGA by SPI
- To ensure the transmission of acquisition data from FPGA to PC via the USB port
- To communicate with the PC via USB port

Figure 1-5. EV12AS350 - Evaluation Board dimensions





*Figure 1-6.* EV12AS350 - Evaluation Board photo (TOP VIEW)

EV12AS350BTP-EB Evaluation Board



Quick start



# Section 2

Quick start

## 2.1 Required equipment

The EV12AS350 - Evaluation Board requires the following equipment to operate:

- A RF generator for the clock
   To get optimum dynamic performances, a low phase noise generator is mandatory.
   A balun is mandatory to provide a differential clock to the Evaluation Board.
- A RF generator for the analog input To get optimum dynamic performances, a low phase noise generator is mandatory. A balun is mandatory to provide a differential analog input to the Evaluation Board. A filter is also necessary on analog input.
- Cables for power requirements (both ADC and FPGA power)
- USB cable to connect the Evaluation Board to the PC
- The differential analog and clock input are provided by SMA connectors Southwest SMA 2.92 mm.
- Incoming power supplies are bypassed by the banana jack (2mm-5A-EFJ or EMBASE-4mm-10A-DLT)
- A PC operating with Windows XP or Windows 7 (32 ou 64 bits)

Optionally:

• A multimeter to monitor the ADC junction temperature

#### Table 2-1. Examples of RF generators for CLK or VIN

Signal generator	SSB phase noise @1GHz (20 KHz offset)
Agilent E4424B 250KHz 2GHz (High spectral purity)	< -134dBc/Hz
Agilent E4426B 250KHz 4GHz (High spectral purity)	< -134dBc/Hz
Rohde & Schwarz SMA100A 9 KHz 6GHz (High spectral purity)	< -140dBc/Hz

#### Table 2-2. Examples of balun for CLK and VIN

Balun reference	Frequency range
BROADBAND BALUN MARKI (BAL0006)	200KHz – 6GHz
MACOM 96341 - H9	2MHz – 2000MHz
ANAREN 3A0056 – 3dB coupler	2GHz – 4GHz

#### Table 2-3. Examples of power supplies current

Power supplies current
Rohde & Schwarz HMP4040
GWInstek PST3202

EV12AS350BTP-EB Evaluation Board



# 2.2 Evaluation Board connections setup

### 2.2.1 Power supplies

Connect Evaluation Board power supplies as described below:

- Connect a 2V power supply to connectors VCCO and VCC\_COEUR
- Connect a 3.2V power supply to connector VCCD
- Connect a 4.8V power supply to VCCA
- Connect a 5.5V power supply to connector 5v5 (FPGA power supply)

Note: It is not necessary to connect GND and GNDO grounds (it is done within PCB). It is mandatory to connect DIODEC to GND as shown on Figure 2-1, even if temperature is not monitored.



Figure 2-1. Photo of EV12AS350 board with connections

Note: VCCFUSE\_7V5 connector and its GND (left side of PCB) needs to remain unconnected.



### 2.2.2 Clock input

Connect clock RF generator to Evaluation Board SMA (label CLK\_P, CLK\_N) via SMA cables and balun. A filter can be added on input clock, but it is not mandatory.

### 2.2.3 Analog input

Connect Analog Input RF generator to Evaluation Board SMA (label VIN\_P, VIN\_N) via SMA cables and balun. A filter is mandatory.

### 2.2.4 USB

Use the USB cable (provided with Evaluation Board) to connect PCB to the PC.

### 2.2.5 SYNC input

It is possible to apply a SYNC signal either by GUI, either by a potentiometer button on PCB, or by an external signal. In that case the external signal has to be connected to Evaluation Board on SMA label SYNC\_P, SYNC\_N. In other cases, these SMA connectors can remain unconnected.

### 2.2.6 Temperature Diode monitoring

A multimeter can be used to monitor the ADC junction temperature. In that case, it has to be connected between connectors DIODEA and DIODEC. It is mandatory to connect DIODEC to GND as shown on Figure 2-2. The Diode Characteristic is provided below (for I = 1 mA)





#### Figure 2-2. Temperature Diode characteristic for I = 1 mA (with DiodeC=GND)



#### Operating procedure

- 1. Install the Software as described in Section 4 Software Tools.
- 2. Connect power supplies, clock, analog input and USB cable as described in chapter 2.2.
- 3. Turn ON 5.5V FPGA power supply
- 4. Turn ON ADC power supplies
- 5. Turn ON clock generator
- 6. Turn ON Analog input generator
- 7. Press "RESET" button on bottom right corner of PCB
- 8. Launch Setup\_EV12AS350x-EB\_GUI\_v1.6.0.exe
- 9. Press « Hardware Reset » button from GUI (recommended in order to configure the ADC in default mode)
- 10. Verify that ADC currents are in accordance to the EV12AS350 datasheet available online.
- 11. Configure ADC in the desired mode
- 12. Press « SYNC» button from GUI (recommended for a proper synchronization of the 4 ADC cores)
- 13. Launch an acquisition and verify that the signal is correct and that the performance math the datasheet.





# Section 3

# Hardware Implementation

The Evaluation Board can be hardware configured by changing manually some capacitor or resistance. This chapter allows seeing all hardware configurations.

All Hardware modifications are made at user's risk.

## 3.1 Analog Input

Two SMA connectors are provided to access VIN and VINN. It is mandatory to use a differential signal (A balun can be used to provide differential signal. See example of balun references in Table 2-2 above.

The Analog Input is by default AC coupled (10nF AC coupling capacitors C79 and C82).



*Figure 3-1.* Evaluation Board Analog input schematic with AC coupling

It is possible to consider a DC coupled input impedance. In that case it is necessary to remove C79 and C82 capacitors and replace them by 0 ohm resistors. After this hardware modification, it is necessary to apply a common mode either through a T-bias either through output CMIRef which is the image of the internal ADC common mode of the ADC.

The figure 3-2 below shows the location of C79 and C82 capacitors and CMIRef outputs.



3-1

EV12AS350BTP-EB Evaluation Board



Figure 3-2. Photo of Analog input and CMIRef outputs

# 3.2 Clock Input

Two SMA connectors are provided to access CLK and CLKN. It is mandatory to use a differential signal (A balun can be used to provide differential signal. See example of balun references in Table 2-2 above).

The Clock Input is AC coupled with 10nF AC coupling capacitors.

As for Analog Input, it can be possible to consider a DC coupled impedance. Procedure is the same for Clock as for Analog input and is already described in chapter 3.1.





*Figure 3-3.* Evaluation Board Clock input schematic

Figure 3-4. Photo of Clock Input is AC coupled with 10nF AC coupling capacitors





Hardware configuration

# 3.3 SYNC Signal

There are three ways of doing a SYNC on EV12AS350 - Evaluation Board:

- SYNC signal sent by the FPGA (Driven by SYNC button from GUI) = recommended option
- SYNC signal generated on board by a potentiometer (no need of external signal)
- External SYNC signal via SMA connectors





*Figure 3-6.* Evaluation Board SYNC input photo





### 3.3.1 SYNC Signal sent by FPGA (GUI driven = default hardware configuration)

When pressing the SYNC button from the GUI, the FPGA generates a pulse that is sent to the ADC via the FX2 microcontroller. This is the hardware configuration by default. In this configuration it is mandatory to have R197 =  $0\Omega$  and R204 =  $0\Omega$  (See Figure 3-5). It is not necessary to remove below resistors and capacitors to get a proper operation: R196 =  $0\Omega$ , R198 =  $200\Omega$ , R199 =  $200\Omega$  and R200 =  $200\Omega$ . C60 = 10 nF and C63 = 10nF.

This is the recommended option.

### 3.3.2 SYNC Signal generated on board

A SYNC signal can be generated via a potentiometer (P1 on Figure 3-5). This solution is based on the fact that SYNCP voltage has to be higher than SYNCN voltage in order that the ADC detects a SYNC command. This option is less accurate than GUI-driven SYNC because of rebound issues.

With this option it is mandatory to have R196 =  $0\Omega$ , R198 =  $200\Omega$ .

It is not necessary to remove below resistors and capacitors to get a proper operation:

R197 =  $0\Omega$ , R204 =  $0\Omega$ , R199 =  $200\Omega$  and R200 =  $200\Omega$ .

C60 = 10 nF and C63 = 10 nF.

### 3.3.3 External SYNC Signal

Two SMA connectors are provided to access SYNC\_P and SYNC\_N of the ADC (serigraphy SYNC\_EXT\_N and SYNC\_EXT\_P). With this option, a pulse generator needs to be connected to SMA in order to apply a LVDS pulse.

It is recommended to remove R196, R198, R199 and R200 to avoid any interference between potentiometer and pulse generator. Additionally, it is necessary to replace C60 and C63 by 0Ω resistors.

Be careful: FPGA needs to drive the SYNC signal between each training phase. This configuration with external SYNC is therefore not recommended.

Note: If FPGA is not powered ON, relay RL1 of figure 3-5 is in mode external SYNC.

## 3.4 Spare SYNC Signal for FPGA

A spare SYNC differential signal connected to FPGA is provided on the Evaluation Board in order to allow user to develop its own system. This spare signal is accessible through 2 SMA connectors (serigraphy SPARE SYNC\_FPGA\_P and SPARE SYNC\_FPGA\_N).

Contact Teledyne e2v hotline Hotline-BDC@Teledyne-e2v.com for more information on this functionality.

## 3.5 Jumpers configuration

The figures 3-7 and 3-8 below present the required jumpers configuration. Evaluation Board is delivered with this default configuration that must not be changed.



#### Hardware configuration

*Figure 3-7.* Evaluation Board jumpers configuration (photo)







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# Section 4

Software Tools

## 4.1 Introduction

The Evaluation Board requires two software tools to operate:

- Graphical User Interface: the user interface software is a Visual C++<sup>®</sup> compiled graphical interface that does not require a licence to run on a Windows<sup>®</sup> XP/7<sup>®</sup>; Office 2010 and later PC. The software uses intuitive push-buttons and pop-up menus to configure the ADC and do data acquisition. To save acquisition data on Excel files, it is mandatory to have a Microsoft Excel version 2007 or more recent.
- A FPGA code: the FPGA code is provided with the Evaluation Board. Evaluation Board is delivered with FPGA code already downloaded within the FPGA. See Section 6 about FPGA code to have explanations on how to download a new FPGA code version.

Warning: for the software installation, administrative rights are mandatory. Warning: if the software is already installed, the window below appears.



Setu	ring to Install ip is preparing to install EV12AS350x-EB GUI on your computer.	B
8	The following applications are using files that need to be updated by Setup. It recommended that you allow Setup to automatically close these applications. After the installation has completed, Setup will attempt to restart the applications.	is
	Eval Quad ADC12bit Eval Quad ADC12bit Eval Quad ADC12bit	^
		-
	4	
	<u>Automatically close the applications</u>	
	Do not close the applications	
	< Back Next > 0	Cancel



#### FFT calculations

It is necessary to remove previous versions prior to installing a new version.

Click on	Cancel
Exit Setup	
?	Setup is not complete. If you exit now, the program will not be installed. You may run Setup again at another time to complete the installation. Exit Setup?
	Qui Non
Click on	Qui



# 4.2 Getting Started

Install the User interface (EV12AS350-EB GUI) application on your computer by launching the Setup\_EV12AS350x-EB\_GUI\_v1.6.0.exe install).

The screen shown in Figure 4-2 is displayed:





EV12AS350BTP-EB Evaluation Board



### Figure 4-3. Evaluation Board EV12AS350x-EB GUI "Destination Directory" window

Setup	x
Select Start Menu Folder Where should Setup place the program's shortcuts?	B
Setup will create the program's shortcuts in the following Start Menu folder.	
To continue, click Next. If you would like to select a different folder, click Browse.	
Teledyne e2v/EV12AS350x-EB_GUI Browse	
< <u>B</u> ack <u>N</u> ext > Cancel	

Setup	×
Select Additional Tasks Which additional tasks should be performed?	
Select the additional tasks you would like Setup to perform while installing EV12AS350x-EB GUI, then click Next.	
Additional icons:	
Create a desktop icon	
< <u>B</u> ack Next > C	Cancel





Figure 4-3. Evaluation Board EV12AS350x-EB GUI installation

Setup X
Installing Please wait while Setup installs EV12AS350x-EB GUI on your computer.
Extracting files C:\Users\ADMINL~1\AppData\Local\Temp\is-IOBAU.tmp\LVRTE2010_SP1f5std.exe
Cancel



#### FFT calculations





Setup	x
	Completing the EV12AS350x-EB GUI Setup Wizard Setup has finished installing EV12AS350x-EB GUI on your computer. The application may be launched by selecting the installed shortcuts. Click Finish to exit Setup. ☑ View the README file ☑ Launch EV12AS350-EB GUI
	Finish

Figure 4-5 EV12AS350x Evaluation Board "README file"





#### Figure 4-6 EV12AS350x Evaluation Board "Launch EV12AS350-EB GUI"

In the following example, LabView is installed on the computer. In this case, all installation steps can be skipped by clicking on 'Cancel'.

Otherwise, the user just needs to select the applications to be installed and click on 'next' until the end of the procedure.



Moteur d'exécution de NI LabVIEW 2010 SP1	
Répertoire de destination Sélectionnez le répertoire d'installation principal.	
Répertoire de destination	
C:\Program Files (x86)\National Instruments\	Parcourir
<< <u>P</u> récéde	nt <u>Suivant &gt;&gt;</u> Annu <u>l</u> er





Moteur d'exe	cution de NI LabVIEW 2010	SP1	
<b>Notif</b> Veu sélé	cations concernant les pro illez lire les informations suivante ctionnée.	duits s concernant la configuration	
☑ Demand les mises accepte de Natio	er à l'installeur de contacter Nati à jour relatives aux produits Nat que votre adresse IP soit envoj nal Instruments.	onal Instruments pour recherche tional Instruments à installer. En yée et recueillie conformément à	r les nouvelles notifications et cochant cette option, vous la politique de confidentialité
		ŝ	Politique de confidentialité
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B Moteur d'exécution de NI LabVIEW 2010 SP1	
Démarrer l'installation Veuillez vérifier le résumé suivant avant de continuer.	
Impossible d'installer • Moteur de variables NI (version ultérieure déjà installée) • DataSocket (version ultérieure déjà installée) • USI (version ultérieure déjà installée)	
Enregistrer le <u>fi</u> chier) << <u>P</u> récédent <u>S</u> uir	vant >> Annuler
Moteur d'exécution de NI LabVIEW 2010	
Êtes-vous sûr de vouloir annuler ?	
Qui Non	

#### Installation is ready

Setup is now completed successfully. You can start application by double clicking on the following icon on your desktop.





## 4.3 USB driver installation

After the installation, EV12AS350x Evaluation Board can be powered up and connected to PC with USB cable.

At the first connection a USB driver installation will be launched.

Warning: if the Evaluation Board is connected to another USB connector this installation must be re-started. The installation is normally fully automatic. If it is not launched automatically, please proceed as described below.

The window shown in Figure 4-7 will be displayed.





Please choose: Locate and install driver software (recommended)

Figure 4-8. Allow Windows to Search Driver



Please choose: Yes, always search online (recommended)

EV12AS350BTP-EB Evaluation Board







Please choose: Browse my computer for driver software (advanced)

#### Figure 4-10. Choose the Folder

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Microsoft Sync Framework	^ Nom	Туре	Taille			
Microsoft Synchronization Services	amd64	Dossier de fichiers				
J Microsoft.NET	Rin	Dossier de fichiers				
🕌 Minitab 16	data	Dossier de fichiers				
퉬 Mozilla Maintenance Service	1386	Dossier de fichiers				
J MSBuild	INI c	Dossier de fichiers				
USECache MSECache	Vml	Dossier de fichiers				
퉬 National Instruments	ew constraiousdopcia client are	Application	025 Ko			
NVIDIA Corporation		Eiskiss ALTACES	303 K0			
Reference Assemblies		Estancian de l'application	10.024 Ka			
Ja SAP	DK_Processing.ai	Deservation de configuration	10 024 KO			
🚹 Snapshot Viewer	EvelEv(12AS250 inf	Informations de configuration	1 KO			
🍌 Teledyne e2v	avalaused at 2 bit ast	Catalagua da sécurité	2 K0			
EV12AS350x-EB_GUI	EvalQuadADC12bitCliant bat	Catalogue de securite	9 KU			
퉬 amd64		Desument texts	I KO			
퉬 Bin		Application	10 Ko			
🌗 data		Application Extension de l'angliention	2 220 K-			
鷆 i386	Creater an	Extension de l'application	2 239 KU			
🕌 INLs	QtGul4.dll     QtAleture.dl4.dll	Extension de l'application	0 USI KO			
퉬 Xml		Extension de l'application	935 KO			
🎍 Uninstall Information	Succession and Succession	Extension de l'application	005 K0			
퉬 VulkanRT	S QtSvg4.dll	Extension de l'application	270 KO			
퉬 Windows Defender	Strett-di	Extension de l'application	101 KO			
🎍 Windows Mail	(%) QtXml4.dll	Extension de l'application	332 Ko			
퉬 Windows Media Player	w qwt.dll	Extension de l'application	628 Ko			
\mu Windows NT	≅ qwtmathml.dll ≡ ™ D = MA + + +	Extension de l'application	188 Ko			
🕌 Windows Photo Viewer	KeadMe.txt	Document texte	4 Ko			
Windows Portable Devices	uninsuu.dat	Fichier DAT	151 Ko			

Select C:\Program Files (x86)\Teledyne e2v\EV12AS350x-EB\_GUI



#### Figure 4-11. Warning: Installation



Please choose: Install the driver software anyway.

Please wait during the data transfer.



🚔 Gestionnaire de périphériques
Fichier Action Affichage ?
4 G4035T
Appareils mobiles
Cartes graphiques
Cartes reseau
Castellaura audia adda at inc
Controleurs audio, video et jeu
Eval Quad ADC12bit
Intel(R) ICH10 Family USB Enhanced Host Controller - 3030
Intel(R) ICH10 Family USB Enhanced Host Controller - 3A3C
Intel(R) ICH10 Family USR Universal Host Controller - 3A34
Intel(R) ICH10 Family USB Universal Host Controller - 3A35
Intel(R) ICH10 Family USB Universal Host Controller - 3A36
Intel(R) ICH10 Family USB Universal Host Controller - 3A37
Intel(R) ICH10 Family USB Universal Host Controller - 3A38
Intel(R) ICH10 Family USB Universal Host Controller - 3A39
Périphérique de stockage de masse USB
Contrôleurs de stockage
Lecteurs de disque
Lecteurs de DVD/CD-ROM
D Moniteurs
National Instruments GPIB Interfaces
> 1 Ordinateur
Périphériques d'interface utilisateur
Périphériques système
Ports (COM et LPT)
Processeurs
Souris et autres périphériques de pointage
l The years driven have been installed

The new driver has been installed.

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After the installation, the interface can be launched with the following file: C:\Program Files (x86)\Teledyne e2v\EV12AS350x-EB\_GUI\EvalQuadADC12bitClient.bat. The window shown in Figure 4-13 will be displayed.



Figure 4-13. EV12AS350x-EB Graphical User Interface (GUI)

- EV12AS350x-EB GUI		
File ?		
Teledyne EV12AS350x e2v	-EB GUI	Hardware Reset Do Interpolation     Refresh SYNC
Start Start	Stop Snap	Software Trig Do Training
Setting Test LUT Interleav	ng Calibrations Acquisition Export De	bug
CLOCK mode : No Interleaving (Aligned dock) Interleaving Standby : No Standby Full Standby Swing Adjust Disabled Enabled	Software Reset       CLOCK division : <ul> <li> <ul></ul></li></ul>	


# 4.4 GUI Overview

The EV12AS350x-EB GUI software included with the Evaluation Board provides a Graphical User Interface to configure the ADC.

Push buttons, popup menus and capture windows allow easy configuration of the ADC, data acquisition and data exportation.

The User Interface window is made of different menus and tabs that are described in the figure 4-14 below.

- Tool bar
- Header menu
- System menu
- Several navigation tabs
  - Settings
  - o Test
  - o LUT
  - o Interleaving calibrations
  - Acquisition
  - Export
  - o Debug
- Status Menu



EV12AS350x-EB GUI		<b>- - X</b>	Tool Bar
Teledyne EV12AS350x	-EB GUI	Hardware Reset Do Interpolation     Refresh SYNC	Header Menu
System Start	Stop Snap	Software Trig Do Training	System Menu
Setting Test LUT Interleav CLOCK mode : No Interleaving (Aligned dock) Interleaving Standby : No Standby Full Standby Swing Adjust Disabled Enabled	ing Calibrations Acquisition Export Det Software Reset CLOCK division : No Divided Divided by 2 Settings : Reset Length 8 ↓ Analog Input : CM_IN 16 ↓ 16 R_IN 8 ↓ 8 Write Read	Jug	Navigation tabs
	ChipID:6.3.4 FPGA:1:3.2 FW:1.0:	9 CRC 🥃 Sync 曼 OTP 🍙 System : 🗬 🖨	Status Menu



# 4.4.1 Tool bar description

The "File" Menu provides the following choices:

*Figure 4-15.* EV12AS350x-EB File Menu



- "Load context": used to load an existing context file (file.ctx) and then,modify ADC calibrations. (ADC calibration context is useful in the only case when the user wants to apply its own calibrations via the SPI mode).
- "Save As...": used to save a context file of ADC calibrations in giving a name to the context file (file.ctx).
- "Save context": used to save a context file (file.ctx) of ADC calibrations (accessible once a file named as already been given using the "Save As..." option).
- "Quit": used to close the Graphical User Interface window.

A context file saves all the configurations accessible via the GUI (Settings, Acquisition...) and can be used to reuse a given configuration without changing manually all the configurations.

The «? » Menu enables to display the version of the GUI software.

File ?	50x-EB GUI
About EV12	AS350x-EB GUI
Teledyne e2v	EV12AS350x-EB GUI <b>1.6.0</b>
	ОК

Figure 4-16. EV12AS350x-EB "?" Menu



### 4.4.2 Header Menu description

Figure 4-17. User Interface Header Menu

	OTP    Hardware Reset  Do Interpolation
e2v EVIZASSSOX-EB GOI	Temperature Low  Refresh SYNC

The Header Menu enables:

- ADC initialization via a "SYNC": pressing this button generates a SYNC pulse on the ADC (See chapter 3.3.1)
- "Hardware Reset": pressing this button generates a reset signal on the SPI of ADC. All changes made on SPI values are erased and SPI values come back to their default values. Pressing this button also switch ADC in OTP mode (default mode)
- The selection between "OTP" or "SPI" register values (OTP SPI SEL register within ADC)
- The configuration of calibrations in OTP mode: choice between one of the two sets of calibration ("Temperature Low" or "Temperature High") "Do interpolation": ADC calibrations are interpolated at the temperature of use (in SPI mode)
- "Refresh": the GUI is refreshed according to ADC registers

For more information about ADC calibrations (OTP, SPI, Do interpolation ...) please refer to chapter 4.5.4.

When OTP is selected:

The two sets of calibration ("Temperature High" or "Temperature Low") is accessible

The process of calibrations interpolation (via "Do interpolation" procedure) is not accessible Note: R IN and CM IN values (Settings tab) are the values written within OTP and cannot be modified in OTP mode.

When SPI is selected:

- The two sets of calibrations (Temperature Low or Temperature High) are no more accessible
- Pop-up window of Figure 4-18 proposes two choices:
  - Launch a "Do interpolation" procedure at the temperature of use. See chapter 0 for more information about calibration interpolation
  - Write OTP calibration values within the SPI registers: The user is asked to select which OTP 0 values need to be written within SPI (OTP Temperature Low or OTP Temperature High)
- The "Do Interpolation" procedure can be launched at any time in clicking on "Do interpolation" button

Figure 4-18. SPI values selection pop-up window

OTP 🔻	🚱 Hardware Reset	Do Interpolation
SPI OTP	Refresh	SYNC



SPI values selection	SPI values selection
Do you want to :	Do you want to :
Write OTP values in SPI in interpolating interleaving calibrations     to the temperature specified below	<ul> <li>Write OTP values in SPI in interpolating interleaving calibrations to the temperature specified below</li> </ul>
Device Temperature :	Device Temperature :
Vdiode: 830 mV → Tj diode: 52°C →	Vdiode : 830 mV 📩 Tj diode : 52°C 🗼
Write OTP values in SPI	Write OTP values in SPI
Temperature High 💌	Temperature High 💌
OK Cancel	Temperature High Temperature Low OK Cancel

Note: When SPI mode is selected, R\_IN and CM\_IN values (defined in the Settings tab) are the values from SPI (no more OTP values).

- R\_IN and CM\_IN have their SPI default values after a hardware or software reset
- R\_IN and CM\_IN have their previous SPI values if no reset has been done (for instance, if R\_IN is modified to value 12, switching to OTP mode will cause the R\_IN value to switch to the value defined in OTP. When coming back to SPI mode, R\_IN value will come back at the value 12 even if the SPI default value is 8).

### 4.4.3 System Menu description

Figure 4-19.	User Interface System Me	nu
--------------	--------------------------	----

System					
	Start	Stop	Snap	Software Trig	Do Training

The System Menu enables:

- ADC synchronization with FPGA. Pressing the "**Do Training**" button launches the procedure described in chapter 6.4.
- Start: enables to start a continuous acquisition of ADC data output by the FPGA until "Stop" button is pressed.
- Stop: Stop an acquisition when a continuous acquisition has been launched via the "Start" button.
- **Snap:** Press this button to start a single acquisition.
- Software Trig: Press this button to start a single acquisition when GUI is in trigger mode.

The LED on the left side of the System Menu interface switches to red color when FPGA is currently doing an acquisition. When acquisition is finished, LED switches to green color.



# 4.4.4 Status Menu description

#### Figure 4-20. User Interface Status Menu

ChipID:6.3.4 FPGA:1:3.2 FW:1.0.9 CRC 🍚 Sync 🍚 OTP 🍚 System : 🗨 😜 🔬

The Status Menu provides information about:

- Chip ID: identification of the chip revision: must be 6.3.4 for P/N EV12AS350BTPY
- FPGA version code
- Firmware version code
- **CRC status:** After each power-up, the value of ADC MASTER\_STATUS register is read in order to verify that all OTP CRC are successful. The LED is green if all CRC are successful, red otherwise.
- **SYNC status:** The LED is green if the ADC synchronization is successful. Otherwise, the LED is red.
- **OTP status:** After each power-up, the value of ADC MASTER\_STATUS register is read in order to verify that OTP\_STATUS is ready and available. The LED is green if OTP is ready and available, red if not ready.
- System status:
  - The first LED is green if the PLL within FPGA are OK. In case of issue with PLL, LED is red.
  - The second LED is green if the FPGA is correctly synchronized to the ADC. The LED is red if FPGA is not synchronized to FPGA.

	ChipID:	6.3.4 FPGA:1:3.2 FW:1.0	0.9 CRC 🍚 Sync 🍚 OT	"P 🔵 System : 🔵 🔴 🔡
In that case pres	s "Do Training" but	ton in the Header I	Menu.	
Start	Stop	Snap	Software Trig	Do Training



# 4.4.5 Navigation tabs description

Refer to chap 4.5 below.

There are the following tabs:

- Settings: to configure ADC settings (clock mode, clock division, Standby, Swing Adjust, Analog input common mode and impedance)
- Test: to activate ADC test modes (Ramp, Flash and PRBS)
- LUT: to apply a Look-Up Table
- Interleaving calibrations: if the user wants to define its own interleaving calibrations (in SPI mode only)
- Acquisition: to configure the acquisition of ADC output data (4 cores interleaved or aligned with/without averaging, FFT configuration)
- Export: to export acquisition data into a file
- **Debug:** to write or read ADC internal registers via its address (advanced mode for debug purpose)



# 4.5 Operating modes

# 4.5.1 Settings

This tab is dedicated to the configuration of EV12AS350 ADC.



EV12AS350x-EB GUI le ?				
Teledyne e2v EV12AS350x	-EB GUI	OTP   Temperature Low	Hardware Reset	Do Interpolation
System Start	Stop	Snap	Software Trig	Do Training
Setting Test LUT Interleave	ng Calibrations Acquisition	n Export Debug		
CLOCK mode :	Software Re	eset		
No Interleaving (Aligned clock)	CLOCK division :			
Interleaving	No Divided			
Standby :	Divided by 2			
No Standby	Settings :			
Full Standby	Reset Length 8			
Swing Adjust	Analog Input :			
Oisabled	CM IN 15			
Enabled				
	Write	Pond		
	write	Redu		



#### 4.5.1.1. Software reset

Pressing the "Software Reset" button set all ADC registers to their default values.

#### 4.5.1.2. CLOCK mode

Two modes are possible:

- No interleaving (Aligned clock): Data ready of the ADC cores are aligned.
- Interleaving: Data Ready of the ADC cores are delayed by T/4.

This setting corresponds to the ADC register CLK\_MODE\_SEL bit 0.

Pop-up window of Figure 4-22 below appears in case of selection of the 3 unauthorized configurations listed below:

- CLOCK mode = "No interleaving" with "4 Cores Interleaved" selection within Acquisition tab.
- CLOCK mode = "Interleaving" with "4 Cores aligned without averaging" selection within Acquisition tab.
- CLOCK mode = "Interleaving" with "4 Cores aligned with averaging" selection within Acquisition tab.

#### Figure 4-22. Pop-up window in case of Clock mode incompatibility

•	😁 Warni	ing	٢
		Acquisition not possible due to 'CLOCK mode' (Setting tab) and 'Acquisition mode' (Acquisition tab) configuration	
		ОК	כ

#### 4.5.1.3. Standby

Two modes are possible:

- No Standby : This is the default mode
- Full Standby : Power down mode (for each channel)

This setting corresponds to the ADC register STDBY

#### 4.5.1.4. CLOCK division

Two modes are possible:

- **No divided**: This is the default mode. Each core of EV12AS350 ADC operates at F/4, F being the frequency of clock applied to the EV12AS350 ADC.
- **Divided by 2:** each core of EV12AS350 operates at F/8, F being the frequency of clock applied to the EV12AS350 ADC.

This setting corresponds to the ADC register CLK\_MODE\_SEL bit 1.

#### 4.5.1.5. Reset length

This function enables to modify the delay of restart of Data Ready after a SYNC.

Reset length is expressed in terms of number of internal clock cycles. GUI value is expressed in decimal.

- Default value is 8.
- Minimum value is 8 internal clock cycles
- Maximum value is 63 internal clock cycles

This setting corresponds to the ADC register RST\_LENGTH.



#### 4.5.1.6. Swing Adjust

Two modes are possible:

- **Disabled**: data output swing is not reduced (LVDS output data).
- Enabled: this is the default mode of the GUI. Data output swing is reduced

This setting corresponds to the ADC register FULL\_SWING\_EN.

#### 4.5.1.7. Analog Input

It is possible to modify analog input common mode (**CM\_IN**) and analog input impedance (**R\_IN**) if SPI is selected in the Header Menu (these settings are not accessible in OTP mode). These 2 settings correspond to ADC registers R\_IN and CM\_IN.

Note: If R\_IN or CM\_IN values are modified (necessarily in SPI mode), and if the user comes back to OTP mode, R\_IN and CM\_IN will come back to OTP values. Then, if the user switches again to SPI mode, R\_IN and CM\_IN will recover the previous values when ADC was in SPI mode.

### 4.5.2 Test

This tab is dedicated to the configuration of EV12AS350 ADC test modes (Flash, Ramp and PRBS).

Figure 4-23. User Interface Test tab

EV12AS350x-EB GUI					
Teledyne EV12AS350x-EB G e2v	IUI	OTP Temperatur	▼ eLow ▼	Hardware Reset	Do Interpolation
System Start	Stop	Snap	]	Software Trig	Do Training
Setting Test LUT Interleaving Calibr	ations Acquisition	Export	Debug		-
Ramp	PRBS Only				
	ChipID:6.3.4 FF	PGA:1:3.2 FV	V:1.0.9 CF	RC 曼 Sync 🍚 OTP	🔵 System : 🌚 🚭

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#### 4.5.2.1. Test

Two modes are possible:

- **Disabled:** this is the default mode. Test mode is not active. ADC is in normal mode.
- Enabled: test mode is activated. Ramp and Flash are accessible.

This setting corresponds to the ADC register TEST MODE.

When Test is "Enabled", before selecting Flash or Ramp mode, SYNC button (Header Menu) needs to be pressed. Then Flash or Ramp mode can be selected.

Flash mode can be selected and the flash length can be adjusted from 2 to 60 internal clock cycles (GUI values are displayed in decimal). This setting corresponds to the ADC register FLASH LENGTH. Default value is 24 internal clock cycles.

When Test is enabled, Ramp mode can be selected and a ramp is generated at the output of each ADC core.

Note: A "Do training procedure" followed by a "SYNC" is mandatory after selecting Ramp or Flash mode in order to re-synchronize EV12AS350 ADC with FPGA.

#### 4.5.2.2. PRBS

A Pseudo Random Bit Sequence (PRBS) can be added on ADC output (encoding within ADC).

Note: It is not necessary to have TEST "Enabled" to activate PRS mode.

- By default there is no PRBS encoding within ADC: "None" selection
- It is possible to consider a PRBS encoding on ADC output data: "PRBS+Data" selection. In that case, the PRBS decoding is done within FPGA.
- A PRBS sequence can be selected as a test mode: "PRBS Only" selection. This mode is not . supported by the Evaluation Board (no acquisition in this mode). As a consequence, a pop-up window appears as shown on figure 4-24.

Figure 4-24. Pop-up window "Acquisition not possible in 'PRBS Only' mode"

Warr	ing X
	Acquisition not possible in 'PRBS Only' mode
	ОК



# 4.5.3 LUT

This tab enables to apply a Look Up Table (LUT) to the ADC. A LUT can be used to correct the static non-linearity of the ADC.

The principle of LUT file is described below.

When doing an acquisition of code N, this code is modified by the value of the LUT for code N (LUT value for code N is subtracted to code N).

For instance, if the LUT value for code 3208 is 1.536 LSB, when doing the acquisition of code 3208, the value to be considered will be 3208-1.536 = 3206.464 which will be truncated to 3206 (12 bit).



SPI Temperatur Snap Acquisition Export UI\INLs	▼ ∳ H re Low ▼ Debug	Hardware Reset) Refresh ware Trig	Do Interpolation SYNC Do Training Do Training Refresh Send From File From File
SPI Temperatur Snap Acquisition Export UI\INLS	Elow     Softw     Debug	Hardware Reset	Do Interpolation SYNC Do Training Refresh Send From File From Clipboard
Acquisition Export	Debug	ware Trig	Do Training Refresh Send From File From Clipboard
Acquisition Export	Debug		Refresh Send From File From Clipboard
UI\Inls			Refresh Send From File From Clipboard
			Refresh         Send         From File         From Clipboard
			From File From Clipboard
			Reset
hipID:6.3.4 FPGA:1:3.2 FV	W:1.0.9 CRC 🔵	Sync 🍚 OTP (	🔵 System : 🍚 🔵
	10.015	Segurate a	
	1ipID:6.3.4 FPGA:1:3.2 F	1ipID:6.3.4 FPGA:1:3.2 FW:1.0.9 CRC	iipID:6.3.4 FPGA:1:3.2 FW:1.0.9 CRC 🝚 Sync 🍚 OTP



#### 4.5.3.1. LUT file format

A LUT file can be created by saving ADC INL characteristics in a file that will be used as a correction table. See chapter 4.5.6 to see how to export acquisition data.

Note: ADC INL files are exported in Excel format. In order to be used as a LUT file, it needs to be saved as a text file as shown on figure 4-26. Be careful, the order of ADC cores is A, B, C, D in the exported INL file and needs to be A, C, B, D in the LUT file!

LUT files are text files (file.txt) and their format change if 4 ADC Cores are aligned or interleaved

#### *Figure 4-26.* LUT file format

<ul> <li>a) 4 ADC cores interleaved</li> </ul>	b) 4 ADC cores aligned
INI Intelevent to Place actor	
INC Intereaved.txt - Bioc-notes	Fichier Accueil Insertion Mise en page INL 4 cores aligned.txt - Bloc
Eichier Edition Format Affich	Calibri <u>11</u> A <u>Fichier Edition Fo</u> rmat <u>Affichage ?</u>
0	
ŏ	$\frac{1}{1229} + \frac{1}{5} + \frac$
0	
ő	
0	209 Channel A 0 <u>-2.15</u> 0
0	211 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
-1.657	212 0 213 0 Channel C -1.395 0
-1.888	
-1.665	215 -1,395 -2.521 0 -1.272 -1.173 -2.17 216 1 4 1 91 -1.345 -1.306 -2.181 Channel D
-1.931	217 -1.272 -1. 73 - Channel B -1. 316 -1.556 -2.47
-1.922 -2.235	-1.858 -2.043 -2.866 -2.763
-2.03	
-2.159	221 -1.771 -1.732 -1.65 Channel D 182 -2.063 -2.312 -2.98
-2.032	
-2.091	224 -1.625 -1.463 -1.969 -3. 68 -1.476 -1.914 -1.904 -2.765
-2.082	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
-2.227	227 -1.69 -1.831 -2.01 -2.01 -2.01 -1.31 -1.756 -2.035 -2.322
-1.859	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
-1.938	
-2.054	231 -1.61 -1.822 -2.057 -2.586 -1.686 -2.245 -2.548 -2.36
-2.1 -1.877	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
-2.1	234 -1.473 -2.214 -2.452 -1.843 -1.128 -1.432 -2.635 -1.933
-1.864 -1.813	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
-1.585	
-1.482	
-1.574	$\begin{array}{c} -0.784 & -1.362 & -2.248 & -0.875 \\ \hline 240 & -0.455 & -1.66 & -2.549 & -0.401 \\ \hline & -1.326 & -1.372 & -2.262 & -0.841 \\ \end{array}$
-1.562	241 -0.784 -1.362 -2.248 -0.875 -1.417 -1.411 -2.31 -1.409
-1.693	242 -1.320 -1.372 -2.202 -0.841 243 -1.417 -1.411 -2.31 -1.409
-1.814	244 -2.079 -1.244 -2.008 -1.015
	245 -2.167 -1.571 -1.938 -1.666
	Prêt 🖀

If 4 ADC cores are interleaved, the LUT file contains only one column corresponding to the INL characteristics of the 4 ADC cores interleaved.

If 4 ADC cores are aligned, the LUT file contains 4 columns : each column corresponds to the INL characteristics of an ADC Core :

- 1st column is the LUT for ADC Core A
- 2<sup>nd</sup> column is the LUT for ADC Core C
- 3<sup>rd</sup> column is the LUT for ADC Core B
- 4<sup>th</sup> column is the LUT for ADC Core D

The values in each column are written in decimal and correspond to the correction to be applied on each acquisition.

Each LUT file needs to contains 4096 lines. If the LUT does not include 4096 lines, the following error message is displayed:



#### Figure 4-27. LUT error message



It is possible to select the directory where LUT files are available by clicking on the button <sup>[....]</sup> on the right side of the field "Directory and INL files"

Button "Refresh" enables to refresh the display of all available LUT files (file.txt) in the selected directory.

Refresh

Note: The refresh is done automatically when a file is written within the selected folder.

#### 4.5.3.2. LUT file selection

The LUT can be dowloaded from a file or from clipboard:

#### a) LUT selection from a file

- Select the directory in which the desired LUT file is saved by clicking on the button used on the right side of the field "Directory and INL files"
- Select the desired LUT file

Whatever the method used to select the LUT file is, the GUI will be executed differently depending on the format of the LUT file:

- If the LUT file contains 4 columns, it directly downloads the LUT into the FPGA. Each column will be applied to the associated ADC Core (case where 4 ADC cores are aligned). A message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA.
   Send INL Done The "Send INL Done" message disappears after a few seconds.
- 2. If the LUT contains 1 column, the pop-up window of figure 4-28 appears and asks the user on which channel the LUT has to be applied (case where 4 ADC cores are interleaved).





*Figure 4-28* LUT channel selection

Found 1 suitable LU Please, select chan	л. nel(s) on which apply it.
Channel A	📝 Channel B
🔽 Channel C	Channel D
<ul> <li>Select/Unselect</li> </ul>	All

Select all channels if 4 ADC cores are interleaved.

Then a message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. Send INL Done

The "Send INL Done" message disappears after a few seconds.

Note: This selection can also be done by clicking on the "**From File**" button: From File" button: Clicking on the "**From File**" button opens an explorer window to select your directory and your LUT file as shown on figure 4-29 below.

Once the LUT file is selected it is directly sent to the FPGA (No need to click on "Send" Button).

Figure 4-29.	LUT explorer window
--------------	---------------------

Organiser   Inclure dans la bil	bliothèque 🔻 Graver Nouveau dossier
🚖 Favoris	LUT.txt
📃 Bureau	LUT.xlsx
🔛 Emplacements récents	EV12AS350x-EB_GUI

#### b) LUT selection From Clipboard

A LUT can be downloaded from clipboard with the following procedure:

- Open the file including the LUT to be applied
- Select the LUT considered column(s)
- Copy the LUT considered column(s)
- Then click on the "From Clipboard" button
   From Clipboard
- The data previously copied has been downloaded in GUI.

Whatever the method used to select the LUT file is, clicking on the "Send" button has the following effect:

1. If the LUT file contains 4 columns, it directly downloads the LUT into the FPGA. Each column will be applied to each ADC Core (case where 4 ADC cores are aligned).

A message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. Send INL Done

**TELEDYNE C2V** 

The "**Send INL Done**" seconds. 4-28

message disappears after a few

Everywhereyoulook EV12AS350BTP-EB Evaluation Board

2. If the LUT contains 1 column, the pop-up window of figure 4-30 appears to ask the user on which channel the LUT has to be applied (case where 4 ADC cores are interleaved).

*Figure 4-30.* LUT channel selection

Found 1 suitable LU Please, select chanr	rr. nel(s) on which apply it.
Channel A	📝 Channel B
🔽 Channel C	Channel D
Select/Unselect	All

Select all channels if 4 ADC cores are interleaved.

Then a message on the left bottom size of the window indicates that the LUT has been correctly downloaded within FPGA. Send INL Done

The "Send INL Done" message disappears after a few seconds.

#### 4.5.3.3. Enabling LUT corrections

Click on "Lookup Table is Disabled" button in order to get the display "Lookup Table is Enabled"

LookupTable is Disabled	$\Rightarrow$	LookupTable is Enabled
----------------------------	---------------	---------------------------

The next acquisitions will now apply LUT corrections until LUT is disabled.

#### 4.5.3.4. Stopping LUT corrections

There are two ways of stopping LUT corrections:

- 1. By clicking on "Lookup Table is Enabled" button
  - LUT corrections can be stopped when clicking on the "Lookup Table is Enabled" button which then displays the text "Lookup Table is Disabled"



This action is stopping the LUT corrections, but LUT correction values are still loaded within FPGA. This means that LUT can be reapplied by a simple click on "**Lookup Table is Disabled**" button.

#### 2. By clicking on "Reset" button

LUT corrections can be stopped in clicking on the "**Reset**" button. This action erases LUT values from FPGA.



After clicking on "**Reset**" button, the pop-up window of figure 4-31 is displayed. Click "**Yes**" to confirm your choice.

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*Figure 4-31* Stopping LUT table.



4.5.3.5. Example of LUT effects on INL with 4 ADC cores interleaved











### 4.5.4 Interleaving calibrations

This tab enables to modify ADC default interleaving calibrations (written within OTP) in order to get an optimum calibration for the considered clock rate and Fin. It is however recommended to use OTP calibrations.

- Interleaving Offset: "Offset" menu corresponds to ADC registers x\_OFFSET\_CAL (x=A, B, C & D)
- Interleaving Gain: "Gain" menu corresponds to ADC registers x\_Gain\_CAL (x=A, B, C & D)
- Interleaving Phase: "Phase" menu corresponds to ADC registers x\_Phase\_CAL (x=A, B, C & D)

This tab is accessible in the only case when SPI is selected in the Header Menu.

The "Calib" Menu displays the calibration value (Offset, Gain and Phase) for each ADC core (A, B, C and D) Values are displayed in decimal.

e2v	<sup>le</sup> EV12A	S350x-EB GUI		Temperat.	Jre Low 🔻	Hard	ware Reset	Do Interpol	lation
/stem	Start	Stop		Snap		Software	Trig	Do Train	ning
etting	Test LUT	Interleaving Calibrations	Acquisition	Export	Debug				
Offset :				Gain :					
	lsb				lsb				
Write	A 255 ≑			Write A	511	-			- 1
Write	B 255 🜩			Write B	511				_
Write	255 🖨			Write C	511	<b>.</b>	0		
Write	255 🜩			Write D	511	÷	0		_
Phase :				Calib :					
	lsb			Name	A	В	С	D	
Write	A 127 🖨	·		Offset	211	229	313	262	
Write	B 127 🌲			Gain Phase	394 150	440	346	687 100	
Write	C 127 ≑			, nose	100		100	100	
Write	127 🚔	Q							
				•		ш			•
								Read	

Figure 4-34. Interleaving Calibrations tab

Clicking on the "**Read**" button in the Calib Menu refresh the display in reading SPI registers x\_OFFSET\_CAL (x=A, B, C & D), x\_GAIN\_CAL (x=A, B, C & D) and x\_PHASE\_CAL (x=A, B, C & D) Notes:

- Possible values for Offset adjustment is 0 to 511
- Possible values for Gain adjustment is 0 to 1023
- Possible values for Phase adjustment is 0 to 255

It is possible to modify interleaving calibrations in writing for each ADC core the value to be written (either with the cursor or with the arrow or in writing directly the value). After modifying a value, click on the associated "Write x" button.

It is possible to verify that the modification is well taken into consideration in checking values from the "Calib" Menu after having clicked on the "**Read**" button.

Note: If a "Do interpolation" is launched; all modifications done on Interleaving Calibrations are lost.

It is possible to save ADC calibrations and settings in a context file (file.ctx) that can be reloaded. Refer to chapter 4.4.1 for explanation about context files.



# 4.5.5 Acquisition

This tab enables to configure the acquisition.

4.5.5.1. Acquisition mode Menu

Figure 4-35. Acquisition tab – Acquisition mode Menu

Acquisition mode		
4 Cores Interleaved	4 Cores aligned without averaging	$\bigcirc~$ 4 Cores aligned with averaging (calculed within GUI)

3 acquisitions modes are possible :

- 4 Cores interleaved. This option is possible in the only case when CLOCK mode is configured in "Interleaving" mode within the Settings tab. If it is not the case, pop-up window of Figure 4-36 is displayed.
- 4 Cores aligned without averaging. This option is possible in the only case when CLOCK mode is configured in "No Interleaving" mode within the Settings tab. If it is not the case, pop-up window of Figure 4-36 is displayed.
- 4 cores aligned with averaging (calculated within GUI). This option is possible in the only case • when CLOCK mode is configured in "No Interleaving" mode within the Settings tab. If it is not the case, pop-up window of Figure 4-36 is displayed.

Figure 4-36. Pop-up window in case of Clock mode incompatibility

1000	- Warni	ing
		Acquisition not possible due to 'CLOCK mode' (Setting tab) and 'Acquisition mode' (Acquisition tab) configuration
		ОК

#### 4.5.5.2. Data Menu

Figure 4-37. Acquisition tab – Data Menu

Data	
Resolution in bit	12
Sampling Nbr	2^18:262144 💌
Payload Size (Bytes)	524288

In this Menu the user indicates the number of bit to be acquired (acquisition on 12-bit) and the number of ADC samples to be acquired. Possible numbers of samples are:

- $2^{18}$  points = 262 144 samples  $2^{17}$  points = 131 072 samples
- $2^{16}$  points = 65 536 samples



Number of samples displayed corresponds to the total number of samples if 4 ADC cores are interleaved. If 4 Cores are aligned the number of samples per core is 4 times lower than the number displayed in the Sample Nbr field.

Payload size (Bytes) represents the memory size to be allocated on the PC to get the sampled data (each sample is coded on 2 Bytes for USB transfer)

#### 4.5.5.3. Clock Menu

*Figure 4-38.* Acquisition tab –Clock Menu

Clocks		Mode :
External Clock (MHz)	5400.00000000 🚔	Freerun
First Analog Input Frequency (MHz)	1900.00000000 🚔	Trigger
Second Analog Input Frequency (MHz)	819.99893188 🗼	Coherent Sampling
Clocks		Mode :
Clocks External Clock (MHz)	5400.0000000	Mode :
Clocks External Clock (MHz) First Analog Input Frequency (MHz)	5400.00000000 1900.02365112 🜩	Mode : Freerun Trigger

This Menu enables to indicate the considered **External Clock** frequency (in MHz) so that the GUI can calculate ADC output spectrum and identify the different spurs (harmonics, interleaving spurs, intermodulation spurs, clock related spurs ...)

**First Analog Input Frequency (MHz)**: In this field the user is asked to complete the first analog input frequency. it is not necessary to fill this field if a single tone is selected in the Processing Menu. Indeed, the GUI uses the highest spur of the ADC output spectrum to detect the fundamental.

Second Analog Input Frequency (MHz): This field is mandatory in the only case when Dual tone is selected. The user is asked to complete the second analog input frequency in this field.

If **Coherent Sampling** option is selected, it automatically slightly modifies the First Analog Input Frequency and the Second Analog Input frequency (if applicable) in order to get a coherent sampling (function of external clock and number of samples).

#### 4.5.5.4. Mode Menu

*Figure 4-39* Acquisition tab – Mode Menu

Mode :	٦.
Freerun	
Trigger	
L	J.

This Menu is used to select between **Freerun** and **Trigger** Acquisition.

• **Freerun** is the mode by default. Acquisition is launched when the "**Snap**" button from the System Menu is pressed. A single acquisition is done.

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- Trigger can be selected in order to launch the acquisition on an event (hardware of soft event).
  - o Soft event:

It is necessary to first press "Snap" button and then "Software Trig" button in the System Menu.

If the user is waiting too much time to launch an acquisition, an error window is displayed as shown on Figure 4-40.

Figure 4-40. Error window if no trigger occurs

1.1	White I do it is
<u> </u>	wait for buffer timeout
<u> </u>	
	OK

Hard event:

It is necessary to first press the "**Snap**" button and then an acquisition is launched when an event (pulse) occurs on signal SPARE SYNC\_FPGA\_P / SPARE SYNC\_FPGA\_N.

#### 4.5.5.5. Processing Menu

*Figure 4-41.* Acquisition tab – Processing Menu

Processing				
FFT Tone	Single	<ul> <li>IMD Order</li> </ul>	5	•
FFT Window	None	<ul> <li>Nb Harmonics</li> </ul>	25	•
FFT unit	dB	<ul> <li>Peak width</li> </ul>	11	×

This Menu enables to configure the FFT calculation :

• **FFT Tone**: this field enables to choose between a **Single** Tone or a **Dual** Tone acquisition.

Processing	
FFT Tone	Single 🔻
	Single
	Dual

Note: In dual tone, the number of harmonics is limited to 20.

 FFT Window: this field is used to apply a FFT windowing option if the sampling is not coherent. A "7-Term Blackmann-Harris" window option is proposed. By default no windowing is applied (case of coherent sampling) → "None"option.

Processing	
FFT Tone	Single 💌
FFT Window	None 🔻
FFT unit	None 7 Term B-Harris



• **FFT Unit**: this field is used to select the FFT unit. By default unit is "**dB**". "**dBc**" option is also possible. Selecting this option implies that the fundamental is set at 0 dBc.

Processing	
FFT Tone	Single 💌
FFT Window	None 💌
FFT unit	dB 🔹
	dBc
Display Graph	dB

IMD Order: this field is used in the only case when a Dual Tone is selected in the FFT Tone field. It indicates how many intermodulations will be displayed in the "FFT Parameters" window. See display Graph Menu.

F1         F2           F1         F2           F1         1F1+1F2           1F1+1F2         1F1+2F2           1F1-1F2         1F1+2F2           11F1-1F2         1F1-2F2	F1         F2           F1         F2           1F1+1F2         1F1+1F2           1F1+1F2         1F1+2F2           11F1-1F2         1F1+2F2           2F1+1F2         2F1+1F2
F1         F2           F2         1F1+1F2           1F1+1F2         1F1+2F2           1F1-1F2         1F1-2F2           1F1-2F2         1F1-2F2	F1         F2           F2         1F1+1F2           1F1+1F2         1F1+2F2           1F1-1F2         1F1-2F2           2F1+1F2         2F1+1F2
F1     1F1+1F2       F2     1F1+1F2       1F1+1F2     1F1+2F2       1F1-1F2     1F1+2F2       1F1-1F2     1F1-2F2	F1     1F1+1F2       F2     1F1+1F2       1F1+1F2     1F1+2F2       1F1+1F2     1F1+2F2       1F1-1F2      2F1+1F2       2F1+1F2     2F1+1F2
F2     [1F1-1F2]       1F1+1F2     1F1+2F2       [1F1-1F2]     1F1-2F2	F2      1F1-1F2        1F1+1F2      1F1-2F2         1F1-1F2       1F1-2F2        2F1+1F2      2F1+1F2
1F1+1F2 1F1-1F2 1F1-2F2 1F1-2F2 1F1-2F2 1F1-2F2	1F1+1F2     1F1+2F2       11F1-1F2     1F1-2F2       2F1+1F2     2F1+1F2
1F1-1F2     1F1-2F2     1F1-2F2	[1F1-1F2]         [1F1-2F2]           2F1+1F2         2F1+2F2
	2F1+1F2

Nb Harmonics: this field is used to indicate how many harmonics will be displayed in the "FFT Parameters" window. It is also used to indicate how many harmonics will be considered in the THD (H2 to Hn) and in the SNR (Hn and higher ranks). By default 25 first harmonics are considered in THD and higher rank harmonics are considered as SNR.

Note : In dual tone, the number of harmonics is limited to 20.

• **Peak width:** this field is used to configure the detection of the highest spur (for SFDR calculation). Indeed, in case of phase noise on fundamental or DC component, some points need to be excluded when looking for the highest spurs. Peak width default value is 11: it means that when looking for the highest spurs, the 5 points around the fundamental plus the point of the fundamental are excluded .On the same way, the 5 points above the DC component are excluded.

It is recommended to keep Peak width value at 11. This value can be increased if SFDR is detected in the cone of the fundamental or DC components.

A peak width value of 1 means that only the highest spur of DC component and highest spur of fundamental are excluded.

Only odd values are possible for peak width.

The peak width effect is illustrated in figure 4-42 and 4-43 below.





FFT		FFT	parameters	product and the Case	-8			
Plots		0	[CHA, CH	C, CHB, CHD]			THD (dB)	THD (dBFS)
				Frequency (MHz)	dB	TAT	-54.06	-55.08
0.0-			H0	0.00000000	3.01		TILD (dB)	TILD (dBFS)
			H1	1899.98245239	-1.02		-60.62	-61.64
-20.0 -			H2	1600.03509521	-64.34		TIMD (dP)	TIMD(apps)
			H3	299.94735718	-55.85			TIMD(GDF3)
40.0			H4	2199.92980957	-83.49		NaN	INaN
-40.0-			H5	1300.08773804	-85.42		TD (dB)	TD (dBFS)
			H6	599.89471436	-115.42		-53.20	-54.21
-60.0 - 8	$\mathbf{H}$		H7	2499.87716675	-82.77		SNR (dB)	SNR (dBFS)
			H8	1000.14038086	-92.91		50.08	51.10
80.0-			H9	899.84207153	-77.89	-	100.00	101.10
-00.0			H10	2600.17547607	-97.50		SINAD (dB)	SINAD (dBFS)
			H11	700.19302368	-86.78		48.36	49.37
100.0	er der Mendenbergen ber an der eine Bernen auf von eine der eine Bernen an der Bernen der Bernen der Bernen eine		H12	1199./89428/1	-105.26	-	ENOB	ENOB_FS
	and the second		HIS	2300.22811890	-82.34	-	7.74	7.91
120 0 - duil	ուների համի հարցերի կանված հանձիր, վեծ իրավիկեր, ավելանին 🖼 անհին, համինի է հեղ անհենի է երկների է հայտնակիր եղել անդեմի		HI4	400.2456650	-95.29	-	SEDR Frequency (	
12010	المترج المتكار المتكافية المتحادية والمتحادية المتحاد المتحاد والمتحاد والمتحاد المتحادية المتحاد المتحاد المتح		HLS	1499.75076569	-/0.90	-	and outparties	
			117	100 20020022	-04.07	-	299.94755710	
140.0-			H18	1700.29030933	-96.12	-	SFDR (dBc)	SFDR (dBFS)
			H19	1700 33340454	-74 25	-	-54.83	-55.85
160.0 -			H20	199 64904785	-03.20	-	SFSR (dB)	-
1800.0	1820 0 1840 0 1860 0 1880 0 1900 0 1920 0 1940 0 1960 0 1980 0 2000 0		H21	2099.63150024	-77.78	-	-1.02	Overlap
1000.0			H22	1400.38604736	-87.38	-		
111-			H23	499,59640503	-81.85	-	Floorivoise(dBF5/	HZ)
VII 12	□ Cursor 31.4 -106.1		H24	2399.57885742	-96.07		-145.41	
			H25	1100.43869019	-83.88		IMD3 (dBc)	IMD3 (dBFS)
JB						101	NaN	NaN



On above figure, SFDR is fund on the fundamental due to the cone. Peak width needs to be increased.



*Figure 4-43.* Example of acquisition with peak width = 11 (Fclk = 5.4GHz, Fin = 1900MHz)

With Peak width = 11, the points around the fundamental does not interfere in the highest spur identification. SFDR is calculated correctly.



#### 4.5.5.6. FFT Band Menu

#### Figure 4-44. Acquisition tab – FFT Band Menu

FFT Band		
Center (MHz)	100.000	A
Span(MHz)	30.000	×

Figure 4-45.

This menu is accessible by selecting the FFT Band field in the top left corner. It enables to calculate FFT parameters on Narrow band. If this option is not selected, the FFT calculation is done over full Nyquist zone.

- Center (MHz): this field is used to indicate the center of the narrowband to be considered. ٠
- **Span (MHz):** this field is used to indicate the span of the considered band of interest.

Example of FFT band with markers showing the band of interest

This menu is accessible for both Single Tone and Dual Tone acquisition.

Once Center and Span parameters are configured, it is possible to launch an acquisition. Two purple vertical markers are displayed on FFT spectrum to delimit the band of interest on which FFT calculation are done. See Figure 4-45.



Center = 1600MHz & Span=20MHz





#### 4.5.5.7. Display Graph Menu

Figure 4-46. Acquisition tab – Display Graph Menu



This Menu enables the user to select which graphs need to be displayed after data acquisition.

- Show FFT parameters: selecting this graph will display FFT parameters (ENOB, SFDR, ...) as shown on the example of Figure 4-47. See Section 5 for parameters definition and FFT formula calculations.
- **Show Sampled Signal:** selecting this graph will display the sampled data as shown on the example of Figure 4-48.
- Show FFT Spectrum: selecting this graph will display the ADC FFT spectrum with spurs identification as shown on the example of Figure 4-49 and Figure 4-50.
- Show INL: selecting this graph will display the ADC INL curve as shown on the example of Figure 4-51.

[CHA]			THD (dB)	THD (dBFS)
<u> </u>	Frequency (MHz)	dB	-53.76	-54.77
HO	0.00000000	3.01	TILD (dB)	TILD (dBES)
HI	549,98245239	-1.01	N-N	N-N
H2	250.03509521	-64.49	INdiv	INdia
H3	299,94735718	-55.81	TIMD (dB)	TIMD(dBFS)
H4	500.07019043	-79.83	NaN	NaN
H5	49.91226196	-85.05	TD (dB)	TD (dBFS)
H6	599.89471436	-82.48	-53.76	-54.77
H7	200.12283325	-82.30	( ) ) ) ( ) ( ) ( ) ( ) ( ) ( ) ( ) ( )	0.00
H8	349.85961914	-91.88	SNR (dB)	SNR (dBFS)
H9	450.15792847	-72.62	50.07	51.08
H10	99.82452393	-88.14	SINAD (dB)	SINAD (dBFS)
H11	649.80697632	-78.18	48.52	49.54
H12	150.21057129	-85.65	ENIOR	ENIOR ES
H13	399.77188110	-98.78	1 77	204
H14	400.24566650	-88.25	1.11	1.94
H15	149.73678589	-75.09	SFDR Frequency	y (MHz)
H16	650.28076172	-76.97	299.94735718	
H17	100.29830933	-101.69	SEDR (dBc)	SEDR (dBES)
H18	449.68414307	-88.83	-54.80	-55.91
H19	350.33340454	-70.91	J-54,00	
H20	199.64904785	-78.43	SFSR (dB)	
H21	600.36849976	-72.44	-1.01	Overlag
H22	50.38604736	-87.56	FloorNoise(dBF	S/Hz)
H23	499.59640503	-75.46	-139.37	
H24	300.42114258	-82.14	1255.57	
H25	249.56130981	-80.15	IMD3 (dBc)	IMD3 (dBFS)

#### Figure 4-47 Examples of FFT Parameters window

a) FFT parameter window for ADC core A

b) FFT parameter window for 4 ADC cores

CHA, CH	IC, CHB, CHD]		THD (dB)	THD (dBFS)
	Frequency (MHz)	dB	-54.27	-55.29
HO	0.00000000	3.01	TILD (dB)	TILD (dBFS)
H1	1899.98245239	-1.02	-60.94	-61.96
H2	1600.03509521	-64.36	100.54	-01.50
H3	299.94735718	-56.07	TIMD (dB)	TIMD(dBFS)
H4	2199.92980957	-84.92	NaN	NaN
H5	1300.08773804	-85.53	TD (dB)	TD (dBFS)
H6	599.89471436	-108.65	-53.42	-54.44
H7	2499.87716675	-83.16	CNID (HD)	
H8	1000.14038086	-93.32	SINK (db)	SINK (GDFS)
H9	899.84207153	-78.75	50.11	51.13
H10	2600.17547607	-99.93	SINAD (dB)	SINAD (dBFS)
H11	700.19302368	-87.13	48.45	49.46
H12	1199.78942871	-102.49	ENOR	ENOR ES
H13	2300.22811890	-81.69	7.76	7.02
H14	400.24566650	-91.69	1.70	1.92
H15	1499.73678589	-77.77	SFDR Frequency	(MHz)
H16	2000.28076172	-84.64	299.94735718	
H17	100.29830933	-85.12	SEDR (dBc)	SEDR (dBES)
H18	1799.68414307	-86.48	-55.05	-56.07
H19	1700.33340454	-74.84	1-55.05	1-50.07
H20	199.64904785	-90.34	SFSR (dB)	
H21	2099.63150024	-77.76	-1.02	Overla
H22	1400.38604736	-86.68	FloorNoise(dBF	S/Hz)
H23	499.59640503	-81.71	-145.44	
H24	2399.57885742	-96.02		
H25	1100.43869019	-84.67	IMD3 (dBc)	IMD3 (dBFS)
		1	NaN	NaN

Notes:

- 1. See Section 5 for definitions of FFT calculations.
- The Overlap LED is green if everything is OK. The Overlap LED is red if some harmonics are superposed (for instance if Fin=Fclk/4) or if analog input RF generator is OFF or if some interleaving spurs are superposed to harmonics. Refer to chapter 5.2 for more information.
- In mode "4 Cores Aligned", it is possible to switch from one core to another thanks to the small arrows located on the top left corner of above window ([CHA] corresponds to ADC Channel A, [CHB] to ADC Channel B, ....)
- With 4 Cores interleaved, the only possible choice is [CHA, CHC, CHB, CHD].





a) Sampled Data for ADC core A, B, C & D interleaved



### Figure 4-49. Examples of FFT Spectrum

- a) FFT Spectrum for ADC core A, B, C & D interleaved
- b) FFT spectrum for 4 ADC cores

b) Sampled Data for 4 ADC cores



Note: In mode "4 Cores Aligned", the 4 FFT spectrum are superposed. For a better readibility it is possible to select which ADC core FFT to be displayed by clicking right on CHA (or CHB or CHC or CHD) as shown on Figure 4-50 below.







### Figure 4-51. Example of INL curve

a) INL for ADC core A, B, C & D

b) INL for 4 ADC cores interleaved





Checks				
	Channel A	Channel B	Channel C	Channel D
Parity Check Failed	0	0	0	0
Overrange	0	0	0	0

This Menu enables to monitor the Parity Bit and Overrange Bit for each ADC Core.

Number of **Parity Check Failed** (among the Sampling Nb) is displayed for each ADC Core. If value is zero, everything is OK.

Number of **Overrange** (among the Sampling Nb) is displayed for each ADC Core. If value is zero everything is OK.



Examples are shown on Figure 4-53 & Figure 4-54

#### Figure 4-53. Checks Menu with saturation



### Figure 4-54. Checks Menu with Over-range

		·			
Overrange	21933	22101	21979	21858	Warning !!
· · · · · · · · · · · · · · · · ·				22000	manning

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# 4.5.6 Export

Figure 4-55. Export tab

e2v EV12AS	350x-EB GUI	Temperature Low	fresh SYNC
/stem	Stop	Snap	Trig Do Training
etting Test LUT	Interleaving Calibrations Acquisiti	on Export Debug	
Excel Data Saving			
File : C: \Users \adminlocal \De	esktop\FFT EV 12AS350B.xlsx	FFT Parameters	INL Coefficients
CAN Test Data Saving			
File :			

This tab is used to export acquisition Data in a File.

#### 4.5.6.1. Data exportation in Excel file

This mode is activated by checking the box in the **Excel Data Saving** Menu as shown on Figure 4-55 above. The procedure to be followed is:

- 1. Indicate the path of the file
- 2. Give a name to the file
- 3. Select the data to be exported in the file (Sampled Signal, FFT Spectrum, FFT parameters and INL coefficients)
- 4. Then click on the "**Snap**" button of the System Menu to launch the acquisition and save the selected data in the Excel File

Notes:

1. If the given file name already exists, the user is asked to confirm he wants to overwrite the existing file as shown on figure below:

#### Figure 4-56. Overwrite window

🐨 Oven	write
?	C:\Users\adminlocal\Desktop\FFT EV12AS350B.xlsx already exists. Overwrite it ?
	OK Cancel



- 2. When the FFT Spectrum is selected, the harmonics are also saved. Each kind of exported data appears in a different sheet of the Excel file as shown on Figure 4-57 to 4-60. Note that FFT Spectrum is saved in two excel tabs:
  - a. FFTModule: for Y axis
  - b. FFTFrequencies: for X axis
- 3. When launching an acquisition in the Freerun mode followed by clicking on the "Start" button from System Menu, only the 1<sup>st</sup> acquisition is saved even if the user performs successive acquisitions.

X | 🖃 🕜 🗆 🗗 🔀 Fichier Accu Fichier () - # X 11 · · A · A · Σ· A Z Calibr = = = =  $\Sigma - \frac{A}{Z}$ = = = = × A ... ĥ Standard Calibri \* 11 Standard A A insérer \* ĥ -G I **- %** 000 💽 - 🐴 -G I § - A A ■ ■ ■ ■ - 9 - % 000 Supprimer 3-Coller 🦪 Style Cellules Coller 🗳 Style Trier et Rechercher et • <u>ð</u> - <u>A</u> i i 🗱 🗞 00,00 ,00 00, 2-∉ # ≫· Format \* 🗄 • 🔕 • 🗛 • €,0 ,00 ,00 €,0 resse-pap Alig Éd fx E12 F14 f, Δ A B C D 1 3671 588 2008 3546 290 2 1781 2 2632 3100 207 3190 744 2519 343 3619 1896 4 3873 678 3859 1279 1169 5 1177 3868 753 1764 3673 6 1263 382 2396 3287 215 7 3853 8 677 9 1873 2991 2754 262 3470 2135 522 3780 1506 9 956 3896 942 1517 10 3772 509 2148 3461 10 3630 11 335 256 2769 2979 220 11 12 2495 13 3203 12 3297 2386 392 3682 13 1754 765 3876 1158 14 202 14 1289 3851 655 1895 15 3086 15 3611 326 2532 3178 16 2654 16 207 3098 2631 300 17 291 17 3550 2007 604 3828 18 3541 18 1374 1070 3884 839 19 2027 19 1655 3729 430 2269 H + + + N SampledSignal \_ INL \_ FFT\_Parameters \_ Harmonics \_ IM \_ FFTModule \_ FFTFrequencies \_ \*3 H + + H SampledSignal / INL / FFT\_Parameters / Harmon 4 100 % Prêt 🞦 回 四 100 %

*Figure 4-57.* Example of exported Excel file – SampledSignal tab (When "Sampled Signal" is selected)

Note: When the acquisition is done in « 4 Cores Interleaved » mode, the Sampled Data is displayed on one column. When the acquisition is done in "4 Cores Aligned" mode, the Sampled Data is displayed on 4 columns:

- Column A for ADC Core A
- Column B for ADC Core C
- Column C for ADC Core B
- Column D for ADC Core D





		(* - &   -	FFT	EV12AS350B.xlsx	- Microsoft E	xcel			(* - 45	a   <del>-</del>	_	-	FFT EV12AS
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207	1.751						207	0	4.344	2.267	0		
208	1.353						208	0	3.812	2.573	0		
209	1.372						209	0	4.324	1.918	0.036		
210	1.59						210	1.187	4.241	2.174	0.014		
211	1.717						211	1.549	4.054	2.282	-0.073		
212	1.744						212	1.717	4.172	2.116	-0.07		
213	1.685						213	1.708	3.793	1.374	0.48		
214	1.926						214	2.209	3.601	1.444	0.655		
215	1.776						215	1.551	3.01	1.663	1.048		
216	1.865						216	1.985	3.028	1.355	1.178		
217	1.762						217	1.907	3.153	1.219	0.843		
218	1.729						218	2.175	2.85	1.021	0.898		
219	1.993						219	2.51	2.61	1.448	1.302		
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### Figure 4-58. Example of exported Excel file – INL tab (When "INL coefficients" is selected)

*Figure 4-59.* Example of exported Excel file – FFT\_Parameters tab (When "FFT Parameter" is selected)

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Note : Values with \_FS are referenced to ADC Full Scale. Overlapped = 0 means that there is no harmonic superposition.



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Press 1 2 3 4 5 6 7 8 9 10 11 11 12 13 14	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H7 H8 H10 H11 H12	H7 B Frequency 0 1.895E+09 1.602E+09 2.97104645 2.196E+09 1.305E+09 1.305E+09 1.305E+09 1.305E+09 1.305E+09 1.008E+09 1.008E+09 710616302 1.188E+09	C C C C C C C C C C C C C C	A • D Idx 1 32190 77767 14424 106613 63344 28847 121036 48921 43270 126687 34498 57693	f Ali	gnemen F Freque	ency Le	G H vel Ida	,00 hbre 15 ntermod	J c <sup>c</sup> requen	K c Level	L Idex i	M nterleavin Fol4 Fol4+Fin Fol4-Fin Fol2-Fin	N Frequency 1.35E+09 2.151E+09 549034882 800965118	Chercher e ilectionner n Level -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 14 15	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13	H7 B Frequency 0 1.893E+09 1.602E+09 1.305E+09 1.305E+09 1.305E+09 1.305E+09 1.006E+09 1.006E+09 1.006E+03 710616302 1.188E+09 2.313E+09	C Level 3.010528 -0.31882 -64.0017 -55.6185 -84.6658 -84.6658 -84.7904 -100.73 -84.9291 -92.7601 -79.5434 -79.5434 -79.757 -93.6601 -31.9031 -9832	A • D Ids 1 32190 77767 14424 106613 63344 28847 121036 48321 43270 126867 34488 57633 112264	fa Ali	gnemen F Freque	ency Le	S H	intermod	J e <sup>e</sup> requen	K c Level	L Idex i	M nteleavin Fol4 Fol4+Fin Fol4-Fin Fol2-Fin	N Frequency 1.35E+09 2.151E+09 549034882 800965118	Chercher e lectionner n -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Press 1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14	Image: second system	C C C Level 3.010528 -0.91882 -0.91882 -0.91882 -0.91882 -64.0017 -55.6185 -84.6658 -84.7904 -100.73 -84.9291 -92.7601 -79.5434 -92.7601 -79.5434 -92.7601 -79.5434 -91.9031 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -89.7181 -80.9832 -80.9832 -80.9832 -80.9832 -91.882 -92.7601 -93.6601 -91.9031 -90.9832 -91.9931 -90.9832 -91.9931 	A • D 1dx 1 92190 77767 14424 106613 63344 26847 121036 48921 43270 126687 34438 57633 112264 20075	fs Ali f₂ E FinDT	gnemen F Freque	ency Le	S H	,ego hbre 13/ ntermod	J e <sup>r</sup> equen	K Cel	L Ida	M nterleavin Fol4 Fol4-Fin Fol2-Fin	N           Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e ilectionner n Level -73.2062 -79.2377 -63.2037 -66.7427	P Ids 65537 104420 26654 38884	Q	
Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H12 H13 H14	H7 B Frequency 0 1.895E+09 2.895E+09 2.97104645 2.196E+09 2.3105E+09 1.008E+09 1.008E+09 1.008E+09 1.008E+09 1.008E+09 2.313E+09 4.13511658 2.313E+09 4.13511658	C Level 3.010528 -0.91882 -0.91882 -64.0017 -55.6185 -84.6658 -84.9291 -92.7601 -79.5434 -97.757 -93.6601 -91.9031 -80.9832 -89.7181 -79.5892	A • 0 1dx 1 92190 77767 1406613 63344 28847 12106643 48921 43270 126687 34498 28687 1226687 34498 576533 112264 20075 72114	f Ali	gnemen F Freque	ency Le	G H vel Ida	,00 hbre 15 ntermod	J crequen	K c Level	L Idex	M nterleavin Foł4 Foł4+Fin Foł4-Fin Foł2-Fin	N           Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e ilectionner n Level -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 12	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H12 H13 H14 H15	H7 B Frequency 0 1.893E+09 1.602E+09 2.97104645 2.196E+09 1.305E+09 1.305E+09 1.305E+09 1.305E+09 1.305E+09 1.008E+09 710616302 1.188E+09 710616302 1.882E+09 710616302 1.318E+09 710616502 1.318E+09 710616502 7106502 7106502 7106	C Level 3.010528 -0.31882 -64.0017 -55.6185 -84.6658 -84.7904 -100.73 -84.9291 -92.7601 -79.5434 -97.757 -93.6601 -91.9031 -89.9181 -79.5886 -89.7181 -79.5886 -89.7181 -79.5886 -91.9172	A • D Ids 1 32190 77767 14424 106613 63344 28847 121036 48321 43270 126687 34498 57693 112264 20075 72116 97944	fa Ali	gnemen F Freque	ency Le	G H	intermod	J ¢requen	K Cel	L Idex	M nteleavin Fol4 Fol4+Fin Fol4-Fin Fol2-Fin	N Frequency 1.35E+09 2.151E+09 549034882 800365118	Chercher e lectionner n -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Pres: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 10 11 12 13 14 15 16 17 16 17 18 19 10 10 10 10 10 10 10 10 10 10	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H14 H11 H12 H11 H12 H14 H15 H16 H17	Image: second system	•         •         •           Police         •         •           Police         •         •           C         Level         3.010528           -0.91882         -64.0017           -55.6185         -84.6658           -84.9291         -92.7601           -79.5434         -90.7757           -93.6601         -91.9031           -80.9832         -89.7181           -79.5886         -91.6172	A • D 1dx 1 32190 77767 14424 106613 63344 28847 121036 48921 43270 121036 48921 121036 48921 121036 48921 12264 20075 72116 97841	F     Ali       f     E       FinDT	手 gnemen F Freque		S H	, ntermod	J e <sup>r</sup> equen	K Cel	L Ide Ide Ide Ide Ide Ide Ide Ide Ide Ide	M nterleavin Fol4 Fol4-Fin Fol2-Fin	N           Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e lectionner n -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Pres: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 20 20 20 20 20 20 20 20 20	A Fin H0 H1 H2 H3 H4 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H16 H17 H16 H17 H16 H17 H16 H17 H17 H17 H17 H17 H17 H17 H17 H17 H17	H7 B Frequency 0 1.895E+09 1.602E+09 2.9704645 2.196E+09 2.9704645 2.196E+09 5.94203290 2.493E+09 1.008E+09 891313934 2.61E+09 710616302 2.313E+09 413511658 1.485E+09 2.015E+09 1160E+09	C C C C C C C C C C C C C C C C C C C	A • D Idx 1 92190 77767 14424 106613 63344 28847 121036 48921 43270 126687 34498 57693 112264 20075 72116 97841 57652 20075	FinDT	gnemen F Freque	t 5	C H	,00 hbre 15 ntermod	style J e <sup>r</sup> requen	K C Level	L Idx I	M nterleavin Foł4 Foł4-Fin Foł2-Fin	N           •         filter * sé           Éditio            •         frequency           1.35E+09         2.151E+09           2.151E+09         549034882           800965118	Chercher e ilectionner n Level -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
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Press 1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 1	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H1 H1 H1 H1 H1 H1 H1 H1 H1 H1 H1 H1 H1	H7 B Frequency 0 1.893E+09 1.602E+09 297104645 2.196E+09 1.305E+09 1.305E+09 1.305E+09 2.493E+09 1.006E+09 2.313E+09 2.313E+09 2.313E+09 2.313E+09 1.188E+09 2.015E+09 116407013 1.782E+09 1.718E+09	•         •	A • D 1 102 103 103 103 103 106 106 106 106 106 106 106 106	F     Ali       f     E       FinDT	手 gnemen F Freque		So H	, ntermod	J erequen	Even Cell	L Ida I	M nterleavin Fol4 Fol4-Fin Fol2-Fin	Inter et R.           filter v 36           Éditio           4Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e lectionner n -73.2062 -73.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
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Press 1 2 3 4 5 6 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H11 H12 H13 H14 H15 H16 H17 H11 H12 H13 H11 H12 H13 H14 H15 H16 H17 H17 H17 H17 H17 H17 H17 H17 H17 H17	Image: second system	•         •	A • D 1 1dx 1 32190 77767 71424 106613 63344 28647 121036 48921 43270 126687 34498 57693 11264 20075 72116 97841 56539 83418 8773 100962 68995	F     Ali       f     E       FinDT	gnemen F Freque		G H	POO	J erequen	For Cel	L Idx I	M nterleavin Fol4 Fol4-Fin Fol2-Fin	Inter et R.           filter * 36           Édítio           4Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e lectionner n -73.2062 -73.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
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Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26	A Fin H0 H1 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H10 H11 H11 H12 H13 H14 H15 H16 H17 H18 H19 H11 H12 H21 H22 H21 H22 H23 H22 H23 H22	H7 B Frequency 0 1.895E+09 2.97104645 2.97104645 2.97104645 2.97104645 2.97104645 2.97104645 2.94209290 2.493E+09 1.008E+09 710616302 2.313E+09 413511658 1.486E+09 710616302 2.313E+09 1.188E+09 1.178E+09 1.277E+03 2.377E+03 1.277	C Level 3.010528 -0.91882 -64.0017 -55.6185 -84.6658 -84.7904 -100.73 -84.9291 -92.7601 -79.5434 -97.7757 -93.6601 -79.5434 -97.7757 -93.6601 -89.9832 -89.7181 -79.5886 -83.3175 -75.1717 -94.1341 -78.2761 -88.0873 -83.9346 -95.3181	A • D bldx 1 32190 77767 14424 106613 63344 28847 121036 43270 126687 34498 57693 112264 20075 72116 97844 20075 72116 86539 83418 8773 100962 88395 23196 115385	fa Ali	gnemen F Freque		G H vel Idx	,00 hbre 15 ntermod	J ¢requen	K c Level	L Idex :	M nteleavin Fol4 Fol4+Fin Fol2-Fin	N           Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e lectionner n -73.2062 -73.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 7 11 12 13 14 15 16 7 20 21 22 23 24 25 26 27 27 27 27 27 27 27 27 27 27	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18 H19 H11 H12 H13 H14 H15 H16 H17 H18 H19 H11 H12 H21 H22 H22 H22 H23 H24 H25	H7 B Frequency 0 1.893E+09 1.602E+09 2.97104645 2.196E+09 1.305E+09 1.305E+09 1.305E+09 1.305E+09 1.006E+09 2.493E+09 1.006E+09 2.313E+09 4.13511658 1.488E+09 2.015E+09 1.628E+09 1.628E+09 1.718E+09 1.718E+09 1.718E+09 1.421E+09 1.421E+09 1.124E+09 1.124E+09	C C Level 3.010528 -0.91682 -64.0017 -55.6185 -84.6658 -84.7904 -100.73 -84.9291 -92.7601 -79.5434 -100.73 -84.9291 -92.7601 -79.5434 -97.7757 -93.6601 -91.9031 -93.6015 -93.7181 -79.5886 -91.6175 -83.3175 -75.1717 -94.1341 -78.2761 -88.0873 -83.9346 -35.3181 -78.2761 -88.0873 -83.9346 -35.3181 -81.8405	A • D 1 132190 77767 14424 106613 63344 28847 121036 48921 43270 126867 34498 57693 11264 20075 72116 97841 5652 86539 83418 8773 100962 68995 23196 115385 54572	F     Ali       J     E       FinDT	gnemen F Freque		G H vel Idx	, ntermod	J e <sup>e</sup> requen	For Cel	L Ides	M nteleavin Fol4 Fol4-Fin Fol2-Fin	Inter et R.           filter v 36           Édítio           1.35E+09           2.151E+09           549034882           800965118	Chercher e lectionner n -73.2062 -73.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 23 24 25 26 27 20 27 20 20 20 20 20 20 20 20 20 20	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H15 H16 H17 H18 H19 H11 H15 H16 H17 H18 H19 H11 H15 H17 H18 H19 H20 H21 H21 H21 H21 H21 H21 H21 H21 H21 H21	Image: second system	C C Level 3.010528 -0.91882 -0.91882 -0.91882 -0.91882 -0.91882 -0.91882 -0.91882 -84.0017 -55.6185 -84.6658 -84.9291 -92.7601 -79.5434 -92.7601 -91.9031 -93.6601 -91.9031 -80.8832 -89.7181 -93.5886 -91.6172 -80.6155 -83.3175 -75.1717 -94.1341 -78.2761 -88.0873 -83.9946 -95.3181 -88.0873 -83.9946 -95.3181	A • • • • • • • • • • • • • • • • • • •	Fa       Ali       fx       E       FinDT	F Freque		C H	ntermod	J e <sup>r</sup> equen	K c Level	L Idx I	M nterleavin Fol4 Fol4-Fin Fol2-Fin	N           Frequency           1.35E+09           2.151E+09           549034882           800965118	Chercher e electionner n Level -73.2062 -79.2377 -63.2037 -66.7427	P Ids 65537 104420 26654 38884		
Press 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 1 1 2 2 2 2 2 2 1 2 2 1 1 1 1 1 2 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1	A Fin H0 H1 H1 H3 H4 H5 H6 H7 H8 H9 H10 H11 H14 H15 H6 H17 H18 H19 H11 H11 H11 H11 H11 H12 H11 H11 H12 H11 H12 H13 H14 H15 H16 H17 H17 H17 H17 H17 H17 H17 H17 H17 H17	Image: second system	C Level 3.010528 -0.91882 -64.0017 -55.6185 -84.6658 -84.7904 -100.73 -84.9291 -79.5434 -97.7757 -93.6601 -79.5434 -97.7757 -93.6601 -79.5434 -97.7757 -93.6601 -79.5434 -97.7757 -93.6601 -79.5434 -97.7757 -93.6601 -79.5434 -97.757 -93.6601 -91.031 -80.9832 -89.7181 -79.5886 -93.3175 -75.1717 -94.1341 -78.2761 -88.0873 -83.9346 -95.3181 -81.8405 -81.8405	A D bdx 1 32190 77767 14424 106613 63344 28647 121036 43270 126687 34498 57693 112264 20075 72116 97844 20075 72116 97844 20075 72116 97844 20075 72116 97845 86539 8418 8773 100962 86395 23196 115385 54572 INL  FF	fa Ali	gnemen F Freque	t 5	G H vel Idx	Intermod	Style J erequen	K c Level	L Ida i	M nterleavin Foł4 Foł4-Fin Foł2-Fin encies	Inter et R.           filtrer * sé           Éditio           N <b>Frequency</b> 1.35E+09           2.151E+09           549034822           800965118	Chercher e electionner n Level -73.2062 -79.2377 -63.2037 -66.7427	P Idx 65537 104420 26654 38884	Q	
Press 1 2 3 4 5 6 7 8 9 10 11 12 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 24 25 26 27 4 27 27 27 27 27 27 27 27 27 27	A Fin H0 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18 H19 H11 H12 H13 H14 H19 H11 H12 H13 H14 H22 H23 H24 H25 H24 H25 H24 H25 H24 H25 H24 H25 H24 H25 H24 H25 H27 H27 H27 H27 H27 H27 H27 H27 H27 H27	Image: second system	Police           Police           C           Level           3.010528           -0.91882           -64.0017           -55.6185           -84.6658           -84.7904           -100.73           -84.9291           -92.7601           -79.5434           -97.7757           -93.6601           -91.9031           -80.9832           -89.7181           -79.5886           -91.6175           -83.3175           -75.1717           -94.1341           -78.2761           -78.2761           -83.3175           -75.1717           -94.1341           -78.2761           -83.9346           -95.3181           -95.3181           -83.9346           -95.3181           -81.8405	A • 0 0 10 10 10 10 10 10 10 10 10	F     Ali       J     E       FinDT	F Freque	t s	So H Non	I I I I I I I I I I I I I I I I I I I	J erequen TModule	K c Level	L Idx I	M nteleavin Fol4 Fol4-Fin Fol2-Fin encies	Inter et Ri         filter v 36         Éditio         4Frequency         1.35E+09         2.151E+09         549034882         800965118	Chercher e electionner n C Level -73.2062 -73.2377 -63.2037 -66.7427 -66.7427	P Idx 65537 104420 26654 38884		

Figure 4-60. Example of exported Excel file – Harmonics\_IM tab (When "FFT Parameter" is selected)

This tab displays all spectral components, including DC component (H0), the fundamental (H1) and interleaving spurs.



#### FFT calculations

#### 4.5.6.2. Data exportation in CAN test

EV12AS350x-EB GUI		
e ?		
Teledyne EV12AS350x-EB GUI e2v	SPI <ul></ul>	Do Interpolation SYNC
System Start Stop	Snap Software Trig	Do Training
Setting Test LUT Interleaving Calibration:	s Acquisition Export Debug	
Excel Data Saving		
File : FFT Spectr	rum FFT Parameters	INL Coefficients
CAN Test Data Saving		
File : C:\Users\adminlocal\Desktop\FFT EV12AS350E	3.txt	
	ChipID:6.3.4 FPGA:1:3.2 FW:1.0.9 CRC - Sync - OTP	System :

Note : CAN test is a proprietary format.

This mode is activated by checking the box in the CAN Test Data Saving Menu.



With this mode, only the sampled signal can be saved.

The procedure to be followed to save Sampled Data in a CAN Test file is:

- 1. Indicate the path of the file
- 2. Give a name to the file.
- 3. Then click on the "**Snap**" button of the System Menu to launch the acquisition and save the sampled signal in a text file with CAN Test format, as example shown on Figure 4-62.

Notes:

1. If the given file name already exists, the user is asked to confirm he wants to overwrite the existing file as shown on figure below:

Figure 4-61. Overwrite window

ſ	teter Overv	vrite
	?	C:\Users\adminlocal\Desktop\FFT EV12AS350B.txt already exists. Overwrite it ?
		OK Cancel

2. When launching an acquisition in the Freerun mode followed by clicking on the "Start" button from System Menu, only the 1<sup>st</sup> acquisition is saved even if the user is continuing successive acquisitions.



3. Notes concerning CAN Test file

Sampled Data is saved on different lines with the following order: Core A, Core C, Core B and finally Core D.

The header in described below:

•

- #Clock Frequency = xxx Frequency of ADC external clock • •
  - #Input Frequency = xxx Frequency of Analog input signal
  - #Resolution = 12 ADC resolution
- #Number of samples Number of samples in the sampled signal •
  - #Signed Encoding Mode = 0 0 means a Two complement coding
- • # Values It indicates the end of the header. Following lines are the sampled data

Figure 4-62. Example of exported CAN test file (4 ADC cores interleaved)





# 4.5.7 Debug

This tab can be used for debug (advanced mode) and is therefore not recommended. It enables to read or write register values manually

Field @0x is used to provide the address (in Hexadecimal) of the register to be read or written.

The two other fields are used to display the read value or to write values at the selected address. Values read/written are displayed in both Binary (**b**) and Hexadecimal format (**0x**).



📰 EV12AS350x-EB GUI
File ?
Teledyne EV12AS350x-EB GUI       SPI       Hardware Reset       Do Interpolation         E2v       Temperature Low       Refresh       SYNC
System Start Stop Snap Software Trig Do Training
Setting         Test         LUT         Interleaving Calibrations         Acquisition         Export         Debug           Ouad         ADC 12bit Registers :
@ 0x b 0x
Read Write Binary Value Write Hex Value
ChipID:6.3.4 FPGA:1:3.2 FW:1.0.9 CRC 🍚 Sync 🍚 OTP 🍚 System : 🍚 🤤



Example: OTP\_SPI\_SELECT is a register of the channel A, B, C, D and the MASTER SPI. It is the same address for channel and MASTER SPI

SPI Instruction (in hexa)

1- Channel A selected : Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 00 FFFF
2- CHANNEL B selected Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 01 FFFF
<b>3-</b> CHANNEL C selected Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 02 FFFF
4- CHANNEL D selected Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 03 FFFF
5- MASTER selected Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 07 FFFF
6- All selected (OTP value) Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 04 0000
7- All selected (SPI value) Write @CHANNEL_SELECT Write @ OTP_SPI_SEL	@0x 04 FFFF



# 4.5.8 ADC Calibrations / interpolation

Several options are considered for ADC interleaving calibrations:

- OTP mode: Using calibration values defined in OTP Temperature High registers
- OTP mode: Using calibration values defined in OTP Temperature Low registers
- SPI mode: Using user's defined values (calibrations need to be done by the user after each powerup)
- SPI mode: Interpolate calibrations at the temperature of use. This interpolation mode provides the best dynamic performances regarding the level of interleaving spurs. It is therefore the recommended option

The choice between the different options is done via the Header Menu of figure 4-64:

#### Figure 4-64. User Interface Header Menu

EV12AS350x-EB GUI	
File ?	
Teledyne European En Cur	OTP   Hardware Reset Do Interpolation
e2v EV12AS350X-EB GOI	Temperature Low  Refresh SYNC

Note that parameters that are not linked to ADC interleaving calibrations (such as CM\_IN and R\_IN) are not affected by above choice, since it exists only two choices:

- OTP values (valid whatever the temperature range)
- SPI values (default values or user defined values)

#### 4.5.8.1. OTP Temperature Low calibrations

This configuration is to be used for junction temperature lower than 70 °C (ambient and cold temperatures). It corresponds to CAL\_SET\_SEL register defined in Master SPI of the ADC (CAL\_SET\_SEL=1).

It is the mode by default when opening the GUI.

Figure 4-65.	Header Menu with "OTP Temperature Low"	selection
--------------	--	-----------

OTP 👻	🚱 Hardware Reset	[Do Interpolation]
Temperature Low 🔻	Refresh	SYNC
	OTP    Temperature Low	OTP    Hardware Reset  Temperature Low  Refresh



EV12AS350BTP-EB Evaluation Board
This configuration is to be used for junction temperature higher than 70 °C (hot temperature). It corresponds to CAL\_SET\_SEL register defined in Master SPI of the ADC (CAL\_SET\_SEL=0).

*Figure 4-66.* Header Menu with "**OTP Temperature High**" selection

EV12AS350x-EB GUI	
File ?	
	OTP    Mardware Reset  Do Interpolation
e2v EV12AS350x-EB GOI	Temperature High   Refresh SYNC

4.5.8.3. SPI User's defined calibrations

With this option the user doesn't use OTP values anymore and write his own calibration values (interleaving calibrations). This is done in the "Interleaving calibrations" tab from the GUI. Please refer to chapter 4.5.4. This option is an advanced mode and is reserved to expert users.

When the user wants to switch from OTP mode to SPI mode, the user is asked to select between the two choices of figure 4-67 (in order to avoid getting the SPI default values that would lead to high interleaving spurs).

- Launch a "**Do interpolation**" procedure at the temperature of use. See chapter below.
- Write OTP calibration values within the SPI registers: The user is asked to select which OTP values need to be written within SPI (OTP Temperature Low or OTP Temperature High)

<b>igure 4-07.</b> Of i values selection pop-up window
--

SPI values selection	SPI values selection
Do you want to :	Do you want to :
<ul> <li>Write OTP values in SPI in interpolating interleaving calibrations to the temperature specified below</li> <li>Device Temperature :</li> <li>Vdiode : 830 mV + Tj diode : 52°C +</li> </ul>	Write OTP values in SPI in interpolating interleaving calibrations to the temperature specified below         Device Temperature :         Vdiode :       830 mV +         Tj diode :       52°C +
Write OTP values in SPI Temperature High   CK Cancel	Write OTP values in SPI      Temperature High     Temperature High     Temperature Low     OK     Cancel

Note: Interpolation of calibrations at the specified temperature are referenced to diode which is 7 °C below hot spot temperature

Note: When SPI mode is selected; R\_IN and CM\_IN values (defined in the Settings tab) are the values from SPI (no more OTP values).

- R\_IN and CM\_IN have their SPI default values after a hardware or software reset
- R\_IN and CM\_IN have their previous SPI values if no reset has been done (for instance, if R\_IN is modified to value 12, switching to OTP mode will cause the R\_IN value to switch to the value defined in OTP. When coming back to SPI mode, R\_IN value will come back at the value 12 even if the SPI default value is 8).



#### 4.5.8.4. Interpolated calibration: "Do Calibration"

This option will lead to optimum performances in terms of interleaving spurs.

This option is accessible in SPI mode only. When switching from OTP mode to SPI mode, the user has to select the first choice (interpolation of calibrations at the specified temperature. Reference is the diode which is 7 ℃ below hot spot temperature)



SPI values selection	SPI values selection
Do you want to :	Do you want to :
<ul> <li>Write OTP values in SPI in interpolating interleaving calibrations to the temperature specified below</li> <li>Device Temperature :</li> <li>Vdiode : 830 mV + Tj diode : 52°C +</li> </ul>	● Write OTP values in SPI in interpolating interleaving calibrations to the temperature specified below Device Temperature : Vdiode : 762 mV ⊕ Tj diode : 100 mC ⊕
Write OTP values in SPI Temperature High	Write OTP values in SPI Temperature High
OK Cancel	OK Cancel

Before clicking on "OK", be sure your have well filled the junction temperature (either through junction temperature expressed in °C either by Vdiode expressed in mV).

The principle consists in reading the OTP value dedicated to the calibration at cold temperature, then reading the OTP value dedicated to the calibration at hot temperature and then interpolate the value for the temperature of interest (Ti measured at diode which is 7 °C below hot spot temperature) and write it via the SPI.

Interpolation formula is given below: Equation 1 - Interpolation formula

Register ( $V_{diode}$ ) = ( $R_0$ - $R_1$ )/(787-830) \* ( $V_{diode}$ -830) +  $R_1$ 

With:

Vdiode = Value of the diode of temperature for the considered temperature in mV.  $R_1$  = Register when CAL\_SET\_SEL=1 is selected and  $R_0$ =Register when CAL\_SET\_SEL=0. Register = each register listed in Table 1 below.

Registers to be interpolated over temperature are listed in Table 1.

Table 1. List of registers to be interpolated over temperature for optimum calibrations.

Registers in Master SPI	Registers in Channel SPI
A_OFFSET_CAL	CAL1
B_OFFSET_CAL	CAL2
C_OFFSET_CAL	CAL3
D_OFFSET_CAL	CAL4
	CAL5
	CAL6
	CAL7
	GAIN_CAL
	INT_GAIN_CAL
	PHASE_ CAL



Once ADC is in SPI mode, the interpolation procedure can be launched at any time in pressing the "**Do Interpolaton**" button from the Header Menu.

Figure 4-69.	Header Menu in SPI mode – access to "Do Interpolation" button
- g	

EV12AS350x-EB GUI			
File ?			
Teledyne EV12AS350x-EB GUI	SPI -	🚱 Hardware Reset	Do Interpolation
	Temperature Low 🔻	Refresh	SYNC ]

Pressing the "Do Interpolation" button opens the window of figure 4-69:

*Figure 4-70.* Do Interpolation window

Do you want to :			
Write OTP values in SPI	in interpola	ting interleaving	calibrations
Device Temperature :	cified below		
bevice reliperature .			
Vdiode: 888 mV 😤	Tj diode :	0°C	
Write OTP values in SPI	[		
Temperature High 💌			
		OK	Cancel
		UN	Cancel

The user indicates the current junction temperature of the DAC (either through junction temperature expressed in  $^{\circ}$ C either by Vdiode expressed in mV).

The junction temperature is referenced to the diode which is 7 °C below hot spot temperature.





# 4.6 Troubleshooting

### 4.6.1 Software installation

Check that you own rights to write in the directory (administrator rights). Check for the available disk space. Check that the USB port is free and properly configured

Figure 4-71. USB Port Driver Configuration



Warning: this installation is done for one USB connector only. If USB connector is changed, USB driver need to be re-installed before use.



### 4.6.2 Regional and Language options

Use a control Regional Setting to check if decimal separator is configured with a dot ".".



ormats Lo	ocation Keyboards and Languages Administrative
To change time, selec	e the way your computer displays numbers, currencies, dates, and ct an entry from the format list.
Eronch /E	
French (F	rance)
Examples	of how data is displayed using this format:
Number:	123 456 789,00
Currency:	123 456 789,00 €
Time:	15:08:25
Short date	e 06/08/2010
Long date	: vendredi 6 août 2010
	C <u>u</u> stomize this format
For additi	onal formats, keyboards, and tools, go to the Microfoft website.

On Figure 4-72, press on « Customize this format..." button to get the window displayed in Figure 4-73.

Figure 4-73. Customize Regional Options

lumbers Cu	irrency Time Date		
Example			
Positive:	123 456 789,00	Negative: -123 456	5 789,00
Decim	al symbol:	[]	•
<u>N</u> o. of	digits after decimal:	2	•
Digit g	prouping symbol:		•
Digit g	rouping:	123 456 789	•
Negati	ive sign symbol:	-	•
Negati	ive number format:	-1,1	-
Display	y leading zeros:	0,7	•
<u>L</u> ist se	parator:	;	•
Measu	rement system:	Metric	•
Standard digits:		0123456789	•
Use native digits:		Never	•
Click Reset	to restore the system de	fault settings for	Reset

Sheet Numbers: the decimal separator must be configured with a dot "."



1210A



### 4.6.3 Start-up procedure

Check that supplies are properly connected and powered ON. Check that RF generators are properly connected and powered ON. Check if USB connector is properly plugged. Check if jumpers are configured as described in paragraph 3.5.

### 4.6.4 Measurement

If low dynamic performances and/or high interleaving spurs are obtained:

ADC used in OTP mode:

- Check that the temperature selected (Temperature High or Temperature Low) is suitable to the real junction temperature of the ADC (Temperature Low is recommended for ambient).
- If a Do Interpolation procedure has been launched, verify that the specified junction temperature is close to the real junction temperature of ADC.

ADC used in SPI mode:

• If ADC is used in SPI mode and if a Hardware reset is done, ADC calibrations will come back to their default values, meaning that ADC interleaving calibration is not appropriate.

If level of 2<sup>nd</sup> harmonic (H2) is high:

- Verify that your cables on Analog input are matched
- Verify that cables are fully tightened with an automatic reset wrench



• The SMA connectors Southwest can be unscrewed. If this is the case check their alignment on the PCB trace before screwing again the SMA connectors







Section 5

FFT calculations

This chapter describes how the different FFT parameters are calculated. FFT parameters are calculated by using the formula below based on rms spectral components:

Spectre<sub>i</sub> =  $\sqrt{2} \frac{FFTModule_i}{N}$  (rms value) With N = number of samples used in the FFT

Output spectrum expressed in dB or dBc are calculated with the following formula:

$$spectre_{dB_{pk}} = 20\log(\frac{\sqrt{2*spectre_i}}{\frac{2^{Résolution} - 1}{2}}) \quad ; \quad spectre_{dB_c} = 20\log(\frac{spectre_i}{Max(spectre_i)})$$

With2<sup>*Resolution*</sup>, Resolution being the resolution of the ADC (12-bit)



# 5.1 Nomenclature

	$\sum_{n=1}^{N}$ spectre <sup>2</sup>			
Sig	Signal power = $\begin{bmatrix} 0 \\ 0 \end{bmatrix}$			
H0	Power of DC component = $\frac{spectre_i^2}{spectre_i^2}$ with i =0 = index of the DC component			
H1	Power of the fundamental = $\frac{spectre_i^2}{1}$ with i = index of the fundamental			
H2	Power of 2nd harmonic = $\frac{spectre_i^2}{spectre_i^2}$ with i = index of the 2nd harmonic			
Setup.cal/Nbr	OfHarmonics is the number of harmonics taken into consideration for THD calculation in the			
Harmonics is t	the index of the harmonic in the spectra setup.cal.NbrOfHarmonics $\sum spectre_i^2$			
H1i	Power of 1st tone harmonics = $Harmonics$ (over Nyquist) with i = index of the i <sup>th</sup> harmonic of the first tone.			
	setup.cal.NbrOfHarmonics			
H2i	Power of 2nd tone harmonics = $\sum_{Harmonics} spectre_i^{-}$ (over Nyquist) with i = index of the i <sup>th</sup> harmonic of the 2 <sup>nd</sup> tone.			
	setup.cal.NbrOfHarmonics			
H1i_NB	Power of 1st tone harmonics in Narrow Band = $\sum_{Harmonics} Spectre_{i}^{2}$ (over Narrow Band)			
	setup.cal.NbrOfHarmonics $\sum_{i}^{i}$ spectre;			
H2i_NB	Power of 2nd tone harmonics in Narrow Band = Harmonics (over Narrow Band)			
IMx	Power of an intermodulated spur = $spectre_{i(x)}^2$ over Nyquist with x being the intermodulation iF1 ± jF2 with i & j integer			
IMx_NB	Power of an intermodulated spur in Narrow band = $spectre_{i(x)}^{2}$ at x index (over Narrow Band)			
MaxSpur	Level of the highest spur excluding the DC component and the fundamental (1 <sup>st</sup> tone and 2 <sup>nd</sup> tone if applicable) over the considered band of interest (Nyquist or Narrow Band if applicable)			
PmaxSpur	Power of the highest spur excluding the DC component and the fundamental (1st tone and 2 <sup>nd</sup> tone if applicable) over the considered band of interest (Nyquist or Narrow Band if applicable)			
Setup.cal.Nbr	OfInterleaving is the number of interleaving spurs taken into consideration in the calculation. In single tone: $Fc/2 \pm F1$ , $Fc/4 \pm F1$ In dual tone: $Fc/2 \pm F1$ , $Fc/4 \pm F1$ , $Fc/2 \pm F2$ , $Fc/4 \pm F2$			
Pint	Power of interleaving spurs = $\sum_{Harmonics}^{setup.cal.NbrOfInterleaving} (over Nyquist)$			
Pint_NB	Power of interleaving spurs in Narrow band = $\sum_{Harmonics}^{setup.cal.NbrOfInterleaving} spectre_i^2 \text{ (over Narrow Band)}$			



# 5.2 Overlap of spurs

If there is an overlap of an interleaving spur with a harmonic (spurs having the same frequency), it is no more possible to discriminate the contribution of each spur. In that case, no calculation will be done and the overlap LED of the FFT parameter window will switch to RED color.

There is no issue if two spurs of same nature are overlapped (2 harmonics for instance). In that case, the power is taken into account once in the calculations.

## 5.3 Calculations

### 5.3.1 Initialisation of calculations

We define the following values;

- Pf : Power of the fundamental (2 tones if Dual tone)
- Mf : Power of the highest fundamental
- Ph : Power of harmonics
- Ph\_NB: Power of harmonics in narrow band
- Ps : Power of spurs in narrowband (includes fundamentals, harmonics, intermodulation spurs and interleavings spurs if any but not DC component)
- Pn : Power of Noise (ie all spurs excluding DC component, fundamentals, harmonics, intermodulation spurs and interleaving spurs if any)
- Nb : Number of point for noise

The following calculations need to be done:

- Pf = H1
- $M_f = H1$
- Ph = H1i
- $Ph_NB = H1i_NB$
- $Nb = N_{Sig} N_{H0} N_{H1} N_{H1i}$



Acquisition in Single or Dual tone?			
Single tone	Dual tone		
$Pn = Sig - H0 - Pf - Ph$ $Ps = Ph_NB$	$\begin{array}{l} Pf = Pf + H2\\ M_{f} = Max(M_{f}; H2)\\ Ph = Ph + H2i\\ Ph_NB = Ph_NB + H2i_NB\\ IM = \sum_{0 < i, j < IMDOrder - 1} IM_{iF1+jF2} + IM_{ iF1-jF2 }\\ 2 < i + j < IMDOrder \\ (Intermode Nyquist)\\ IM_NB = \sum_{0 < i, j < IMDOrder - 1} IM_NB_{iF1+jF2} + 2 < i + j < IMDOrder \\ 2 < i + j < IMDOrder \\ IM_NB_{ iF1-jF2 } (Intermode bande étroite)\\ Pn = Sig - H0 - Pf - Ph - IM\\ Ps = Ph_NB + IM_NB\\ N_b = N_b - N_{H2} - N_{H2i} - N_{IM}\\ TIMD_{dBc} = 10 \log\left(\frac{IM_NB}{Pf}\right)  \text{if IM_NB is different}\\ from 0\\ IMD3(-)_{dBc}\\ = 10 \log\left(\frac{Mf}{max(Spur(2F1 - F2); Spur(1F1 - 2F2))}\right)\\ (For Narrow band, if one of the two IMD3 (-) spurs is not within the band, then it needs not to be taken into consideration.\\ If no IMD3(-) spur is detected within the narrowband, IMD3 is not calculated)\\ \end{array}$		

## 5.3.2 Acquisition in Single or Dual tone?

## 5.3.3 Acquisition with 4 ADC cores aligned or interleaved?

Acquisition with 4 ADC cores interleaved?								
4 cores aligned	4 cores interleaved							
Do nothing	$\begin{array}{l} P_n = P_n - S_{int} \\ N_b = N_b - N_{int} \\ \text{With N}_{\text{int}} \text{ the number of interleaving spurs} \\ \text{Nint} = 4 \text{ in single tone and 7 in Dual tones} \\ P_S = Ph\_NB + S_{int\_}NB \\ TILD_{dBc} = 10 \log \left( \frac{S_{int\_NB}}{P_f} \right)  \text{if Sint\_NB different} \\ \text{from 0} \end{array}$							



Remove TD term if it was not possible to calculate it

### 5.3.4 Performances calculation in dBc

• 
$$SNR_{dBc} = 10 \log\left(\frac{Pf}{Pn}\right)$$

• With Narrow Band :  $SNR_{dBc} = SNR_{dBc} + 10 \log \left(\frac{\frac{Fc}{2}}{Bandwidth of Interest}\right)$  because we consider that thermal noise is dominant compared to jitter

•  $THD_{dBc} = 10 \log \left(\frac{Ph_NB}{Pf}\right)$  If Ph\_NB different from 0

• 
$$TD_{dBc} = 10 \log \left(\frac{Ps}{Pf}\right)$$
 If Ps different from 0

• 
$$SINAD_{dBc} = -10 \log \left( 10^{-\frac{SNR_{dBc}}{10}} + 10^{\frac{TD}{dBc}} \right)$$

• 
$$ENOB_{dBc} = \frac{SINAD_{dBc} - 10\log(1.5)}{6.02}$$

• 
$$SFSR_{dBc} = 10 \log \left( \frac{Mf}{\left( \frac{2Resolution_{-1}}{2\sqrt{2}} \right)^2} \right)$$

• 
$$SFDR_{dBc} = 10 \log\left(\frac{PmaxSpur}{Mf}\right)$$

### 5.3.5 Performances calculation in dBFS

•  $AverageNoise = 10\log(\frac{2*Pb}{N_b \left(\frac{F_c}{N}\right)*\left(\frac{2^{Resolution}-1}{2\sqrt{2}}\right)^2})$  (Noise floor)

• 
$$SNR_{dBFS} = SNR_{dBc} - SFSR_{dBc} - 10\log\left(\frac{Pf}{Mf}\right)$$

• 
$$THD_{dBFS} = THD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$$

• 
$$TD_{dBFS} = TD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$$

• 
$$SINAD_{dBFS} = -10 \log \left( 10^{-\frac{SNR_{dBFS}}{10}} + 10^{\frac{TD_{dBFS}}{10}} \right)$$

• 
$$ENOB_{dBFS} = \frac{SINAD_{dBFS} - 10\log(1.5)}{6.02}$$

- $SFDR_{dBFS} = SFDR_{dBc} + SFSR_{dBc}$
- $TIMD_{dBFS} = TIMD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$
- $TILD_{dBFS} = TILD_{dBc} + SFSR_{dBc} + 10\log\left(\frac{Pf}{Mf}\right)$

• 
$$IMD3(-)_{dBFS} = IMD3(-)_{dBc} - SFSR_{dBc}$$





# Section 6

# **FPGA** Code

FPGA code was developed to be used with a FPGA ALTERA ARIA V model 5AGXB3 (model used on the Evaluation Board).

#### 6.1 **FPGA** functionalities

FPGA enables:

- Synchronization of FPGA \_ ADC interface via its reset sequence and external SYNC (training) •
- . Acquisition of ADC data (sample and control bit) at 3.5GSps per port with a memory 256Ks
- To descramble the data for test mode PRBS and data •
- To launch an acquisition directly (free run mode) or triggered by an event
- To transmit the acquisition data toward USB and restart the acquisition

Limitation: FPGA does not support ADC clock frequency variation during the functioning.

#### 6.2 **FPGA** programming

The FPGA programming can be done with Quartus Programmer. The file .pod is delivered on the CD-ROM of the Evaluation Board.

\FPGA\FPGA-v3.2\bin\fpga top.pof

Below is the procedure to load the pof file into EEPROM.

Note: EV12AS350 Evaluation Board is delivered with FPGA code already loaded in the EEPROM. The procedure below is necessary in the only case when the user wants to download a new FPGA code.

1. Connect USB Blaster cable on one USB port of the PC in order to be recognized by the software.

		USB Blaster			
PC		Rev C	BLASTER SIDE	ALTERA	
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#### FPGA Code

- 2. Open Quartus II 14.1 Programmer 🥑 Firefox 🏉 Internet Explorer (64 bits) 🥖 Internet Explorer 🖸 Lecteur Windows Media Microsoft Excel 2010 Nicrosoft OneNote 2010 Microsoft Outlook 2010 P Microsoft PowerPoint 2010 Microsoft Word 2010 🔯 National Instruments LabVIEW 2010 SP1 (32-bit Mational Instruments TestStand 2010 🔀 NI MAX 📗 7-Zip Altera 14.1.0.186 퉬 Quartus II Programmer and Tools 14.1.0.186 Quartus II 14.1 Programmer QuartusProgram 🗟 Quartus II 14.1 SignalTap II merSetup-14.1.0. Quartus II 14.1 System Console 186-windows.ext 💐 Uninstall Quartus II Programmer and To
- 3. Click on the "Hardware setup..." button.

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4. Select USB-Blaster (if USB-blaster is not displayed, click on "Add Hardware ..." button)

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USB-Blaster			Local	USB-0	Remove Hardware
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### 5. Select mode "active serial programming"

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### FPGA Code

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8. Connect USB Blaster on JTAG connector of the Evaluation Board

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USB	ALTERA	)			un ,

9. Power ON FPGA (5V5 supply)



10. Click on start





TELEDYNE C2V Everywhereyoulook Once programming and verification are completed, the progress status displays 100% (successful). A message is also displayed in the bottom of the window.

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System (8) / Processing /		

FPGA Code

#### 6.3 **FPGA VHDL code**

The Top level architecture of VDHL code is described below:

Figure 6-1. VHDL Top Level Simplified Block Diagram



FPGA State Machine is described below.



**TELEDYNE C2V** Everywhereyoulook"

Figure 6-2. FPGA State Machine

The chosen configuration mode to program FPGA is Active Serial x4.

Arria V GX B3 Bitstream size is 138 416 696 bits.

The EEPROM memory is EPCQ256 with 268 435 456 bits (several EEPROM can be mounted to select different configurations).

Data is written into EEPROM by Active Serial Mode.

# 6.4 FPGA Training procedure

FPGA Training procedure is described below:

- IDLE
- SAVE CONTEXT
  - Read CHANNEL\_SEL Register and store value
  - Write CHANNEL\_SEL Register to 0 to select Channel A
  - Read TEST\_MODE Register and store value
  - Read FLASH\_LENGTH Register and store value
- INIT
  - Write CHANNEL\_SEL Register to 4 to select all channels
  - Write FLASH\_LENGTH Register to 23
  - Enable Test Mode
  - Do SYNC
- SET FLASH 23
  - Write TEST\_MODE Register to 5 to select Flash Mode
- WAIT LOCK
  - Wait that all PLL and DPA are locked
  - Lock DPA values
- ALIGN BY PORT
  - Fill the whole buffer with incoming data
  - Search an address where all bits of the port are 0
  - Increment address
- For each increment make a bitslip action for each 1 until all bits of the port are 1
- SET RAMP
  - Write TEST\_MODE Register to 9 to select Ramp Mode
- ALIGN ALL PORTS
  - Fill the whole buffer with incoming data
  - Read a data on each port at the same address, if it is too close to 0 read another data at another address until the data is enough far to 0
  - Freeze address counter of the earliest ports until the distance with the latest is less or equal to 4.
  - Apply bitslip on all bits of the earliest port until the gap between all ports is null
- CHECK RESULT
  - Fill the whole buffer with incoming data
  - Read all ports at a random address and check if the data is the same



#### FPGA Code

- RESTORE CONTEXT
  - Restore FLASH\_LENGTH Register

  - Restore TEST\_MODE Register
     Restore CHANNEL\_SEL Register
- return to IDLE state .





# Section 7

# Ordering Information

Table 1.Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AS350BTPY-EB	EBGA380 RoHS	Ambient	Prototype	Evaluation board mounted with EVP12AS350BTPY ADC

