EV12AQ600-FMC-EVM User guide

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If you require any support, please contact your local FAE or send an email at GRE-HOTLINE-BDC@Teledyne.com.

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conditions of sale in respect of infringement of third party patents arising from the use of the devices in accordance with information contained herein.

2 Introduction

The EV12AQ600-FMC-EVM is an evaluation board used to evaluate the EV12AQ600/605 ADCs.
The EV12AQ600/605 are the first 12-bit, quad, dual or single-channel C-band capable ADCs with RF sampling up to 1.6, 3.2 or 6.4 GSps.

The EV12AQ600/605 ADCs main features are:

- 4 input channels with 4.5 / 6.5 GHz selectable analog input bandwidth (-3dB).
- A built-in Cross-Point-Switch (CPS) allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates.
  - In 4-channel mode, the four cores can sample, in phase, four independent inputs at 1.6 GSps.
  - In 2-channel mode the cores are interleaved by 2 in order to reach 3.2 GSps sampling rate on each of two inputs.
  - In 1-channel mode a single input is propagated to each of the four cores which are interleaved by 4 in order to reach a sampling rate of 6.4 GSps.
- 4 ADC cores sampling at 1.6 GSps max which can be used independently or interleaved
- An ADC input clock (CLK) up to 6.4 GHz max
- A serial link and data sampling synchronization input signal, the SYNCTRIG input.
- A synchronization output signal for multi-ADC synchronization, the SYNCO input.
- An ESIstream serial interface allowing data transmission to a logic device. With lane rate up to 12.8 Gbps, $f_{CLK} = f_{serial}/2$, (Protocol specification and license free VHDL ESIstream RX IP available on www.esistream.com).
- An SSO, Slow Synchronization Output clock used as clock reference for serial link receiver $f_{SSO} = f_{CLK}/32$.
- A 2.5V and 3.3V SPI registers configuration interface.

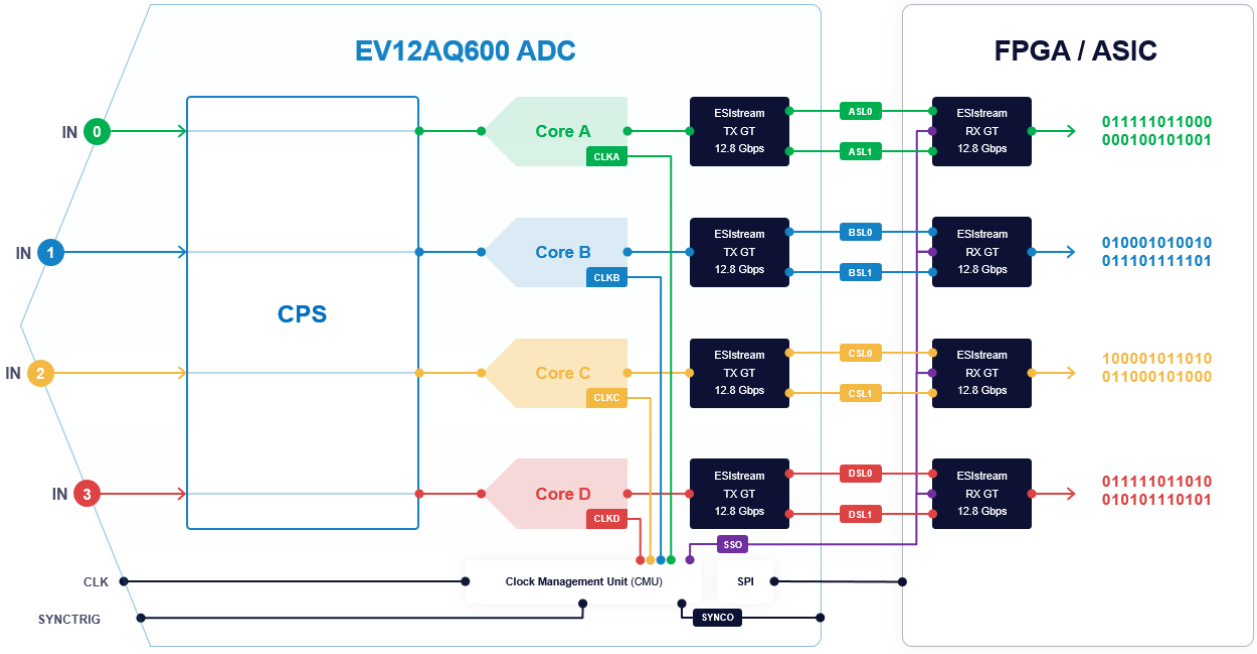
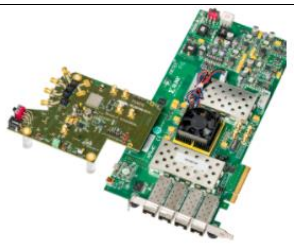


Figure 1 – EV12AQ600/605 architecture overview.

3 Quick start

3.1 Hardware and software

The table below lists the FPGA carrier boards validated to support the EV12AQ600-FMC-EVM.

FPGA FMC/FMC+ carrier board reference	FMC/FMC+ connector type	VHDL design example on Check ESIstream website	VHDL design example User Guide Check ESIstream website	Boards assembly
ADA-SDEV-KIT2	FMC+ HPC	Download ADA-SDEV-KIT2 VHDL design example	Download VHDL design example user guide	
KCU105	FMC HPC	Download KCU105 VHDL design example		
VC709	FMC HPC	Download VC709 VHDL design example		

3.2 System setup

Complete the following steps to install the EV12AQ600-FMC-EVM to a FPGA carrier board. For additional information on FPGA carrier boards, refer to the manufacturer board's user guide.

1. Turn off the DC power switch (SW1) and disconnect the input power source (J8) from the EV12AQ600-FMC-EVM and from the FPGA carrier board.
2. Install the EV12AQ600-FMC-EVM board to the FPGA carrier board FMC or FMC+ connector.
3. Connect the input power source to the FPGA carrier board and then to the EV12AQ600-FMC-EVM (J8).
4. Turn the FPGA carrier board power input switch to ON and then turn the EV12AQ600-FMC-EVM power input switch ON (SW1). The system is now ready for use.

3.3 Technical support

The EV12AQ600-FMC-EVM is compatible with standard high pin count (HPC) FMC and FMC+ interfaces. Please contact your local FAE or Teledyne-e2v support at GRE-HOTLINE-BDC@Teledyne.com for more information **or support on others FMC/FMC+ FPGA carrier boards.**

4 Board technical description

The EV12AQ600-FMC-EVM is a partially populated High Pin Count (HPC) FMC mezzanine board.

4.1 Key Features

For the implementation of EV12AQ600/605 ADC, the EV12AQ600-FMC-EVM includes the following key features:

- x4 single-ended signal inputs transformed into differential signals through broadband baluns (BAL-0006SMG) allowing a single-ended signal source from 500 kHz to 6 GHz.
- ADC selectable high-speed clock input from the LMX2592 clock synthesizer or from a single-ended clock input transformed into differential signal through a broadband balun (BAL-0208SMG) to test the ADC performance with an external low-noise clock source
- Single-ended clock reference input for the LMX2592 clock synthesizer to synchronize multiple EV12AQ600-FMC-EVM boards.
- SYNCTRIG selectable input from the HPC FMC connector or from differential SMA connectors.
- SYNCO selectable output to the HPC FMC connector or to differential SMA connectors.
- Temperature diode monitoring (AD7708 + LM334) with SPI interface over the FMC connector interface.
- x8 High-Speed Speed Lanes (HSSL) to receive ADC samples using ESIstream protocol (see ESIstream protocol specifications).
- Debug user interface, GPIO x9, dip switches x4 and leds x4 over HPC FMC connector interface.
- 1.8V control signals HPC FMC connector interface.

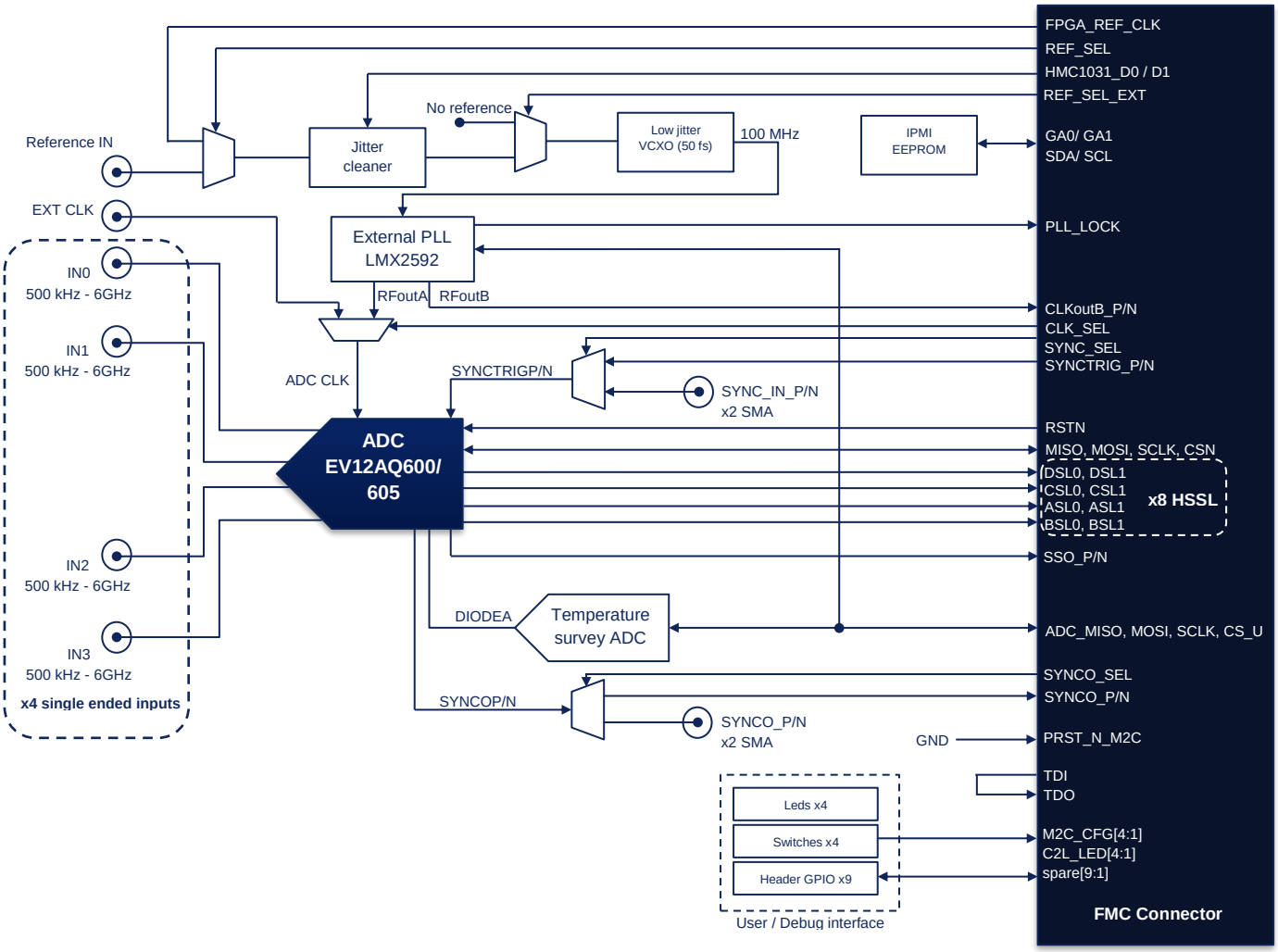


Figure 2 – EV12AQ600-FMC-EVM architecture overview.

4.2 EV12AQ600 top and bottom views

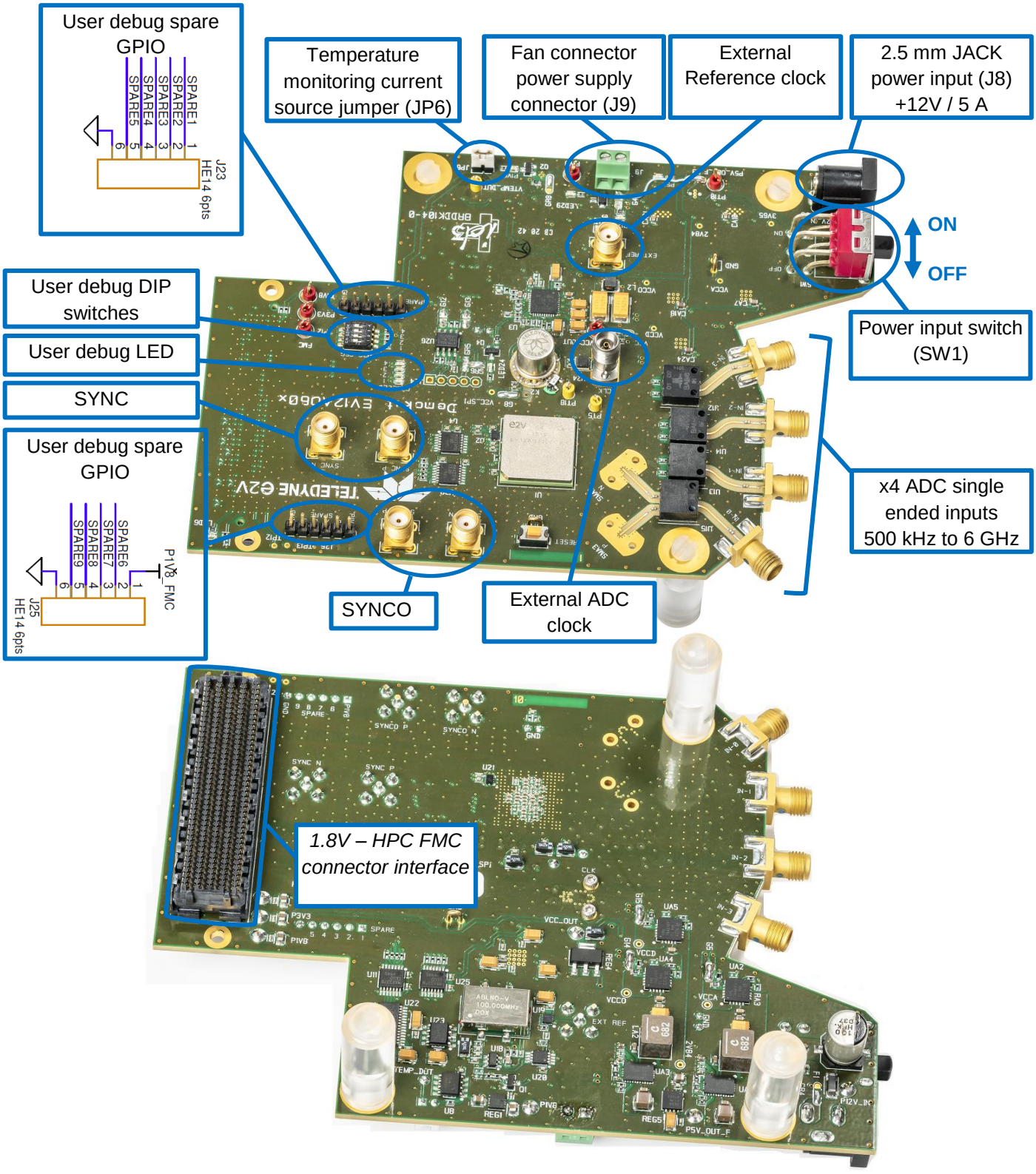


Figure 3 – EV12AQ600-FMC-EVM top and bottom view.

4.3 FMC connector

4.3.1 FMC signals description

Pin name	Pin reference	Signal name	M2C/C2M (1)	Signal Description
CLK0_M2C_P	H4	-	-	Not used
CLK0_M2C_N	H5	-	-	Not used
LA00_P_CC	G6	FPGA_REF_CLK	C2M	Optional 10 MHz clock reference for the PLL LMX2592. REF_SEL must be high (1.8V) to use this reference.
LA00_N_CC	G7	-	-	Not used
LA01_P_CC	D8	ADC_SCLK	C2M	SPI SCLK signal both for LMX2592 clock synthesizer and Diode temperature monitoring ADC (AD7708 Channel 1).
LA01_N_CC	D9	-	-	Not used
LA02_P	H7	-	-	Not used
LA02_N	H8	-	-	Not used
LA03_P	G9	REF_SEL_EXT	C2M	0 (0 V): Select VCC/2 for low jitter VCXO 100 MHz (ABLNO-V-100.000MHZ) Voltage Control (VC) input. No external clock reference. 1 (1.8 V): Select CP output of HMC1031 for low jitter VCXO 100 MHz (ABLNO-V-100.000MHZ) Voltage Control (VC) input. External clock reference. 2-channel analog multiplexer 74LVC1G3157 S-input.
LA03_N	G10	REF_SEL	C2M	0 (0 V): External clock reference to be connected on SMA12 (10 MHz). 1 (1.8 V): External clock reference from the carrier board using C2M FPGA_REF_CLK FMC connector input. SP3T RF switch JSW3-272DR+ RF1-input
LA04_P	H10	SYNCTRIG_P-DUT	C2M	EV12AQ600/605 ADC SYNCTRIG input when SYNC_SEL is low (0 V).
LA04_N	H11	SYNCTRIG_N-DUT	C2M	
LA05_P	D11	HMC1031_D1	C2M	HMC1031: 0.1 MHz to 500 MHz Clock Generator with Integer N PLL Phase lock clean high frequency references to 10 MHz equipment.
LA05_N	D12	HMC1031_D0	C2M	D0 / D1 / Reference clock frequency / PLL Feedback division ratio 0 / 0 / N.A. / Power-down 1 / 0 / 100 MHz / Divide by 1 0 / 1 / 20 MHz / Divide by 5 1 / 1 / 10 MHz / Divide by 10
LA06_P	C10	spare[7]	TBD	User Debug GPIO / spare signal
LA06_N	C11	MISO	C2M	EV12AQ600/605 ADC SPI MISO.
LA07_P	H13	spare[4]	TBD	User Debug GPIO / spare signal
LA07_N	H14	spare[3]	TBD	User Debug GPIO / spare signal
LA08_P	G12	CLK_SEL	C2M	EV12AQ600/605 ADC CLK source switch 0 (0 V): External SMA 1 (1.8 V): LMX2592 Clock synthesizer
LA08_N	G13	SYNCO_SEL	C2M	0 (0 V): EV12AQ600/605 SYNCO from FMC connector interface 1 (1.8 V): EV12AQ600/605 external SYNCO from SMA15/SMA16.
LA09_P	D14	spare[6]	TBD	User Debug GPIO / spare signal
LA09_N	D15	ADC_CS_U	C2M	SPI NCS signal for diode temperature monitoring ADC (AD7708 Channel 1).
LA10_P	C14	spare[8]	TBD	User Debug GPIO / spare signal FTDI UART 1 TXD (Orange) when using ESIstream VHDL design example.
LA10_N	C15	RSTN	C2M	EV12AQ600/605 ADC active low reset.
LA11_P	H16	CSN-PLL	C2M	SPI NCS signal for EV12AQ600/605 ADC CLK PLL (LMX2592).
LA11_N	H17	spare[1]	TBD	User Debug GPIO / spare signal
LA12_P	G15	SYNC_SEL	C2M	0 (0 V): SYNC C2M 1 (1.8 V): External SYNC from SMA13/SMA14 2-channel differential multiplexer CBTL01023 SEL-input.
LA12_N	G16	spare[2]	TBD	User Debug GPIO / spare signal

LA13_P	D17	ADC_MISO	C2M	SPI MISO signal both for LMX2592 clock synthesizer and Diode temperature monitoring ADC (AD7708 Channel 1).
LA13_N	D18	ADC_MOSI	M2C	SPI MOSI signal both for LMX2592 clock synthesizer and Diode temperature monitoring ADC (AD7708 Channel 1).
LA14_P	C18	SCLK	OUT	EV12AQ600/605 ADC SPI SCLK.
LA14_N	C19	Spare[9]	TBD	User Debug GPIO / spare signal FTDI UART 1 RXD (yellow) when using ESIstream VHDL design example.
LA15_P	H19	C2M_LED1	OUT	Debug user led 1 (LED15)
LA15_N	H20	C2M_LED2	OUT	Debug user led 2 (LED16)
LA16_P	g18	PLL_MUXOUT	IN	LMX2592 clock synthesizer PLL locked when high (1.8V)
LA16_N	G19	Spare[5]	TBD	User Debug GPIO / spare signal
CLK1_M2C_P	G2	-	-	Not used
CLK1_M2C_N	G3	-	-	Not used
LA17_P_CC	D20	CLKoutB_P	M2C	LMX2592 RFoutB P
LA17_N_CC	D21	CLKoutB_N	M2C	LMX2592 RFoutB N
LA18_P_CC	C22	-	-	Not used
LA18_N_CC	C23	-	-	Not used
LA19_P	H22	C2M_LED3	C2M	Debug user led 3 (LED17)
LA19_N	H23	C2M_LED4	C2M	Debug user led 4 (LED31)
LA20_P	G21	CSN	C2M	EV12AQ600 ADC SPI NCS
LA20_N	G22	MOSI	C2M	EV12AQ600 ADC SPI MOSI
LA21_P	H25	-	-	Not used
LA21_N	H26	-	-	Not used
LA22_P	G24	M2C_CFG1	M2C	Debug user SW3.1 switch
LA22_N	G25	M2C_CFG2	M2C	Debug user SW3.2 switch
LA23_P	D23	-	-	Not used
LA23_N	D24	-	-	Not used
LA24_P	H28	-	-	Not used
LA24_N	H29	-	-	Not used
LA25_P	G27	M2C_CFG3	M2C	Debug user SW3.3 switch
LA25_N	G28	M2C_CFG4	M2C	Debug user SW3.4 switch
LA26_P	D26	-	-	Not used
LA26_N	D27	-	-	Not used
LA27_P	C26	-	-	Not used
LA27_N	C27	-	-	Not used
LA28_P	H31	SYNCO_P	M2C	EV12AQ600/605 ADC SYNCO output when SYNCO-SEL is low (0 V).
LA28_N	H32	SYNCO_N	M2C	
LA29_P	G30	-	-	Not used
LA29_N	G31	-	-	Not used
LA30_P	H34	-	-	Not used
LA30_N	H35	-	-	Not used
LA31_P	G33	-	-	Not used
LA31_N	G34	-	-	Not used
LA32_P	H37	-	-	Not used
LA32_N	H38	-	-	Not used
LA33_P	G36	-	-	Not used
LA33_N	G37	-	-	Not used

DP0_M2C_P	C6	P_BSL0		EV12AQ600/605 channel B output P, serial link0 (CML)
DP0_M2C_N	C7	N_BSL0		EV12AQ600/605 channel B output N, serial link0 (CML)
DP1_M2C_P	A2	P_BSL1		EV12AQ600/605 channel B output P, serial link1 (CML)
DP1_M2C_N	A3	N_BSL1		EV12AQ600/605 channel B output N, serial link1 (CML)
DP2_M2C_P	A6	P_ASL0		EV12AQ600/605 channel A output P, serial link0 (CML)
DP2_M2C_N	A7	N_ASL0		EV12AQ600/605 channel A output N, serial link0 (CML)
DP3_M2C_P	A10	P_ASL1		EV12AQ600/605 channel A output P, serial link1 (CML)
DP3_M2C_N	A11	N_ASL1		EV12AQ600/605 channel A output N, serial link1 (CML)
DP4_M2C_P	A14	P_DSL0		EV12AQ600/605 channel D output P, serial link0 (CML)
DP4_M2C_N	A15	N_DSL0		EV12AQ600/605 channel D output N, serial link0 (CML)
DP5_M2C_P	A18	P_CSL1		EV12AQ600/605 channel C output P, serial link1 (CML)
DP5_M2C_N	A19	N_CSL1		EV12AQ600/605 channel C output N, serial link1 (CML)
DP6_M2C_P	B16	P_CSL0		EV12AQ600/605 channel C output P, serial link0 (CML)
DP6_M2C_N	B17	N_CSL0		EV12AQ600/605 channel C output N, serial link0 (CML)
DP7_M2C_P	B12	P_DSL1		EV12AQ600/605 channel D output P, serial link1 (CML)
DP7_M2C_N	B13	N_DSL1		EV12AQ600/605 channel D output N, serial link1 (CML)
GBTCLK0_M2C_P	D4	SSO_P		Slow Synchro Output P. $f_{sso} = f_{ADC\_CLK}/32$. To be used as transceiver clock reference by the logic device receiving ADC samples.
GBTCLK0_M2C_N	D5	SSO_N		Slow Synchro Output N. $f_{sso} = f_{ADC\_CLK}/32$. To be used as transceiver clock reference by the logic device receiving ADC samples.

Notes:

(1) M2C : Mezzanine to Carrier signal
C2M: Carrier to Mezzanine signal

4.3.2 FMC pinout

	K	J	H	G	F	E	D	C	B	A
1	TP13 - VREF_B_M2C	GND	TP12 - VREF_A_M2C	GND	P3V3 - PG_M2C	GND	LED6 - PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	GND - PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	P_BSL1 - DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	N_BSL1 - DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	SSO_P - GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	SSO_N - GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	FPGA_REF_CLK - LA00_P_CC	GND	HA05_P	GND	P_BSL0 - DP0_M2C_P	GND	P_ASL0 - DP2_M2C_P
7	HA02_P	HA03_N	SYNCO_P - LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	N_BSL0 - DP0_M2C_N	GND	N_ASL0 - DP2_M2C_N
8	HA02_N	GND	SYNCO_N - LA02_N	GND	HA04_N	GND	ADC_SCLK - LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	REF_SEL_EXT - LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	SYNCTRIG_P - LA04_P	REF_SEL - LA03_N	HA08_P	HA09_N	GND	J23.1 Header - LA06_P	GND	P_ASL1 - DP3_M2C_P
11	HA06_N	GND	SYNCTRIG_P - LA04_N	GND	HA08_N	GND	HMC1031_D1 - LA05_P	MISO - LA06_N	GND	N_ASL1 - DP3_M2C_N
12	GND	HA11_P	GND	CLK_SEL - LA08_P	GND	HA13_P	HMC1031_D0 - LA05_N	GND	P_DSL1 - DP7_M2C_P	GND
13	HA10_P	HA11_N	J23.2 Header - LA07_P	SYNCO_SEL - LA08_N	HA12_P	HA13_N	GND	GND	N_DSL1 - DP7_M2C_N	GND
14	HA10_N	GND	J23.3 Header - LA07_N	GND	HA12_N	GND	J23.4 Header - LA09_P	J23.5 Header - LA10_P	GND	P_DSL0 - DP4_M2C_P
15	GND	HA14_P	GND	SYNC_SEL - LA12_P	GND	HA16_P	ADC_CS_U - LA09_N	RSTN - LA10_N	GND	N_DSL0 - DP4_M2C_N
16	HA17_P_CC	HA14_N	CSN-PLL - LA11_P	J25.3 Header - LA12_N	HA15_P	HA16_N	GND	GND	P_CSL0 - DP6_M2C_P	GND
17	HA17_N_CC	GND	J25.2 Header - LA11_N	GND	HA15_N	GND	ADC_MISO - LA13_P	GND	N_CSL0 - DP6_M2C_N	GND
18	GND	HA18_P	GND	PLL_LOCK - LA16_P	GND	HA20_P	ADC_MOSI - LA13_N	SCLK - LA14_P	GND	P_CSL1 - DP5_M2C_P
19	HA21_P	HA18_N	C2M_LED1 - LA15_P	J25.5 Header - LA16_N	HA19_P	HA20_N	GND	J25.4 Header - LA14_N	GND	N_CSL1 - DP5_M2C_N
20	HA21_N	GND	C2M_LED2 - LA15_N	GND	HA19_N	GND	CLKoutB_P - LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	CSN - LA20_P	GND	HB03_P	CLKoutB_N - LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	C2M_LED3 - LA19_P	MOSI - LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	C2M_LED4 - LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	M2C_CFG1 - LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	M2C_CFG2 - LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	M2C_CFG3 - LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	M2C_CFG4 - LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	P1V8 - VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	P1V8 - VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

LA31_P
LA31_N

Grey cells means “not connected” on EV12AQ600-FMC-EVM board

5 Power supplies

- FMC connector interface 12P0V not used on EV12AQ600-FMC-EVM board. Connected to PT15 test point.
- FMC connector interface 3P3V not used on EV12AQ600-FMC-EVM board. Connected to PT16 test point.
- FMC connector interface VADJ not used on EV12AQ600-FMC-EVM board. Connected to PT17 test point.
- FMC connector interface 3P3VAUX used to supply the IPMI EEPROM (U26).
- All EV12AQ600-FMC-EVM board is supplied by the 2.5 mm JACK connector (J8) +12 V / 5 A input.