EV12AD5x0x-EK

## VITA 57 FMC DUAL 12b ADC Evaluation kit

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The EV12AD5x0x Eval Kit enables the easy evaluation of the characteristics and performance of DUAL 12-bit ADC EV12AD5x0x.

The Eval Kit is delivered with a software allowing acquisition of data with the FPGA. The EV12AD5x0x Eval Kit is compatible with VITA 57 FMC (FPGA Mezzanine Card) standard. For more information please see the VITA web site: <u>http://www.vita.com/fmc.html</u> The DUAL 12-bit ADC Eval Kit is compatible with Virtex-7 FPGA VC709 Connectivity Kit (not provided). Please see <u>Section 5 "FPGA CODE"</u>. The FPGA VHDL data acquisition code for VC709 board is supplied.

### 1.1 Disclaimer

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This kit must be regarded as a tool, not a finished product. It allows the evaluation of performance of the Teledyne e2v component, design prototypes and debug software. It CANNOT be resold as a finished product that must be compliant with local relevant regulations.

Its function is as a development system, demonstrating the performance of Teledyne e2v semiconductors components and not as a final product available on general release.

Since this Development Kit is intended to be used on an industrial workbench and modified by the user to build his prototypes, NO WARRANTY OF ANY KIND can apply.

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### 1.2 EV12AD5x0x

The EV12AD5x0x-EK Eval Kit is based on Teledyne e2v EV12AD5x0x Dual 12-bit 1.5Gsps ADC for which block diagrams are given below.

EV12AD550x is a dual 12 bit 1.5GS/s ADC featuring a built in selectable 1:2-1:1 DEMUX, and LVDS parallel outputs (see Figure 1-1 and Figure 1-2 below). For EV12AD550x refer to <u>http://www.e2v.com/products/semiconductors/adc/ev12ad550/</u>.

EV12AD500x is a dual 12 bit 1.5GS/s ADC featuring selectable serial output on 4 (or 2) lanes per ADC core or a selectable parallel output LVDS in 1:1 mode (see Figure 1-3 below). For EV12AD550x refer to <u>http://www.e2v.com/products/semiconductors/adc/ev12ad500/</u>.

The two ADC cores can operate in phase or in opposition (option controlled through the SPI) to interleave the two cores. External clock must be provided at twice the individual sampling rate.

The innovative architecture allows for high sampling rate (up to 1.5GS/s) without interleaving thus providing high level of spectral purity.

Tunings and functionalities are controlled through a Serial Peripheral Interface (SPI).



Figure 1-1. Simplified block diagram LVDS demux 1:2 configuration EV12AD550x

The block diagram above (Figure 1.1) refers to DEMUX 1:2 mode for output buffer affectation.

- Data Ready
- 12 bit of Data on high and low port
- In Range, Parity or Trigger, selected through SPI command, output
  - On AFU1 for A high port
  - On AFU2 for A low port

- On BFU1 for B high port
- On BFU2 for B low port



Figure 1-2. Simplified block diagram LVDS demux 1:1 configuration EV12AD5x0x

The block diagram above (Figure 1.2) refers to DEMUX 1:1 mode for output buffer affectation.

- Data Ready
- bit of Data on high port
- In Range, Parity or Trigger, selected through SPI command, output
  - on AFU1/AFU2 for A high port
  - on BFU1/BFU2 for B high port.

Figure 1-3. Simplified block diagram serial link or LVDS demux 1:1 configuration EV12AD500x



Depending on SPI code, the LVDS mode or serial mode is activated. Both interfaces cannot be enabled simultaneously.

## 1.3 Eval Kit

The user has 2 choices to connect the EV12AD5x0x board:

- with VC709 Virtex 7 evaluation board from Xilinx (not provided)
- with Data interface board

Figure 1-4. Eval Kit EV12AD5x0x-EK System with VC709



The complete system is built with the Teledyne e2v Eval Kit and the VC709 evaluation board from. Teledyne e2v Eval Kit contains the following items:

- DUAL 12-bit ADC Eval Kit with EV12AD5x0x ADC
- Cables & Power Supply
  - Universal 12V power adapter & cables
  - USB Cables to communicate with a PC (control of ADC settings and settings for data acquisition)
- USB key or CD ROM with GUI Software, VC709 FPGA software
- Data Interface Board

#### **General Overview**

Note: The Virtex 7 FPGA VC709 with XC7VX690T-2FFG1761C FPGA is not supplied within the Teledyne e2v kit and should be purchased separately from Xilinx or its authorized distributors.

Acquisition and formatting of ADC digital output data are done within the FPGA.

Data is then transmitted again to the ADC Eval Kit.

A USB driver on the ADC Eval Kit allows data transmission to the computer that performs the display and processing of ADC output data (FFT).

Software and graphical User Interface are provided with the Eval Kit.

The provided software operates using Labview Run Time (no license required).

## 1.4 External equipment

The EV12AD5x0x Eval Kit needs very little external hardware.

RF generator for clock input:

- The EV12AD5x0x can sample signals up to 1.5Gsps.
- For optimum performance this generator must have a low phase noise. Please see Table 1-1. "Example of RF Generators" below.
- Balun should be used to provide a differential input.

RF generator for analog input signal:

- The EV12AD5x0x has a bandwidth up to 5300MHz.
- For optimum performance this generator must have a low phase noise. Please see Table 1-1. "Example of RF Generators" below.
- Filter should be used to remove input generator harmonics and balun should be used to provide a differential input.

Cables & Power Supply (provided by Teledyne e2v):

- Universal 12V power Adapter & Cables.
- USB Cable to communicate with a PC (control of ADC settings and acquisition settings).

Note: The Eval Kit allows external control of power supplies (Cables not provided). See Section 3.7.

PC with windows:

Windows XP or Windows 7 (32 and 64bit). Please see <u>Section 4.2. "Configuration"</u>.

FPGA evaluation board is compatible with VITA57 FMC Standard:

- This Eval Kit board has been especially designed to be connected to the Xilinx Virtex-7 evaluation board VC709.
- The EV12AD5x0x Eval Kit could be used with other FPGA evaluation boards compatible with VITA57 FMC Standard. However, an assessment of connections should be done prior to connecting the FPGA board in order to ensure full compatibility.
- FPGA code to interface with GUI is provided only for VC709.

#### Table 1-1. Example of RF sources

Signal generator	SSB phase noise @1GHz (20 KHz offset)
Agilent E4424B 250KHz 2GHz (High spectral purity)	<-134dBc/Hz
Agilent E4426B 250KHz 4GHz (High spectral purity)	<-134dBc/Hz
SMA100A 9 KHz 6GHz (High spectral purity)	< -140dBc/Hz
PLL LTC6946-3	< -140dBc/Hz (1MHz Offset)
PLL STW81200	< -156dBc/Hz (1MHz Offset)

# Section 2. QUICK START

#### 2.1 Basic configuration of the board

The board is delivered in the following configuration.

#### Jumpers

- JP1 JP9 JP10 JP6 JP7 and JP8 are set to "LDO" so that internal supply is provided to the ADC. See <u>Section 3.7</u> for details.
- JP3 JP4 JP5 are connected
- JP2 is set on EXT
- JP17 is connected
- JP11 is connected so that 100µA current source is ON for diode voltage measurement. See <u>Section 3.5</u> for details.

#### **Red Switches**

- S3 is set on FLASH
- S4 is on µC
- S5 is set on μC
- S6 is set on FPGA
- S10 is set on ADC

**Black Switches** 

- All tips of S8 are OFF
- For AD550, all tips of S9 are OFF
- For AD500, all tips of S9 are ON except S9-1 that is ON

### 2.2 Operating procedure

In the following procedures, supply of ADC is provided by the board LDO and diode current is provided by the internal current source (100 $\mu$ A). In this configuration, ADC consumption currents cannot be monitored.

To modify this initial setup, please refer to <u>Section 3.5</u> and <u>Section 3.7</u>.

# To insure a proper start of the Eval Kit, the chronological order as described below should be respected.

#### 2.2.1 Using VC709

- 1. Install the software as described in section 4 Software Tools.
- 2. Load the FPGA program (see <u>Section 5 « FPGA Code»</u>).
- 3. Check that the Heatsink/Fan is properly fixed to the ADC board.
- 4. Connect the EV12AD5x0x Eval Kit to VC709 Xilinx evaluation board.
- 5. Connect the power supplies of EV12AD5x0x Eval Kit and FPGA board.
- 6. Connect the USB cable to connector J20 on EV12AD5x0x board.
- 7. Connect a RF generator on clock input and preset clock frequency and level (make sure the losses of baluns and filters are taken into account when applying clock level)
- 8. Turn ON power supply of EV12AD5x0x Eval Kit.
- 9. Turn ON power supply of VC709 Xilinx Evaluation Board.
- 10. Turn ON clock generator.
- 11. Push once on S7  $\mu C\_reset~and$  S1 RSTN-DUT buttons
- 12. Launch the EV12AD5x0x.exe software.
- 13. On the software,
  - o Click on reset then SYNC buttons to initialize ADC (see <u>Section 4</u> for details)
  - $\circ$  ~ Turn the mode ADC test ramp active.
  - o Launch acquisition
- 14. Check if the acquisition is correct

At this stage main connections are validated.

To perform an acquisition, starting from previous stage:

- 15. Return to normal mode (Turn OFF Test mode).
- 16. Connect a RF generator on analog input and preset input signal frequency and level
- 17. Configure the ADC on the software (Parallel or serial mode, calibration loaded or not...). A SYNC may be necessary.
- 18. Turn ON the RF generator.
- 19. Set signal frequency and clock frequency in "Acquisition" tab (see Section 4.9 for details)
- 20. Launch acquisition.

#### 2.2.2 Using Data Interface Board

#### If data interface board is used, switch S6 should be set on EXT.

- 1. Install the software as described in section 4 Software Tools.
- 2. Check that the Heatsink/Fan is properly fixed to the ADC board.
- 3. Connect the EV12AD5x0x Eval Kit to Data Interface Board.
- 4. Connect the power supplies of EV12AD5x0x Eval Kit.
- 5. Connect the USB cable to connector J20 on EV12AD5x0x board.
- 6. Connect a RF generator on Clock input and preset clock frequency and level (make sure the losses of baluns and filters are taken into account when applying clock level)
- 7. Turn ON power supply of EV12AD5x0x Eval Kit.
- 8. Turn ON clock generator.
- 9. Push once on S7  $\mu C\_reset~$  and S1 RSTN-DUT buttons
- 10. Launch the EV12AD5x0x.exe software.
- 11. On the software,
  - o Click on reset then SYNC buttons to initialize ADC (see Section 4 for details)
  - Turn the mode ADC test ramp active.
  - Launch acquisition
- 12. Check if the acquisition is correct

At this stage main connections are validated.

To perform an acquisition, starting from previous stage:

- 13. Return to normal mode (Turn OFF Test mode).
- 14. Connect a RF generator on Analog input and preset input signal frequency and level
- 15. Configure the ADC on the software (Parallel or serial mode, calibration loaded or not...). A SYNC may be necessary.
- 16. Turn ON the RF generator.
- 17. Launch acquisition.

## 2.3 Troubleshooting

#### 2.3.1 Installation

Check that you own rights to write in the directory (administrator rights). Check for the available disk space.

Check that the USB port is free and properly configured. It should appear in the device manager as shown below.



#### 2.3.2 Start-up procedure

Verify that the board is properly configured as described in <u>Section 2.1</u>.

Check that boards are properly supplied.

Check if the Xilinx FPGA evaluation board VC709 is properly configured with correct software. If LED4 on VC 709 is blinking regularly then the FPGA program has been correctly loaded. Check if EV12AD5x0x Eval Kit is properly plugged into FPGA connector and its LED3 is ON. It detects the presence of the VC709 board. See Figure 2-1 below.

Check if USB connector is properly plugged on J20.

Figure 2-1. LED3 that indicates VC709 board connection



Figure 2-2. Software output if no FPGA board detected

Initialization Sequence	Status INITIALIZATION TERMINATED with WARNINGs	μC ID
🥪 μC Open COM		Serial Number
A Check EPGA	Initialization Progress	LOG4Z077
T CHECK FPOA		Version & Revision
	Initialization messages	19 1261
		CRC
		×6816
😤 Restart		FPGA PLLs TD Version ×0000 ×0000

Figure 2-3. Software output if no microcontroller detected

ADC Settings Calibration	Acquisition (via FPGA)	EV12AD550	Td 527.5	SYNC SYNC
Initialization Sequence	Status ERROR(s) OO	CURED DURING INITIALIZATION	μC ID	
💥 µС Open COM			Serial Number	
	Initialization Progress		LOG4Z077	
			Version & Revisio	n
	1-141-11-41-		19 1261	
	Initialization messages		CRC	
			×6816	
💈 Restart			FPGA	FPGA PLLs
			ID Version	Core A Core B
			×0001 × D100	A KA
			~0001 × D100	UNLOCKED UNLOCK

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### 2.3.3 Measurements

Check if EV12AD5x0x is properly configured in normal mode.

- Check if test mode is OFF.
- Check if acquisition mode is correctly configured.

In case of doubt, click on RESET and re-configure ADC.

If no windowing is used and signal is not coherent, reconstructed signal of Figure 2-4 is obtained. *Figure 2-4.* Reconstructed signal without windowing and not coherent signal







Check that the junction temperature of EV12AD5x0x is lower than 110°C and that heatsink is properly connected.

Check EV12AD5x0x board connection to FPGA or data interface board.

Verify that board is properly configured as described in <u>Section 2.1</u>.

Check if all RF cables are properly connected to CLK and inputs of EV12AD5x0x board.

Make sure applied levels of clock and input signals are high enough taking into account the losses of filters and baluns.

# Section 3. Main Functions

## 3.1 VC709 board or Data Interface board

Our EK can be connected either to the Data Interface Board or VC709 board.



Figure 3-1. Data Interface Board



Figure 3-2. VC709 Board

To change configuration, make sure that all the evaluation boards are turned off and then disconnect the boards.

## 3.2 Analog input signal

The user needs to provide an analog signal at the input. This signal is digitized by the ADC. It is mandatory to drive the ADC by a differential input signal.

Figure 3-3. Analog input schematics



Analog inputs A or B can be used in DC configuration mode by replacing C1, C2 and C5, C6 by a  $0\Omega$  resistor.

## 3.3 ADC Clock input signal

The user needs to provide a differential analog clock.

Figure 3-4. Clock input schematics



## 3.4 Control of ADC settings

The Graphical User Interface allows complete monitoring and control of all the settings of EV12AD5x0x such as Gain, Offset, Phase and Test Mode. Please see <u>Section 4.5 Operating Modes</u> and refer to datasheet EV12AD5x0x for more information.

### 3.5 ADC Junction Temperature Monitoring

ADC junction temperature can be monitored by temperature sensor from component U2 (LM334). The configuration is done for  $100\mu$ A; it can be changed via R1. By default, this  $100\mu$ A current source is used as JP11 is plugged on board.

Figure 3-5. Junction temperature monitoring



ADC junction temperature can be displayed on the PC via the GUI. The Eval Kit provides an external heat sink with internal fan. The use of the internal current source is not mandatory. The user can monitor Vdiode through a multimeter plugged on J1 and J2 connectors. Then the user must take 2 precautions:

- disconnect J11
- check which current is delivered by the multimeter and modify the temperature coefficients (See Section 4.5.2 and Figure 4-18)

## 3.6 SYNC

The EV12AD5x0x requires a SYNC signal when the internal configuration is changed.

#### 3.6.1 Nominal case

If the board is in the initial configuration as described in <u>Section 2.1</u> then:

- When VC709 is connected (<u>\$2.2.1</u>), SYNC is done by the FPGA
- When Data Interface Board is connected ( $\frac{22.2.2}{2}$ ), SYNC is done by the  $\mu$ C.

#### 3.6.2 Advanced case

The user has other possibilities to do a SYNC.

#### 3.6.2.1 SYNC done by SYNC TRIG on ADC board

In this case, SMA13 is used to input the SYNC signal. Switch S5 must be set on SMA. Refer to the datasheet to identify the input pulse signal to be applied.

#### *Figure 3-6.* Switch S5; SMA13 on board



#### 3.6.2.2 SYNC done by SYNC TRIG on Data Interface Board

In this case, SMA2 and SMA4 of the Data Interface Board are used to input the SYNC signal. Switch S6 must be set on EXT.

Refer to the datasheet to identify the input pulse signal to be applied.

Figure 3-7. Switch S6 on ADC board; SMA2 and SMA4 on Data interface board



## 3.7 DC/DC converter

The user has the possibility to use on-board LDO or external power supply. The 12V jack must be connected whatever external or internal supply option is selected.

#### 3.7.1 To use on-board LDO

- 1. Connect the 12V Jack
- 2. Put the jumpers on LDO label (JP1, JP9, JP10, JP6, JP7, JP8)



3. Switch on SW1



4. All the LEDs (LED1, LED2, LED4, LED5 and LED6) must be lighted on.

If the user chooses the solution with the 12V jack, the user can monitor the power supply of VCCD and VCCIOx1 between 2.5V and 3.4V thanks to R40.





Figure 3-9. 2.5V or 3.4V on evaluation board



#### 3.7.2 To use external power supplies

- 1. Connect the 12V Jack
- 2. Put the jumpers on EXT label (JP1, JP9, JP10, JP6, JP7, JP8)



3. Connect the external supplies to the board



- 4. Switch on SW1
- 5. Switch on external supplies
- 6. All the LEDS (LED1, LED2, LED4, LED5 and LED6) must be lighted on.

Note that the chronological order in which power supplies are set ON has no effect on the ADC behavior.

## 3.8 SSO signal

SSO signal can be provided via the ADC or through the two SMA connectors: SSO\_N-EXT and SSO\_P-EXT.

The selection is done manually with a switch S10.

Figure 3-10. SSO schematics







Refer to the datasheet to get details on SSO function.

## 3.9 Fan power supply

The fan can be powered through the 12V jack of the evaluation board. To do so, the fan cables must be connected to the [J24 fan] as shown on figure below. JP17 must be removed.





# Section 4. Software Tools

## 4.1 Overview

The Eval Kit board needs three different kinds of software tools:

• FPGA Software (do not consider this point if you use Data Interface board)

The Eval Kit board can be plugged with XILINX VIRTEX 7 evaluation board EK-V6-VC709-G (<u>http://www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html</u>).

Teledyne e2v provides FPGA program to be used with EV12AD5x0x Eval Kit.

User Interface Software

The User Interface software is a Labview compiled graphical interface that does not require a license to run on Window 7/XP.

The software uses intuitive push-buttons and pop-up menus to configure the ADC and recover the ADC samples.

Revision 1.0.1 is the GUI version for EV12AD5x0A.

Revision 1.2.5 is the GUI version for EV12AD5x0B.

## 4.2 Configuration

The advised configuration for Windows 7 is:

- PC with core i3 or equivalent
- Memory of at least 1GB
- Office 2010 (for data recovering)

Note: The GUI is not compatible with Office 2003

## 4.3 User interface installation

Install the DUAL ADC Eval Kit application on your computer by launching the install.exe (please make sur proper GUI version is installed: 1.0.1 for EV12AD5x0A, 1.2.5 for EV12AD5x0B).

Installation is intuitive. Simplified guide with main steps follows. Others windows than the ones described below can pop-up. Then clicking on "Next" should be done.

• On first window, select the applications you want to install.

#### Figure 4-1. Selection

Choose Components Choose which features of E2V	EV12AD5x0 Software (v0.6.4) you want to install.	ezv
Check the components you wai install. Click Install to start the	nt to install and uncheck the components you don't wa installation.	nt to
Select components to install:	NI-Drivers     NI-LabVIEW RunTime Engine     NI-VISA RunTime Engine     STI32 - USB drivers     G4bits     SIL SUBSERS	4 III >
Space required: 0.0KB	Position Position your mouse over a component to see its description.	
Nullcoft Inctall System v2:46		

• On each following window that pops up, click on "Next".

Figure 4-2. Labview installation start

Moteur	d'exécution de NI LabVIEW 2010 SP1	
	Moteur d'exécution de NI LabVIEW 2010	) SP1
1	LabVIEW 2010	
	Service Pack 1	
	Quittez tous les programmes avant d'exécuter cet installeur. La désactivation des anti-virus peut améliorer la vitesse c'installation. De programme est suiet aux contrats de licence civinits.	
	National Instruments Corporation est un distributeur agréé de Microso	oft Silverlight.
	© 2010 National Instruments. Tous droits réservés.	<b>MATIONAL</b> INSTRUMENTS
		10

• On page shown on Figure 4-3, please uncheck the box.

Figure 4-3. Labview notifications

B Moteur d'exécution de NI LabVIEW 2010 SP1	
Notifications concernant les produits Veuillez lire les informations suivantes concernant la confi sélectionnée.	guration MATIONAL INSTRUMENTS
Demander à l'installeur de contacter National Instruments pour les mises à jour relatives aux produits National Instruments à in acceptez que votre adresse IP soit envoyée et recueillie confo de National Instruments.	rechercher les nouvelles notifications et staller. En cochant cette option, vous rmément à la politique de confidentialité
	Politique de confidentialité
	cédent Suivant >> Annuler

Please accept the licenses when suggested. See Figure 4-4.

#### Figure 4-4. Licenses

Contrat de licence		T NATIONAL
continuer.	ence ci-dessous pour pouvoi	MINSTROMENTS
CONTRAT DE LICENCE LOC	GICIEL NATIONAL	
GUIDE D'INSTALLATION : LE PRÉSENT DOC	CUMENT EST UN CONTR	AT. AVANT DE
VEUILLEZ LIRE ATTENTIVEMENT LE PRÉSE	ENT CONTRAT. EN TÉLÉ	CHARGEANT LE LOGICIEL
ET/OU CLIQUANT SUR LE BOUTON PERME	TTANT DE FINALISER LE	PROCESSUS
ACCEPTEZ D'ÊTRE LIÉ PAR CELUI-CI. SI VO	OUS NE VOULEZ PAS DE	VENIR PARTIE AU
PRESENT CONTRAT NI ETRE LIE PAR L'EN CLIQUER SUR LE BOUTON OUI ANNULE LE	SEMBLE DE SES DISPO E PROCESSUS D'INSTAL	SITIONS, VEUILLEZ
ET N'UTILISEZ PAS LE LOGICIEL, ET RETOU	JRNEZ CELUI-CI DANS L	ES TRENTE (30) JOURS
DE SA RECEPTION (ACCOMPAGNE DE TOU L'ACCOMPAGNENT, AINSI QUE DE LEURS E OBTENUE, TOUR LES DETOURS SEDONTS	EMBALLAGES) À L'ENDR	OIT OÙ VOUS LES AVEZ
Cette licence National Instruments s'applique au logi	ciel Moteur d'exécution de NI	LabVIEW 2010 SP1.
	J'accepte le co	ntrat de licence.
	🔘 Je n'accepte p	as le contrat de icence.

• The tool provides the list of applications which are already installed and those which are not. See Figure 4-5.

Just click on "Next".

Figure 4-5. List of applications

Démarrer l'installati	on	7 NATIONAL
Veuillez vérifier le rés	umé suivant avant de continuer.	INSTRUMEN
Impossible d'installer		
<ul> <li>DataSocket (version ultérieur</li> <li>USI (version ultérieure déjà in</li> </ul>	re déjà installée) nstallée)	
Ajout ou modification		
Moteur de variables NI     Licence pour le déploiement	d'applications LabVIEW 2010	
	L. P. LH.Y. Mr. LL.L.	
liquez sur le bouton Suivant pou installation.	r lancer l'installation. Cliquez sur le bouton	Précédent pour mod fier les options

• On NI window, please uncheck the box.

## Figure 4-6. NI product notifications

VI-VISA 5.4 Runtime	
Product Notifications Please read the following information about the configura selected.	ation you have
<ul> <li>Search for important messages and updates on the National I perform this search, your IP address will be collected in accor Privacy Policy.</li> <li>Note: You will be given the opportunity to select the</li> </ul>	Instruments products you are installing. To dance with the National Instruments <b>he updates you want to install.</b> <u>Privacy Policy</u>
	Back Next >> Cancel
	Dack Next>> Cancel

Installation of VSB driver proceeds the same way.

Figure 4-7. USB driver installation

CP210x USB to UART Bridge Dr	Welcome to the CP210x USB to UART Bridge Driver Installer This wizard will help you install the drivers for your CP210x USB to UART Bridge device.
	Cliquez sur Suivant pour continuer.

• Please accept licenses as done previously.

## Figure 4-8. USB driver license

iontrat de	licence
Ń	Vous devez accepter le contrat de licence pour continuer. Utilisez la barre de défilement ou appuyez sur la touche PG SUIV. pour afficher le reste du contrat.
	LICENSE AGREEMENT SILICON LABS VCP DRIVER IMPORTANT: READ CAREFULLY BEFORE AGREEING TO TERMS THIS PRODUCT CONTAINS THE SILICON LABS VCP DRIVER AND INSTALLER PROGRAMS AND OTHER THIRD PARTY SOFTWARE. TOGETHER THESE PRODUCTS ARE REFERRED TO AS THE "LICENSED SOFTWARE". USE OF THE LICENSED SOFTWARE IS SUBJECT TO THE TERMS OF THIS LICENSE AGREEMENT. DOWNLOADING THE LICENSED SOFTWARE AND INDICATING +
	J'accepte les termes de ce contrat     Imprimer     Je n'accepte pas les termes de ce contrat

• Select where you wish application to be registered (Default directory is recommended).

Figure 4-9. Destination directory

All software will be installed in the following locations. To install software into a different location, click the Browse button and select another directory. Directory for E2V - EV12AD5x0 C:\Program Files (x86)\E2V\EV12AD5x0\ Browse	All software will be installed in the following locations. To install software into a different location, click the Browse button and select another directory. Directory for E2V - EV12AD5x0 C:\Program Files (x86)\E2V\EV12AD5x0\ Browse	Destination Directory Select the primary installation o	dire atory.
Directory for E2V - EV12AD5x0 C:\Program Files (x86)\E2V\EV12AD5x0\ Browse	Directory for E2V - EV12AD5x0 C:\Program Files (x86)\E2V\EV12AD5x0\ Browse	All software will be installed in the different location, click the Brow	e following locations. To install software into a se button and select another directory.
C:\Program Files (x86)\E2V\EV12AD5x0\ Browse	C:\Program Files (x86)\E2V\EV12AD5x0\ Browse		
		Directory for E2V - EV12AD5xL	0
		Directory for E2V - EV12AD5x0 C:\Program Files (x86)\E2V\E	0 V12AD5x0\ Browse

• At the end, restart your computer.

## Figure 4-10. End of application

👷 E2V - EV	12AD5x0 Software (v0.6.4) Setup	X
?	Do you want to restart your comp	uter now ?
	Oui	Non

## 4.4 USB driver installation

After installation, EV12AD5x0x Eval Kit can be powered up and connected to a PC with USB cable. At the first connection a USB driver installation will be launched.

The installation is normally fully automatic. If it is not launched automatically, please install with CP210x VCPInstaller\_x64.exe or CP210x VCPInstaller\_x86.exe which are available on CD / USB key.

## 4.5 Operating modes

The EV12AD5x0x software included with the Eval Kit provides a Graphical User Interface to configure the ADC.

Push buttons, popup menus and capture windows allows easy:

- 1. ADC Settings
- 2. Interleaving Calibration
- 3. FPGA Post-Processing
- 4. Acquisition

After the SW is launched, first window is the "login page" as shown on Figure 4.11.

Once the initialization is terminated without errors, software and hardware revision of the microcontroller and the FPGA code appear on the right.

ADC Interleaving Settings	Acquisition (Via FPGA)	EV12AD500	Reset SYNC
Initialization Sequence ✓ Application initialization ✓ µC Open COM ✓ Read ADC configuration	Status INITIALIZ Initialization Progress	ATION TERMINATED without errors	pC ID Serial Number LOG42077
Check PPGA	Initialization messages		Version & Revision 19 1261 CRC ×6816
S Restart			FPGA FPGA PLLs D Version ×0001 × C110 FPGA PLLs Core A Co Locked Lo
	Load Fuses	perature 1 Temperature 2	

#### On AD5x0B (GUI 1.2.5)

Initialization Sequence	Status INITIALIZA	TION TERMINATED without errors	μC ID	
<ul> <li>μC Open COM</li> <li>Read ADC configuration</li> </ul>	Initialization Progress		Serial Number LOG4Z077	
🌱 Check FPGA			Version & Revis	ion
	Initialization messages		19 126: CRC	1
sestart			ID     Version       ×0001     ×D100	FPGA PLLs Core A Core Locked Lock
	Load Fuses	perature 1 Temperature 2		

On the bottom corner the software displays information about software, hardware revision and the component state:

- Date
- ADC ID
- ADC Serial
- ADC Date
- Fuse
- Fuse CRCs

#### Figure 4-12. Component state

28/10/2016 08:39:14 ADC ID ID × 0814 Serial × 0000 Date × 0000 Fuse 🥥 Fuse CRCs A 🔾 B 🔾

On the top of the window, there are 3 menus:

- 1. File
- 2. Device
- 3. Help

Figure 4-13. Header menu

ezy EZ	V - EV12	AD5x0	[0.7.3]
File	Device	Help	

#### 4.5.1 File

#### Figure 4-14. File menu

ve Context Ctrl+X	Acquisition (via FPGA)	550 Td 51.4 Refresh
Initialization Sequence	Status INITIALIZATION TERMINATED without	errors pC ID
<ul> <li>✓ µC Open COM</li> <li>✓ Read ADC configuration</li> <li>✓ Check FPGA</li> </ul>	Initialization Progress	Serial Number LOG4Z077
	Initialization messages	Version & Revision           19         1261           CRC         ×6816
Contract Restart		FPGA FPGA PLLs The Marine Core A Core

It is possible to save the context of the Eval Kit for later uses. Then it can be reloaded. <u>Settings and configurations of the ADC are saved (mode, calibrations ...) but the acquisition</u> <u>parameters filled in 'Acquisition sheet' are not saved.</u>

#### 4.5.2 Device

Select Menu:

This menu is very important as the choice impacts the visible features in the GUI. You have to correctly choose the device you want to measure: EV12AD500x or EV12AD550x.

Temperature V12AD500	ta FPGA	Td 52.0	Refresh
Initialization Sequence	Status	uC ID	
ψ μC Open COM		Serial Number	
V Read ADC configuration	Initialization Progress	LOG4Z077	
Y Check FPGA		Version & Revision	
		19 1261	
	Initialization messages	CRC	
		×6816	
🤣 Restart		FF FF	PGA PLLs
		HPGA	Core A Core
		ID Version	8 8
		× 0001 × D100	100

Note that device choice menu can be modified only when login page is selected. On any other page "device select" is disabled. By default, AD550x is selected.
- Temperature Menu:
- Figure 4-16. Device choice menu Temperature

Initialization Sequence	Status	uC ID
V μC Open COM V Read ADC configuration	Initialization Progress	Serial Number
Check FPGA		Version & Revision
	Initialization messages	19 1261
	Initianzation messages	CRC
		× 6816
Concentration Restart		
		FPGA FPLs
		FPGA Core A Core

Figure 4-17. Temperature coefficients for 1 mA temperature sensor

Slope (	mV/°C)
-1.	33
Zero Crossing	g Point (mV)
86	i9
Temperatur	e alarm (°C)
11(	0.0
<b>V</b>	- X
Validate	Cance

Slope	(mV/°C)
-1.5	5164
Zero Crossin	g Point (mV)
79	9.9
Temperatu	re alarm (°C)
11	0.0
~	<b>*</b>
×	<u></u>

*Figure 4-18.* Temperature coefficients for 100µA temperature sensor

Slope and Zero Crossing Point are indicated by Teledyne e2v in the datasheet (die junction temperature monitoring diode). Theses indications allow the GUI to give the diode temperature of the component.

Temperature alarm allows the user to indicate a temperature from which it will flash in red on the main screen.

### By default, values with 100µA are registered in the GUI.

Note that the coefficients given above are valid for AD5x0xA products and will be re-evaluated on second run.

Settings About	Acquisition (via FPGA)	EV12AD550	Td	50.7	SYNC  Refresh
Initialization Sequence	Status		_		
Application initialization	INITIALIZA	TION TERMINATED without errors	μCID		
Pead ADC configuration	I det e di a Danama		Serial Nu	mber	
Y Check FPGA			LOG4Z07	7	
			Version &	Revision	
	Initialization messages		19	1261	
			CRC		
			× 6816		
			FPGA ID	Version Co	ore A Core
			×0001	× D100	cked Lock
	Load Fuses				
	Temp	perature 1 Temperature 2			

By clicking on 'User Manual', the user guide will open. By clicking on 'About', our logo will appear.



### Figure 4-19. Help menu

### Software Tools

### 4.5.4 Fuses & Stored calibration

Two calibrations set are stored and fused in the device:

- Calibration 1 done at ambient temperature
- Calibration 2 done at hot temperature

Refer to datasheet to select the best calibration set versus temperature.

Figure 4-20. Component state bar when calibrations are fused



### Figure 4-21. Calibration set selection

2	3	
	Temperature 1	Temperature 2

The user needs to click on any of the calibration set to get it loaded in the device.

### 4.6 Control display

### Figure 4-22. Control display

<u>On AD5x0A (GUI 1.0.1)</u>		
File Device Help		
ADC Settings Calibration Acquisition (via FPGA)	EV12AD500	Td 48.9 SYNC Refresh C2V
File Device Help		
ADC Settings Calibration Kacquisition (via FPGA)	EV12AD550	Td 47.4 SYNC C
<u>On AD5x0B (GUI 1.2.5)</u>		
File Device Help		
ADC Settings Calibration (via FPGA)	EV12AD550	Td 52.0 Refresh

- Reset: A reset is sent to the ADC, the FPGA and the microcontroller.
- Refresh: Data on the active screens are refreshed.
- Td: The diode temperature is displayed in °C. This indicator may flash if the target temperature is reached.
- SYNC: A SYNC is sent to the ADC. On AD5x0B, the lamp closed to SYNC helps to validate either it has been taken into account or not.

### 4.7 ADC settings

### 4.7.1 ADC core



ADC Settings Calibration	Acquisition (via FPGA)	EV12AD500 Td 47.4	SYNC Refresh
ADC core Parallel output			
Output Configu	ration		
DEMUX 1:1 (//)			
Clock configuration		Single Event Protection	
Interleaving	Swing Adjust		
Disabled	Reduced	1 Onocked	
Enabled	© Full		
		Sampling Delay Adujst (SDA)	
Bandwidth	StandBy	Inshied     Dischied     Dischied     Dischied	1
C Extended	Core: A B	Delay (ps) 0	
Nominal	Full	Fine 0 🚖	
Trigger Mode		Core B	
Disabled Enabled	Analog 🗐 🕅	Enabled      Disabled     Delay (or)	1
•			=
		Fine 0 💌	
Reset Length			
16 💌			

Settings Calibration	Via FPGA)	EVIZAD550 Td 52.0 Refresh
ADC core Parallel output Output Con DEMUX 1:1 Clock configuration Interleaving Disabled	figuration //) Swing Adjust @ Reduced	Single Event Protection
Enabled      Bandwidth     Extended     Nominal      Trigger Mode      Disabled Enabled     ©	Full StandBy Core: A B Full Analog	Sampling Delay Adjust (SDA) Core A
Reset Length		Coarse 0 3

On AD5x0B (GUI 1.2.5)

In this window "ADC Core", the following functions are available:

- Output Configuration
- Clock Configuration
- Bandwidth
- Trigger Mode
- Reset Length
- StandBy
- Sampling Delay Adjust (SDA)
- Single Event Protection

### 4.7.1.1 Output configuration

If you have selected EV12AD550x, Demux 1:1 or Demux 1:2 can be chosen.

Figure 4-24. EV12AD550x Output Configuration

ile Device Help  ADC Settings  Log Laboration  Lab	Acquisition (via FPGA)	EV12AD550
ADC core Parallel output Chapter Confi DEMUX 1.1 (/ DEMUX 1.1 (/ DE	guration )  1(/) 2(/) Swing Adjust © Reduced Full StandBy Core: A B Full Analog	Single Event Protection Unlocked Sampling Delay Adjust (SDA) Core A Enabled Disabled Delay (ps) 30 Fine 0 Core B Core B Fine 0 Core B Core B Core Core B Core B C

If you have selected EV12AD500x, Demux 1:1 or SERIAL can be chosen.

File Device Help	Acquisition	EV12AD500	👶 Reset	SYNC	e2V
ADC core Parallel output Output Config DEMUX1:1 (/) / DEMUX1:1 DEMUX1:2 SERIAL © Insabled © Lobie	Vin Profit	Single Event Protection	Td48.1	Refresh	
Bandwidth © Extended © Nominal Trigger Mode	StandBy Core: A B Full	Enabled  Disabled Fine Core B	Delay (ps) 0		
Disabled Enabled Reset Length       16	Analog 🕅	Enabled @ Disabled	Delay (ps) 0		
28/10/2016 09:00:07		ADC ID ID ×0814 Serial ×0000 Da	te × 0000 Fuse	Fuse CRCs	A 🔵 B 🔵

4.7.1.2 Clock configuration

		Figure 4-26.Clock	Configuration			
			Clock configura	tion		
			Interleaving		Swing Adjust	
			Oisabled		Reduced	
			Enabled		© Full	
		<ul> <li>Interleaven</li> <li>The two ADC core</li> <li>Swing Acceleration</li> <li>Identical to swing</li> </ul>	ving: es can work in phase (sa Jjust (clock): adjust LVDS. It control	impling clocks aligne s SYNCO and SSO out	d) or interleaved. tput swings.	
4.7.1.3	Bandwidth					
		The ADC cores h details).	ave a tunable bandwi	dth depending on t	he package (refer to th	e datasheet for
		Figure 4-27. Band	width selection			
				Bandwidth		
				Extended		
				Nominal		
4.7.1.4	Trigger mode					
		When disabled (d When enabled, th	efault mode), the SYNC ne SYNC TRIG input acts	CTRIG input acts as t as the TRIGGER.	he SYNC.	
		Figure 4-28. Trigge	er Mode			

Trigge	er Mode
Disab	led Enabled
۲	0

To put the device in TRIGGER mode, it is mandatory to set Trigger Mode on Enabled. It is not sufficient; the control bits detailed in sections 4.7.2.3 for LVDS mode and 4.7.3.3 in serial mode must also be programmed properly.

#### 4.7.1.5 Reset Length

The reset length after a SYNC can be configured. This reset length translates into a certain number of data period where the data ready is maintained at low level after a RESET, when working with LVDS output.

Figure 4-29. Reset Length

Re	eset Lo	ength
	16	
		Contract of the second

The configuration by default is 16 data periods. The minimum is 2 data periods and the maximum is 63 data periods.

### 4.7.1.6 StandBy

The user can put the analog part of the device in standby mode. Full mode allows putting a core in a complete standby mode. Each box is independent. Refer to the datasheet for details on StandBy modes.

Figure 4-30. Standby

StandBy		
Core: Full	<b>A</b>	B
Analog		

#### 4.7.1.7 Single Event protect

Figure 4-31. Single event protection



If the padlock is green, the configuration of the device can be changed. If the padlock is red, no change is possible. A simple click on the padlock allows user to unlock/lock again.

### Software Tools

### 4.7.1.8 Sample Delay Adjust

The effective sampling instant of each ADC is adjustable independently thanks to the built-in fine internal clock shifter. Refer to the datasheet for further details.

Figure 4-32. Sampling delay Adjust

On AD5x0A (GUI 1.0.1)

C Enabled O Disabled	Delay (ps)	0
ine 0 😫 📄		
Core B		
Core B		14
Core B	Delay (ps)	0

### On AD5x0B (GUI 1.2.5)

	C Enabled O Disabled	Delay (ps)	30
Fine	0 🔄		
Coarse	0		
	Core B		
	Enabled Oisabled	Delay (ps)	30
Fine	0		
oarse	0		

## Sampling Delay Adjust (SDA)

	Enabled Disabled	Delay (ps)	30
Fine	0		
Coarse	0 🚖		
	Core B		
	Enabled Disabled	Delay (ps)	30
Fine	0		20
Contro	0		

By default, SDA is disabled (by-passed). Activating the SDA has an impact on the jitter performance of the device.

On AD5x0A version, only fine steps can be used.

On AD5x0B version, fine and coarse steps can be selected. When SDA is enabled on core A it is also enabled on core B and vice-versa.

#### 4.7.2 Parallel output

### Figure 4-33. User Interface Eval Kit – Parallel output (for EV12AD550x and EV12AD500x)

### On AD5x0A (GUI 1.0.1)

PRBS Swing Adjust // IR - Parity - Trigger _ fu1 Configuration Data Only Data + PRBS PRBS Only Test Mode Test mode Flash Ramp	Refresh C	48.9	Td			00	2AD	EV	<u>U</u>	Acquisition (via FPGA)	ibration	Parallel outpu	ADC Settings
Test Mode Test enable Disabled Enabled Test mode Flash © Ramp				rigger _ fu: Trigger rigger _ fu: Trigger _ fu:	ity - Tri Parity ity - Tri	IR - Pa		Swing Adjust @ Reduced O Full	n	PRBS Configuration Data Only Data + PRBS PRBS Only			
Test enable Disabled Enabled © Test mode © Flash © Ramp				0	0				t Mode	Ter			
Disabled Enabled Test mode Flash © Ramp									st enable	Tes			
Test mode Flash © Ramp									isabled Enabled	Dis			
S Flash Ramp									st mode	Tes			
									) Flash 💮 Ramp				

ADC Settings Calibration	(via FPGA)	EV12	2AD550	Td 52.0	SYNC Refresh
	PRBS Configuration Data Only © Data + PRBS PRBS Only ©	Swing Adjust Reduced Full	// IR - Parity - Trigger _ fu1 IR Parity Trigger // IR - Parity - Trigger _ fu2 IR Parity Trigger <ul> <li>O</li> </ul>		

In this window "Parallel Output", the following functions are available:

- PRBS (Pseudo-Random Binary Sequence)
- Swing Adjust (output data)
- //IR Parity Trigger\_fu1 and //IR Parity Trigger\_fu2
- Test Mode (on AD5x0A only)

### 4.7.2.1 PRBS

Pseudo Random Bit Sequence can be generated for LVDS output. It can be:

- Disabled
- Scrambling the data
- Output alone

The PRBS used is based on the sequence X7 + X6 + 1. When used with the LVDS output (in DEMUX 1:1 or 1:2), the same pseudo-random sequence is output on every digital data bit.

Figure 4-34. PRBS configuration

ł	KBS
	Configuration
	Data Only
	0
	Data + PRBS
	PRBS Only
	$\bigcirc$

By default, Data Only is selected.

### 4.7.2.2 Swing Adjust

IO's consumption represents a non-negligible part of dissipation. In case of short routing (in the range of 10 cm) or lower receiver input swing, it is possible to reduce the output dynamic and the consumption by using "swing adjust".

In parallel mode, the swing is reduced by 1/3.

Figure 4-35. Swing Adjust

Swing Adjust
Reduced
◎ Full

By default, reduced swing is selected.

### 4.7.2.3 //IR - Parity -Trigger\_fu1/fu2

In case of LVDS output, InRange (IR), Parity or Trigger (TRIG) signals are multiplexed on pad AFU1 and AFU2 for core A, on pad BFU1 and BFU2 for core B.

In Demux 1:1, InRange, Parity or Trigger, selected through SPI command, can be output:

- On AFU1/AFU2 for A high port
- On BFU1/BFU2 for B high port.

In Demux 1:2, InRange, Parity or Trigger, selected through SPI command, can be output:

- On AFU1 for A high port
- On AFU2 for A low port
- On BFU1 for B high port
- On BFU2 for B low port

Figure 4-36. //IR - Parity -Trigger\_fu1/fu2

// IR - Parity - 1		igger_fu1
IR	Parity	Trigger
۲	0	0
// IR -	Parity - Tr	igger _ fu2
IR	Parity	Trigger
0	0	0

See the datasheet to get explanations on the role of each bit.

Those bits work properly only if the trigger mode described in section 4.7.1.4 is put on Enabled.

4.7.2.4 Test Mode on AD5x0A only

Figure 4-37. Test Mode

Test e	nable
Disab	led Enabled
۲	0
200	
Test n	node

To access the test mode function, click on enabled button. In test mode selection, checking the box enables the relevant test mode.

Two test modes are available:

- Flash mode
- Ramp mode

Both are described in the datasheet.

Due to the FPGA code and the LVDS interface synchronization, it is not possible to use the test flash mode with the flash\_length setting under 16 when interleaving the 2 cores and using the LVDS interface (DMUX 1:1 and 1:2).

### 4.7.3 Serial output

Figure 4-38. User Interface Eval Kit – Serial Output (for EV12AD500x only)

File Device Help					
ADC Settings	Interleaving Acquisition Calibration	EV12AD5	500	Reset     SYNC       Td     48.9	e2V
ADC core Serial	PRBS Configuration Data + PRBS PRBS Only	Serial Swing Adjust Full Reduced StandBy Channel 1 Channel 2	Serial IR-Parity-Trigger IR Parity TimeStamp Trigger Channel 3 Channel 4		
28/10/2016 09:07:53		ADC ID I	D ×0814 Serial ×0000 Date	× 0000 Fuse 🥥 Fuse CRCs	а 🔾 в 🔾

In this window "Serial Output", the following functions are available:

- PRBS (Pseudo-Random Binary Sequence)
- Serial Swing Adjust (output data)
- Serial IR Parity Trigger
- StandBy

Note: This window is accessible only if you have selected EV12AD500x in the Device Menu and SERIAL mode in ADC core tab.

### 4.7.3.1 PRBS

There is an option to output the scrambled data (data + PRBS) according to ESIstream protocol or just the scrambling (PRBS only) on the serial interface. This can be used as a test mode to verify correct function of the serial interface. In PRBS only, the sampled data should be 0x000. Please refer to the datasheet for details on these functions.

Figure 4-39. PRBS configuration

PRBS	
Conf	iguration
Data	+ PRBS
PRB	S Only

By default, (Data + PRBS) is enabled.

### 4.7.3.2 Swing Adjust

IO's consumption represents a non-negligible part of dissipation. In case of short routing (in the range of 10 cm) or lower receiver input swing, it is possible to reduce the output dynamic and so the consumption by using "swing adjust". In serial mode, the reduction is 1/2.

Figure 4-40. Serial Swing Adjust



### Software Tools

### 4.7.3.3 Serial IR – Parity - Trigger

In case of serial link interface, InRange (IR) is multiplexed with Parity on output frame bit 12, trigger (TRIG) is multiplexed with a timestamp (PRBS sequence) on output frame bit 13.

The timestamp can be used to identify the samples order and/or check the synchronization of the serial interface.

Please refer to the datasheet for details on these functions.

By default, InRange and TimeStamp are selected.

Figure 4-41. Serial IR - Parity - Trigger

Serial	IR-Parity-	Frigger
IR	Parity ©	
Time ()	Stamp	Trigger

Those bits work properly only if the trigger mode described in section 4.7.1.4 is put on Enabled.

### 4.7.3.4 StandBy

Figure 4-42. StandBy

StandBy			
Channel 1 📃	Channel 2	Channel 3	Channel 4 📃

Each channel can be put in Standby mode by checking the relevant box. By default, all channels are active.

EV12AD5x0-EK User Guide

### 4.8 Interleaving calibration

ADC ttings	Interleaving Calibration	Acquisition (via FPGA)	<u>ധ</u>	EV12AD550	Td	Reset     SYNC       52.7     Refresh
OFFS	ET Core A 256	Core B 256 🔄	<ul> <li>Read</li> <li>Write</li> <li>0</li> <li>Core A</li> <li>Last Correction (</li> </ul>	Calibration input Automatic	C External cloc Signal Fre 10 Nb ol	locks k frequency (Hz) G S gquency (Hz) M S Samples
GAIN	Core A 512 🖈 1023 0	Core B 512 🔄	Read Write       0     0       Core A     Core B       Last Correction	Califration Start Calculation Selection Offset Gain Phase V V V Undo last correction (LSB)	2^16 : 6: St offsetA (code/LSB) 0.112 apple (4P/LSP)	eps offsetB (code/LSB) 0.112 opinP (dP/(LSD)
PHAS	E Core A 128 - 255 0	Core B	Read       Write       O     O       Core A     Core B		0.001 phaseA (s/LSB) -7f	0.001 phaseB (s/LSB) -7f alculate
Core	A TRIBENCE CI	annei	Lost Correction	(L30)		

Figure 4-43. User interface Eval Kit – Interleaving calibration

Figure 4-44. Automatic or Manual calibration

Automa	tic	
Man	ual (fro	m files
🗸 Auto	matic	NK 199899784
$\triangleright$	Start	
Calcula	tion Se	electio
Offset	Gain	Phase
	V	

The user has the choice between an automatic calibration done by the GUI and a manual calibration. Besides, the user can calibrate each part separately (Offset and/or Gain and/or Phase). Please refer to dedicated Application Note to run an interleaving calibration.

### 4.9 Acquisition (via FPGA)

Figure 4-45. User Interface EVal Kit – Acquisition (Via FPGA	aure 4-45. User int	erface Eval K	it – Acquisition	(via FPGA)
--	---------------------	---------------	------------------	------------

ADC Settings Calil	rleaving Acquisition (via FPGA)	EV12AD550	Td 52.0 Refresh
tandard			
INPUT/CONFIG		OUTPUT	
	Clocks	Display	
Data	External clock frequency (Hz)	Signals FFT Spectrum	FFT Parameters Histo - INL - DNL
Resolution (bits)	3G 🚖		
12	1st Tone Frequency (Hz)		
Number of Samples	100M	Error counts	
2^16:65536	2nd Tone Frequency (Hz)	A B	
	0	Parity 0 0	
	Coherent	InRange 0 0	
Processing	Frequency		
EET window	1		
Rectangular	DC Offset (nb of Points)	Export data	
FFT unit	4	Format	
dB	Nb of Harmonics	MS Excel	
FFT Band	25	File Name	
Center Frequency (Hz)	Peak width (nb of points)		Save&Close
0		Save Directory	- Neuronal Participante Contraction of Contractiono
Frequency Span (Hz)	IMU order		
0			
	Soan	Start Stop Dringer	
	(iii) Shap	Start Stop	

Note: This window is not visible if the system has not detected the VC709 board.

### 4.9.1 INPUT/CONFIG

Figure 4-46	. INPUT/	CONFIG
-------------	----------	--------

Data	External clock frequer	ncv (Hz)
Resolution (bits)	3G	
12	1st Tone Frequency	(Hz)
Number of Samples	100M	
2^16:65536	2nd Tone Frequence	y (Hz)
	0	
FFT window Rectangular	DC Offset (nb of	Points)
	Nb of Harmonic	s
FFT Band	25 🚔	
Center Frequency (Hz)	Peak width (nb o	of points
0		
Frequency Span (Hz)	IMD order	
E	0	

#### • Data

Resolution (bits): Resolution of the ADC (Read Only). Number of samples: Number of samples considered for acquisition (Must be a 2<sup>n</sup>).

### Figure 4-47. Data

Data	
Resolution (bit	s)
12	
Number of Sar	nples
2^16:65536	•

By default, a number of 65536 sampling points is selected.

Clocks

Figure 4-48. Clocks

CIOCKS	
External clock frequence	y (Hz)
3G	
1st Tone Frequency	(Hz)
100M	
2nd Tone Frequency	(Hz)
0	×
Coherent Frequency	

In order to ensure proper signal reconstruction and FFT calculation, the user has to fill in the following frequency values:

• External clock frequency (Hz): Master clock RF generator frequency.

. .

- 1st Tone Frequency (Hz): Analog RF generator frequency.
- 2nd Tone Frequency (Hz): In case of Dual Tone measurement, second Analog RF generator frequency.
- Coherent Frequency: Calculation of the coherent frequency versus total number of points and clock frequency.

Note: Number of Samples, Fclock, Fin, Interleaving mode can change the coherent frequency. Do not forget to re-click on the coherent frequency button when parameters are modified.

• Processing

Figure 4-49. Processing

Processing	
FFT window	
Rectangular 💌	DC Offset (nb of Points)
FFT unit	4
dB 💌	Nb of Harmonics
FFT Band	25 🚔
Center Frequency (Hz)	Peak width (nb of points)
0	0
Frequency Span (Hz)	IMD order
0	0

FFT window:

When the analog input signal and the sampling clock are not coherent signals, a FFT window has to be applied to obtain a correct result.

By default, rectangular is selected.

Blackmann-Harris (4th order) and Blackmann-Harris (7th order) are also available.

Figure 4-50. FFT Window

FFT window	
Rectangular 📃	DC Offset (nb of Points)
✓ Rectangular Blackmann-Harris (4th o Blackmann-Harris (7th o	order) armonics order)
Center Frequency (Hz)	Peak width (nb of points)
0	
Frequency Span (Hz)	IMD order
0	0

- FFT unit: Results can be expressed in dB or dBc.
- FFT band, center frequency and frequency span:

FFT calculations can be computed over a smaller range than Nyquist. To do so, center frequency and frequency span must be filled in.

- DC offset (number of points):

Number of points to be excluded from calculations to bypass DC peak (to ensure DC peak is not taken into account when computing FFT calculations). Default value depends on the selected FFT window.

Nb of Harmonics:

Number of Harmonics considered for THD and SNR calculation (Default value is 25 harmonics).

- Peak width:

When a FFT window is applied the harmonic signal is composed of several points.

The number to be filled in corresponds to the number of points that should be removed from the calculations on each side of the fundamental and harmonic signals.

As an example, if Peak Width = 4 then 4 points will be removed on the left of the peak and 4 points on the right of the peak; a total amount of 9 points will be removed (exclusion on left + exclusion on right + harmonic itself).

Default value depends on the selected FFT window.

IMD order:

In the case of dual-tone measurement, this box allows to choose the number of intermodulation harmonics to be computed.

F1	F1
F2	F2
1F1+1F2	1F1+1F2
1F1-1F2	1F1-1F2
	1F1+2F2
	1F1-2F2
	2F1+1F2
	2F1-1F2

*Figure 4-51.* Example of IMD order = 2 and IMD order = 3

### 4.9.2 OUTPUT



Si	gnals 📃	FFT Spectrum	FFT Parameters Histo - INL - DNL
Fror count	5		
	Α	В	
Parity	0	0	
InRange	0	0	
Exp	oi t uata		
Exp	Name	Format	
File	Name	Format	Save&Close
Exp	Name	Format	Save&Close

• Display

Figure 4-53. Display

Display			
Signals	FFT Spectrum	FFT Parameters	Histo - INL - DNL

By checking the boxes the user can select the data to be displayed. A dedicated window will then open.

On each opened window, refresh and zoom options are available. Also window sizes can be modified.

- Signals

In this window, sampled and reconstructed signals are visible.

Figure 4-54. Signal window with Reconstructed Signal



Control bits can be displayed using buttons on bottom left. All the control bits for core A and core B can then be visible.



#### Figure 4-55. Signal window with Control Bits

In interleaving mode, core A, core B and interleaved [A, B] can be visible together or separately.



Figure 4-56. Signal window with non-interleaved signal and interleaved signal

- FFT spectrum

Core A alone, Core B alone and interleaved can be displayed separately. 'Show annotations' box can be disabled.

Figure 4-57. FFT spectrum window



FFT parameters

-

This window allows reading the values of each parameter on core A or core B or interleaving. Results are given in dBc and dBFS.

Figure 4-58.	FFT	calculation	window
--------------	-----	-------------	--------

Core Selection						SI	DR Frequ	Jency (Hz)		
CoreA						4	18.968M			
Peak List							0.000111			
Label	Frequency (MHz)	Amplitude (dBm)	Overlap	*	Results			Fullscale Re	sults	
DC	0.000000	3.012481			THD	-63.036	dB	тнр	-71 0859	dRE
Fundamental	99.003601	-8.049906	44			0		771.0	0	upr
H2	198.007202	-88.634326	8 <u>89</u>	E	TILD	0	dB	TILD	0	dBF
H3	297.010803	-86.002258			TIMD	0	dB	TIMD	-8.04991	dBF
H4	396.014404	-97.222562	(inte		IMD3	Inf	dB	IMD3	Inf	dBF
H5	495.018005	-83.575447			SNR	51 4032	dB	SNR	59.4531	dRE
H6	594.021606	-102.103732	822		CILLAD	51 1140		CT LL D	50 16 47	upr
H7	606.974792	-78.919360	1000		SINAD	51.1148	dB	SINAD	59.1047	dBF
H8	507.971191	-104.044564			ENOB	8.19832	bits	ENOB	9.53551	bits
H9	408.967590	-73.980867	222		SFDR	-65.931	dBc	SFDR	-73.9809	dBF
H10	309.963989	-88.524061	822		SESR	-8.0499	dBES	NoiseEloor	-147.578	dBn
H11	210.960388	-83.653529		-	JUDIC					abri



- Histo- INL-DNL

#### • Error counts

Figure 4-60. Error counts

Error counts	i.	
	Α	В
Parity	0	0
InRange	0	0

This indicator displays errors relative to Parity and InRange bits for both cores depending on AFU 1/2, BFU 1/2 user selection.

The InRange bit indicates whether the input signal is within the ADC dynamic range or not. When the ADC input signal is over the ADC dynamic range, the InRange bit is low and it generates a +1 on the error indicator.

The Parity of the 12 output bits of each data is calculated by performing a XOR combination between the 12 bits of output data. It is output at the same time as the 12-bits data.

Refer to the datasheet for details on those functions.

### • Export Data

Figure 4-61. Export Data

	Format	
	MS Excel	
File Name		
		100000
		Save&Close

Data can be exported in Excel format.

Once MS Excel is checked, Excel Hide/show box appears. If the box is not checked, the recording is done but the file does not appear.

Figure 4-62. Excel Hide/Show

	Format	Excel
	MS Excel	Hide/Show
File Name		
		🔚 Save&Close
Save Directo	ny	

To save the data in Excel format, the user needs to create a File Name and choose the Directory in which the file will be recorded.

Figure 4-63. File Name and Directory

Export data Format	Eurol	
MS Excel	Hide/Show	
File Name		
Part1_Fin100M_Fc3G	🔚 Save&Clos	
Save Directory		
C:\		

From then onwards, each acquisition launched through 'SNAP' or 'START' buttons is recorded. *Figure 4-64.* SNAP/START-STOP

1	🛞 Snap	🙀 Trigger			
Status		Idle	<u> </u>	0	ACQ#

The user has the possibility to uncheck and then recheck the box "MS Excel" to select some acquisitions to be recorded and some to be run with recording data.

In the excel file, data are recorded one after the other. If a file is closed and reopened later, the existing data will not be deleted.

The following figures show examples of the excel file with <u>2 acquisitions on core A and core B</u>.

Figure 4-65. Data tal	b
-----------------------	---

1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1			MHz	MHz	MHz	MHz	Mhz			dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS
2	ACQ#	Core	Fc	Fin1	Fin2	FFT Band	FFT Band Width	Parity	InRange	THD	THD_FS	TIMD	TIMD_FS	TILD	TILD_FS	TD	TD_FS	SINAD	SINAD_F
3	1	A	2600	99.00360107	0	0	0	0	0	-70.22556126	-73.27817272	0	-3.052611459	0	0	-70.22556126	-73.27817272	55.92277435	58.9753
4	1	в	2600	99.00360107	0	0	0 0	0	0	-71.01516949	-74.07531156	0	-3.060142076	0	0	-71.01516949	-74.07531156	56.06177284	59.1219
5	2	A	2600	99.00360107	0	0	0 0	0	0	-62.78562839	-70.82776207	0	-8.042133676	0	0	-62.78562839	-70.82776207	51.07936797	59.1215
6	2	в	2600	99.00360107	0	0	0 0	0	0	-63.2380164	-71.29040355	0	-8.052387152	0	0	-63.2380164	-71.29040355	51.20248279	59.2548
7																			

1	2	3	4	5	6	7	E
1 ACQ#	‡ <b>1</b>	1	2	2	-		
2	Level_A	Level_B	Level_A	Level_B			
3	2567	2871	1258	1321			
4	3123	3319	1424	1574			
5	3446	3489	1736	1923			
6	3453	3329	2113	2306			
7	3143	2882	2480	2633			
8	2589	2247	2744	2825			
9	1907	1568	2857	2844			
10	1264	995	2787	2684			
11	796	660	2549	2380			
12	606	636	2202	2003			
13	746	928	1817	1636			
14	1174	1472	1485	1362			
15	1801	2145	1281	1242			
16	2482	2798	1246	1300			
17	3063	3277	1393	1526			
18	3422	3483	1690	1871			
19	3470	3369	2065	2256			
20	3197	2954	2433	2595			
21	2669	2335	2721	2809			
22	2001	1655	2855	2851			
23	1339	1061	2805	2712			
24	844	687	2590	2426			
25	610	618	2249	2053			-
14 4 P PI	Data / Data	ILD Samp	ledSignal 🦯	Sani 4	1111	•	Ĩ

### Figure 4-66. Sampled tab

### Figure 4-67. ControlBits tab

	1	2	3	4	5		6 7	8	9	10	11	12	13	14	15	16	E
1	ACQ#	1 1		1	1	1	1	1	1	2	2	2	2	2	2	2	1
2	2	Disparity (Se D	isparity (Se	Clock (Seria	I Clock (Serial	IR_A	IR_B	IR_A	IR_B	Disparity (S	Se Disparity	(Se Clock (Seri	ial Clock (Seri	al IR_A	IR_B	IR_A	
3	1	1 1		1	1	0	0	0	0	1	1	1	1	0	0	0	
4	1	1 1		1	1	0	0	0	0	1	1	1	1	0	0	0	
5		1 1		1	1	0	0	0	0	1	1	1	1	0	0	0	
6	5	1 1		1	1	0	0	0	0	1	1	1	1	0	0	0	
7	6	1 1		1	1	0	0	0	0	1	1	1	1	0	0	0	
14	4 1 1	Data Data_I	ILD / Sampl	edSignal 🦯	SampledSignal	ILD	ControlBits /	ControlBits_ILD	Reconstru	uctedSignal 🛛 🖣			.111			▶	

1	1	2	3	4	5	6	7	-
1	ACQ#	1	1	2	2			
2		Level_A	Level_B	Level_A	Level_B			
3		2567	2871	1258	1321			
4		2561	2871	1258	1321			
5		2561	2870	1259	1324			
6		2563	2870	1260	1320			
7		2563	2870	1259	1322			
8		2567	2874	1256	1322			
9		2567	2872	1257	1320			
10		2564	2872	1258	1317			
11		2565	2869	1257	1323			
12		2565	2873	1257	1322			
13		2564	2873	1257	1319			
14		2565	2873	1257	1320			
15		2563	2874	1257	1323			
16		2564	2876	1257	1321			
17		2565	2871	1258	1322			
18		2563	2872	1258	1322			
19		2565	2874	1257	1321			
20		2566	2873	1256	1322			
21		2566	2871	1258	1322			,
14	< > >I	Reconstru	ctedSignal /	Reconstructe	edSII∢		•	Π

Figure 4-68. ReconstructedSignal tab

### Figure 4-69. Histogram Tab

A	1	2	3	4	5	6	7	
1	ACQ#	1	1	2	2			
2		Histo_A	Histo_B	Histo_A	Histo_B			
3		0	0	0	0			
4		0	0	0	0			
5		0	0	0	0			
6		0	0	0	0			
7		0	0	0	0			
8		0	0	0	0			
9		0	0	0	0			
10		0	0	0	0			
11		0	0	0	0			
12		0	0	0	0			
13		0	0	0	0			
14		0	0	0	0			
15		0	0	0	0			
16		0	0	0	0			
17		0	0	0	0			
18		0	0	0	0			
19		0	0	0	0			
20		0	0	0	0			
21		0	0	0	0			*

4	1	2	3	4	5	6	7	-
1 A0	CQ#	1	1	2	2			100
2		INL_A	INL_B	INL_A	INL_B			
3		0	0	0	0			
4		0	0	0	0			
5		0	0	0	0			
6		0	0	0	0			
7		0	0	0	0			
8		0	0	0	0			
9		0	0	0	0			
10		0	0	0	0			
11		0	0	0	0			
12		0	0	0	0			
13		0	0	0	0			
14		0	0	0	0			
15		0	0	0	0			
16		0	0	0	0			
17		0	0	0	0			
18		0	0	0	0			
19		0	0	0	0			
20		0	0	0	0			
21		0	0	0	0			

### Figure 4-70. INL Tab

### Figure 4-71. DNL Tab

1	1	2	3	4	5	6	7	E
1	ACQ#	1	1	2	2			
2		DNL_A	DNL_B	DNL_A	DNL_B			
3		0	0	0	0			
4		0	0	0	0			
5		0	0	0	0			
6		0	0	0	0			
7		0	0	0	0			
8		0	0	0	0			
9		0	0	0	0			
10		0	0	0	0			
11		0	0	0	0			
12		0	0	0	0			
13		0	0	0	0			
14		0	0	0	0			
15		0	0	0	0			
16		0	0	0	0			
17		0	0	0	0			
18		0	0	0	0			
19		0	0	0	0			
20		0	0	0	0			
21		0	0	0	0			

### Figure 4-72. Spectra Tab

1	1	2	3	4	5	6	7	8	9	10	11
1	ACQ#	1	1	1	1	2	2	2	2		
2		Freq_A	Level_A	Freq_B	Level_B	Freq_A	Level_A	Freq_B	Level_B		
3		0	3.01400694	0	3.008082	0	3.01465718	0	3.00904454		
4		0.01983643	-104.147296	0.01983643	-91.3741539	0.01983643	-91.1491798	0.01983643	-118.673829		
5		0.03967285	-94.6385042	0.03967285	-98.7965797	0.03967285	-97.7040536	0.03967285	-98.6374052		
5		0.05950928	-102.875651	0.05950928	-94.782427	0.05950928	-101.415289	0.05950928	-100.838084		
7		0.0793457	-106.654031	0.0793457	-102.762423	0.0793457	-98.3345692	0.0793457	-102.876576		
В		0.09918213	-105.949862	0.09918213	-105.14727	0.09918213	-113.141035	0.09918213	-106.750864		
9		0.11901855	-104.281204	0.11901855	-106.810569	0.11901855	-103.059669	0.11901855	-105.194897		
0		0.13885498	-108.20424	0.13885498	-110.256978	0.13885498	-113.805367	0.13885498	-101.838319		
1		0.15869141	-104.964051	0.15869141	-94.4930559	0.15869141	-103.389521	0.15869141	-104.093398		
12		0.17852783	-101.103101	0.17852783	-113.822514	0.17852783	-126.501342	0.17852783	-104.661761		
L3		0.19836426	-101.315645	0.19836426	-105.63216	0.19836426	-101.854641	0.19836426	-102.395974		
14		0.21820068	-102.924579	0.21820068	-104.63625	0.21820068	-107.400135	0.21820068	-104.454008		
15		0.23803711	-102.77577	0.23803711	-104.387502	0.23803711	-103.937956	0.23803711	-108.994295		
16		0.25787354	-105.055838	0.25787354	-108.852717	0.25787354	-100.726318	0.25787354	-102.2771		
17		0.27770996	-99.7947894	0.27770996	-111.065893	0.27770996	-104.103411	0.27770996	-99.1046082		
18		0.29754639	-111.996859	0.29754639	-100.07417	0.29754639	-101.922465	0.29754639	-104.385243		
19		0.31738281	-105.549353	0.31738281	-106.145129	0.31738281	-123.735464	0.31738281	-103.426974		
20		0.33721924	-101.783379	0.33721924	-112.327612	0.33721924	-111.454681	0.33721924	-100.404975		
21		0.35705566	-106.581132	0.35705566	-101.4589	0.35705566	-102.262835	0.35705566	-107.611333		
4 4	I F FI	/INL ILD /		D Spectra	Spectra ILI	D / Harmonic	s ∕ Hī ◀		10		•

### Figure 4-73. Harmonics Tab

4	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	ACQ#	Core	DC_Freq	DC_Level	Fund_F1_Freq	Fund_F1_Level	H2_F1_Freq	H2_F1_Level	H3_F1_Freq	H3_F1_Level	H4_F1_Freq	H4_F1_Level	H5_F1_Freq	H5_F1_Level	H6_F1_F
2	1	A	0	3.014007	99.00360107	-3.052611459	198.007202	-82.7346817	297.010803	-84.3650793	396.014404	-92.2219979	495.018005	-82.8553845	594.021
3	1	в	0	3.008082	99.00360107	-3.060142076	198.007202	-83.6778891	297.010803	-81.3623815	396.014404	-84.6694904	495.018005	-92.1460326	594.021
1	2	A	0	3.014657	99.00360107	-8.042133676	198.007202	-87.0433067	297.010803	-88.8944693	396.014404	-96.4167183	495.018005	-82.0868363	594.021
5 '	2	в	0	3.009045	99.00360107	-8.052387152	198.007202	-85.9731399	297.010803	-94.0938342	396.014404	-99.4940235	495.018005	-85.3024977	594.021
5		1													

### Figure 4-74. Identification of the 2 acquisitions on core A and core B

1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	E
1			MHz	MHz	MHz	MHz	Mhz			dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc
1	ACC	Core	Fc	Fin1	Fin2	FFT Band	FFT Band Width	Parity	InRange	THD	THD_FS	TIMD	TIMD_FS	TILD	TILD_FS	TD	TD_FS	SINAL
3	1	A	2600	99.00360107	0	0	C	0	C	-70.22556126	-73.27817272	. 0	-3.052611459	0	0	-70.22556126	-73.27817272	55.92
5	1	в	2600	99.00360107	0	0	C	0	C	-71.01516949	-74.07531156	C	-3.060142076	0	0	-71.01516949	-74.07531156	56.06
1	2	А	2600	99.00360107	0	0	C	C	C	-62.78562839	-70.82776207	C	-8.042133676	0	0	-62.78562839	-70.82776207	51.07
6	2	в	2600	99.00360107	0	0	C	0	C	-63.2380164	-71.29040355	0	-8.052387152	0	0	-63.2380164	-71.29040355	51.20
K																		
	E F H	Data	Da	ta 11 D Sam	nledSi	innal Sa	moledSignal TLD	Cont	rolBits	ControlBits ILD	Reconst	1		1				► III

When interleaving clock is enabled, XXX\_ILD tabs are created. In the example below, first line corresponds to the  $1^{st}$  acquisition and second line corresponds to the  $2^{nd}$  acquisition.

### Figure 4-75. Data\_ILD Tab

1	13	14	15	16	17	18	19	20	21	22	23	24	25	-	
1	dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS	MHz	dBc	dBFS	bits	bitsFS	dBFS	Ē
2	TILD	TILD_FS	TD	TD_FS	SINAD	SINAD_FS	SFDR	SFDR_FS	SFDR Freque	SNR	SNR_FS	ENOB	ENOB_FS	SFSR	=
3	-54.0010134	-57.0574058	-53.9205253	-56.9769177	51.8723675	54.9287599	-54.0010134	-57.0574058	1200.9964	56.12048301	59.1768754	8.32416195	8.83186833	-3.05	Ł
4	-53.8181769	-61.8654524	-53.3541923	-61.4014677	49.2648724	57.3121479	-53.8181769	-61.8654524	1200.9964	51.41159586	59.4588713	7.89102323	9.22777994	-8.04	
5															
6															
7															
14	♦ ► ► Data	Data II D	SampledSig	al Sample	dSignal TLD	ControlRits	ControlBits	ILD Reco	nell 4					b II	r.

1	2	3	4	5	6
1 ACQ	# 1	2			
2	Level	Level			
3	2567	1258			
4	2871	1321			
5	3123	1424			
6	3319	1574			
7	3446	1736			
8	3489	1923			
9	3453	2113			
10	3329	2306			
11	3143	2480			
12	2882	2633			
13	2589	2744			
14	2247	2825			
15	1907	2857			
16	1568	2844			
17	1264	2787			
18	995	2684			
19	796	2549			
20	660	2380			
21	606	2202			
22	636	2003			
23	746	1817			
24	928	1636			
25	1174	1485			
26	1472	1362			
27  4 4 } H	1801 SampledSi	1781 gnal_ILD Con	trolBits 4		► []

Figure 4-76. Sampled ILD Tai
------------------------------

### Figure 4-77. Harmonics\_ILD Tab

1.1	1	2	3	4	5	6	124	125	126	127	128	129	130	131
1	ACQ#	DC_Freq	DC_Level	Fund_F1_Freq	Fund_F1_Level	H2_F1_Freq	//	S.+1F2_Freq	1F1+1F2_Level	1F1-1F2  _Freq	1F1-1F2  _Level	1F1+2F2_Freq	1F1+2F2_Level	1F1-2F2  _F
2	1	0	3.011044975	99.00360107	-3.056392421	198.0072021	//	0	0	0	0	0	0	
3	2	0	3.011851316	99.00360107	-8.047275417	198.0072021	//	0	0	0	0	0	0	

In Harmonics tab, in addition to all harmonics, there are interleaved spurs [Fclock/2]  $\pm$  [nFin] where n = 1 or 2.

### Software Tools

### 4.9.3 Acquisition

Four buttons are available for acquisition:

- Snap: the acquisition will be run one single time
- Start: the acquisition will continuously run until a stop is done
- Stop: the acquisition will be stopped as soon as possible
  - Trigger: the acquisition is launched once when there is a pulse on SYNC TRIG. The ADC needs to be in TRIGGER mode (Please refer to datasheet). The acquisition is triggered 5 clock cycles after the trigger reception.

The status is visible and the counter of acquisitions is updated.

Figure 4-78. Acquisition running

-





	Clocks	Display
Data	External clock frequency (Hz)	Signals FFT Spectrum FFT Parameters Histo - INL - DNL
Resolution (bits)	2.6G	
12	1st Tone Frequency (Hz)	
Number of Samples	99.0036010742M	Error counts
2^16:65536 💌	2nd Tone Frequency (Hz)	A B
	0 🔄 👷	Stopping Acquisition
FFT window Rectangular FFT unit	DC Offset (nb of Points)	Format
FFT window Rectangular FFT unit dB	DC Offset (nb of Points)	Format
FFT window Rectangular FFT unit dB FFT Band	DC Offset (nb of Points)	Format MS Excel File Name
FFT window Rectangular FFT unit dB FFT Band Center Frequency (Hz)	DC Offset (nb of Points) 4	Format MS Excel File Name Partl_Fin99M_Fc2600M
FFT window Rectangular FFT unit dB FFT Band Center Frequency (Hz) 0	DC Offset (nb of Points)	Format MS Excel File Name Parti_Fin99M_Fc2600M Save Directory
FFT window Rectangular FFT unit dB FFT Band Center Frequency (Hz) 0 Frequency Span (Hz) 0	DC Offset (nb of Points) 4 25 2 Peak width (nb of points) 1MD order 0 20	Format MS Excel File Name Part1_Fin99M_Fc2600M Save Directory Ut\Plbm\BDC\Carac\CALLISTO\1_Environnement\User
FFT window Rectangular FFT unit dB FFT Band Center Frequency (Hz) 0 E Frequency Span (Hz) 0 E	DC Offset (nb of Points) 4 25 25 25 25 25 25 25 25 25 25 25 25 25	Format MS Excel File Name Part1_Fin99M_Fc2600M Save Directory Ut\Plbm\BDC\Carac\CALLISTO\1_Environnement\User

Figure 4-80. Acquisition done

	🖲 Snap	💽 Start	Stop	🙀 Trigger	
Status		ACQUISITION	Done	0	ACQ#

### 4.10 Regional and language options

Use the Regional Settings window to check if decimal separator is configured with a dot "."

In regional and language options, select "customize this format"

### Figure 4-81. Regional and language options window

rançais (France)			
Eormate de date el	t d'haura		
Date courte :	jj/MM/aaaa		
Date longue :	jjjj j MMMM aaaa 🔹		
Heure courte :	HH:mm		
Heure longue :			
Premier jour de la semaine :			
Que signifie la not	ation ?		
Exemples			
Date courte :	28/10/2016		
Date longue :	vendredi 28 octobre 2016		
Heure courte :	12:47		
Heure longue :	12:47:10		
	Desmiètes supplémentaises		

On this tab, the decimal separator must be configured with a dot ".". *Figure 4-82.* Customize Regional option sheet numbers

Nombres Sy	mbole monétaire Heure	Date			
Exemples					
Positif :	123 456 789.00	Négatif :	-123 456 789.00		
			$\sim$		
Symbo	ole décimal :		$( \cdot )$		
Nomb	ore de décimales :		2	•	
Symbo	ole de groupement des	chiffres :			
Group	ement des chiffres :		-		
Symbo	ole du signe négatif :				
Format de nombre négatif :			-1.1		
Affich	er les zéros en en-tête :		0.7 ;		
Sépara	ateur de listes :				
Systèr	me d'unités de mesure :		Métrique		
Chiffre	es standard :		0123456789		
Utilise	r les chiffres natifs :		Jamais		
Cliquez su défaut pou et les dates	r Réinitialiser pour resta ur les nombres, les symb s.	urer les paramètre oles monétaires,	s par Réinitialis	er	

# Section 5. FPGA CODE



The FPGA code has been designed to be used with VC709 Xilinx Virtex 7 evaluation board. Please refer to Xilinx: <u>http://www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html</u>

Warning: Please configure your VC709 evaluation board as follows: SW2: all OFF + SW11: 4 ON and 1/2/3/5 OFF.

### 5.1 Software Configuration

Xilinx configuration: Virtex-7 FPGA VC709 Evaluation Kit Vivado 2015.4.

### 5.2 FPGA binary file

**Loading .bit on VC709** Possible with Vivado.
Loading .mcs on VC709

Possible with Vivado 2014.1 onwards. Start Vivado. Flow => Open Hardware Manager



Open target => Auto Connect (The board has to be powered up at this time and the USB cable connected between J20 on board and PC).

Nivado 2014.4		a second seco
File Eat Fjow Ioos Window U だ 👌 119 6月 🌆 🌆 🗙   🐝	ayout yew Help	· # * 1 8
Hardware Manager - unconnected No hardware target is open. Open	target	
Hardware 옥조후 📰 🔖 ) ) ) it III	Auto Connect Recent Targets	ug Probes 🗆 L <sup>a</sup> X
Name Status	Closed Targets  Open New Target	

The FPGA is detected.



Right click on FPGA (xc7vx690t\_0) => Add Configuration Memory Device

ne gat How ]	008	Mindow Layout Wew Help	- 7	( & X ( Q)
Hardware Manage	er i	ocalhost/xilnx_tcf/Diglent/210203826219A		
There are no de	bug	cores. Program.device. Befresh.device.		
Hardware _ ロビ× 久江市区 時 日 1 日 1 日			Debug Probe	
Name localhost (1) localhost (1)	/Dig	Status Connected lent/210203826219A (1) Open		
AX Q		Hardware Device Properties Program Device Refresh Device	Ctrl+E	
		Add Configuration Memory Device Boot from Configuration Memory Device		
		Program BBR Key Clear BBR Key		
		Program ePUSE Registers		
und an De la D		Export to Spreadsheet		

A new window appears to configure the memory device loading. This window asks for memory part number.

For VC709, it is the mt28gu01gaax1e-bpi-x16 (NB: there are 2 different memory part numbers that can be set up on the VC709).

(ganufacturer Density (bb)     Al     *       Beset Al Filters     Width     Al     *       Configuration Memory Part     Beset Al Filters     *       Search:     Q=00ag     (1 match)       Name     Part     Manufacturer     Alas     Family     Type     Density (Mb)     Width       Imt28gu0 Lgasx1e-bpt-x16     mt28gu0 Lgasx1e/bpt-x16     1024     x.16	evice: 🧇 xc7vx690 r	U								
Density (Mb)     All       Beset All Filters       ct Configuration Memory Part       Search:     Q= 00ag       (1 match)       Name     Part       Manufacturer     Alas       Family     Type       Density (Mb)     Width       Imt28pu0 Lpasx1e-bpt-x16     mt28pu0 Lpasx1e/bpt-x16	Manufacturer	Al		Ŧ			Туре	Al		Ŧ
Reset Al Filters         Configuration Memory Part         Search: Q- 00ag         Name       Part       Manufacturer       Alas       Family       Type       Density (Mb)       Width         Im t28gu0 Lgasx1e-bpt-x16       mt28gu0 Lgasx1e-       Micron       28f00ag16f       g19       bpt       1024       x.16	Density (Mb)	Al		w			Width	Al		w
🛥 mt28gu01gaax1e-bpl-x16 mt28gu01gaax1e Micron 28f00ag16f g18 bpl 1024 x16	Name		Part	Manufacturer	Allas	Family	Туре	Density (Mb)	Width	
	THE TEL		mt28cu01caavie	Micron	28f00ag18f	g19	6pi	1024	x16	
	mt28gu0 Lgaan	1e-bpi-x16	112220012000							
	mt28gu01gaax	1e-bpi-x16								

Next pop-up will start the memory loading (if clicked on 'OK').



Next window lets you configure the loading. Keep the default value below and check that the correct .mcs is set up in Configuration file.

Program Configuration fi	tion Memory le and set pro	Device gramming options.	 ↓
Memory Device: Configuration file: State of non-config m Program Operations	iem I/O pins:	tricalisto foga/Calisto_TOP.mcs Puli-none	
Address Range: RS Pins: C Grase Blank Check Program C Venify	Configuration	n File Only 🔻	
			OK Cancel

Click 'OK', the memory loading starts.

### 5.3 FPGA program architecture

- EV12AD5x0x-EK Eval kit Functional Architecture
  - Parallel Interface

Figure 5-1. Functional architecture for parallel output



Color	Clock	Min frequency	Max frequency	Synchronized with
	Deserializer clock for core A	300 MHz	700 MHz	
	Deserializer clock for core B	300 MHz	700 MHz	Deserializer clock for core A
	Sync generator clock	MCLK freq	200 MHz	MCLK
	RAM and BER clock for core A	75 MHz	175 MHz	1/4 deserializer clock for core A
	RAM and BER clock for core B	75 MHz	175 MHz	1/4 deserializer clock for core B

• Serial Interface



### Figure 5-2. Functional architecture for serial output

Color	Clock	Min frequency	Max frequency	Synchronized with
	Deserializer clock		6 GHz	
	IP output clock	2 x MCLK freq	375 MHz	
	Sync generator clock	MCLK freq	200 MHz	MCLK
	RAM and BER clock	PCLK freq	187,5 MHz	1/2 IP output clock

# Section 6. DATA INTERFACE BOARD

The data interface board is provided with the evaluation kit. It is intended to be used with a logic analyzer. This section describes the board itself and the recommended connections to logic analyzer.



#### **Global overview**

Zoom on core A



#### Zoom on core B

BDR BFU2 BFU1 BH10 BH9 BH8 JP4 N P	IN IN IN IN IN IN IN IN IN IN IN IN IN I			10_8 10_6 10_1 0DE_FPGA
BH7	BH7 BI	L7 ( 10 10 BL7	ť	
BHB	EH6 B	L6 ( 10 CL6	1	
BH5	BH5 B	L5 (	1	No. of Concession, National Science of Concession, National Sc
BH4	EH4 B	L4 ( 18 BL4	1	
BH3	EH3 B	L3 ( BEL3	8L11	10.00
BH2	BH2 B	L2 W BL2	BL 10	Na 12, 10
BHI	GHI B		BL9	9.4
BHE	GHØ 8		BLB	21.6
NP	JP3	T P JP7		NP

## Board with the 2 boards connected to logic analyzer



# **Section 7. Ordering Information**

Table 7-1. Ordering information

Part Number	Temperature	Comments
EV12AD550A-EK	Ambient	Contact sales for availability
EV12AD550B-EK	Ambient	Contact sales for availability
EV12AD500A-EK	Ambient	ROHS compliant
		Contact sales for availability

Note: For any technical questions, contact Teledyne e2v hotline (hotline-bdc@teledyne-e2v.com)

Abbreviation	Term	Definition				
DNL	Differential non-linearity	The Differential Non Linearity for an output code "i" is the difference between the measured step size of code "i" and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximu value of all DNL (i). DNL error specification higher than -1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.				
ENOB	Effective Number Of Bits	$ENOB = \frac{SINAD - 1.76 + 20 \log (A I FS/2)}{6.02}$ Where A is the input amplitude and the full scale range of the ADC unce				
GUI	Graphical User Interface					
IMD	Intermodulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to th worst third order intermodulation products. It may be reported in dBFS (i.e., related to conver full scale), or in dBc (i.e., related to carrier signal level).				
INL	Integral non-linearity	The Integral Non Linearity for an output code "i" is the difference between the measured input roltage at which the transition occurs and the ideal value of this transition. NL (i) is expressed in LSBs, and is the maximum value of all  INL (i) .				
JITTER	Aperture uncertainty	Sample to sample variation in aperture delay. The vo slew rate of the signal at the sampling point.	oltage error due to jitter depends on the			
LDO	Low-Drop Out regulator					
ROHS	Restriction of Hazardous Substances					
SFDR	Spurious Free Dynamic Range	Ratio expressed in dB of the RMS signal amplitude, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may n be a harmonic. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).				
SINAD	SIgnal to Noise And Distortion ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).				
SNR	Signal to Noise Ratio	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the 25 <sup>th</sup> first harmonics. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).				
SSO	Slow Synchronization Output	See datasheet for details				
THD	Total Harmonic Distortion	Ratio expressed in dB of the RMS sum up to 25 <sup>th</sup> har amplitude. It may be reported in dBFS (i.e., related t to carrier signal level).	monic components, to the RMS input signal o converter full scale), or in dBc (i.e., related			
TSYNC	SYNC duration	xternal SYNC pulse width needed for SYNC function.				