EV12AD5x0x-EK

VITA 57 FMC DUAL 12b ADC Evaluation kit

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Section 1. General Overview

The EV12AD5x0x Eval Kit enables the easy evaluation of the characteristics and performance of DUAL 12-bit ADC EV12AD5x0x.

The Eval Kit is delivered with a software allowing acquisition of data with the FPGA.
The EV12AD5x0x Eval Kit is compatible with VITA 57 FMC (FPGA Mezzanine Card) standard.
For more information please see the VITA web site: http://www.vita.com/fmc.html
The DUAL 12-bit ADC Eval Kit is compatible with Virtex-7 FPGA VC709 Connectivity Kit (not provided). Please see Section 5 "FPGA CODE".
The FPGA VHDL data acquisition code for VC709 board is supplied.

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Its function is as a development system, demonstrating the performance of Teledyne e2v semiconductors components and not as a final product available on general release.

Since this Development Kit is intended to be used on an industrial workbench and modified by the user to build his prototypes, NO WARRANTY OF ANY KIND can apply.

All Hardware modifications are made at user's risk.

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1.2 EV12AD5x0x

The EV12AD5x0x-EK Eval Kit is based on Teledyne e2v EV12AD5x0x Dual 12-bit 1.5Gsps ADC for which block diagrams are given below.

EV12AD550x is a dual 12 bit 1.5GS/s ADC featuring a built in selectable 1:2-1:1 DEMUX, and LVDS parallel outputs (see Figure 1-1 and Figure 1-2 below).
For EV12AD550x refer to http://www.e2v.com/products/semiconductors/adc/ev12ad550/.

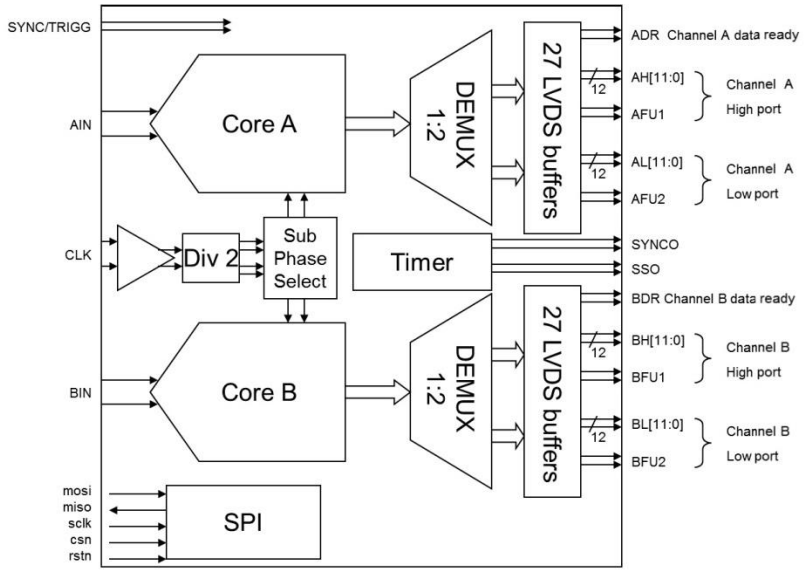
EV12AD500x is a dual 12 bit 1.5GS/s ADC featuring selectable serial output on 4 (or 2) lanes per ADC core or a selectable parallel output LVDS in 1:1 mode (see Figure 1-3 below).
For EV12AD550x refer to http://www.e2v.com/products/semiconductors/adc/ev12ad500/.

The two ADC cores can operate in phase or in opposition (option controlled through the SPI) to interleave the two cores. External clock must be provided at twice the individual sampling rate.

The innovative architecture allows for high sampling rate (up to 1.5GS/s) without interleaving thus providing high level of spectral purity.

Tunings and functionalities are controlled through a Serial Peripheral Interface (SPI).

Figure 1-1. Simplified block diagram LVDS demux 1:2 configuration EV12AD550x

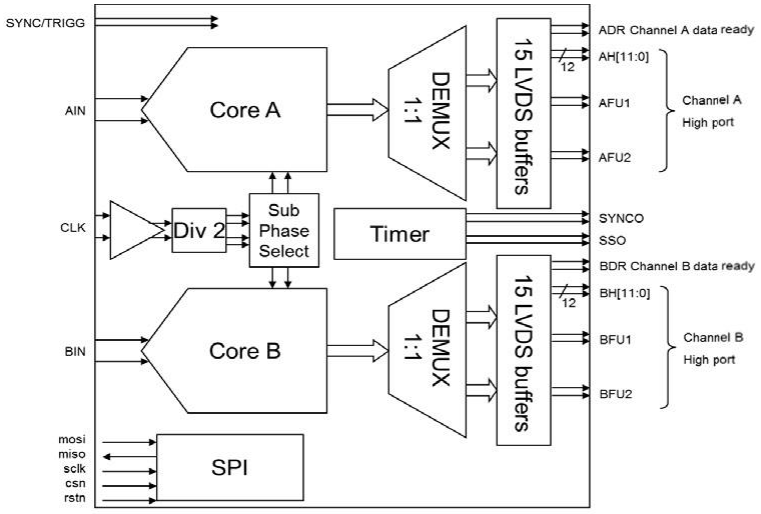


The block diagram above (Figure 1.1) refers to DEMUX 1:2 mode for output buffer affectation.

- Data Ready
- 12 bit of Data on high and low port
- In Range, Parity or Trigger, selected through SPI command, output
  - On AFU1 for A high port
  - On AFU2 for A low port

- On BFU1 for B high port
- On BFU2 for B low port

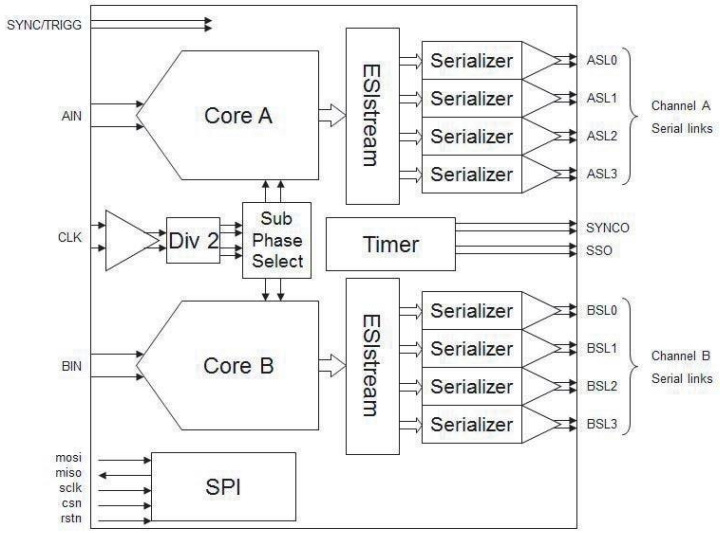
Figure 1-2. Simplified block diagram LVDS demux 1:1 configuration EV12AD5x0x



The block diagram above (Figure 1.2) refers to DEMUX 1:1 mode for output buffer affectation.

- Data Ready
- bit of Data on high port
- In Range, Parity or Trigger, selected through SPI command, output
  - on AFU1/AFU2 for A high port
  - on BFU1/BFU2 for B high port.

Figure 1-3. Simplified block diagram serial link or LVDS demux 1:1 configuration EV12AD500x



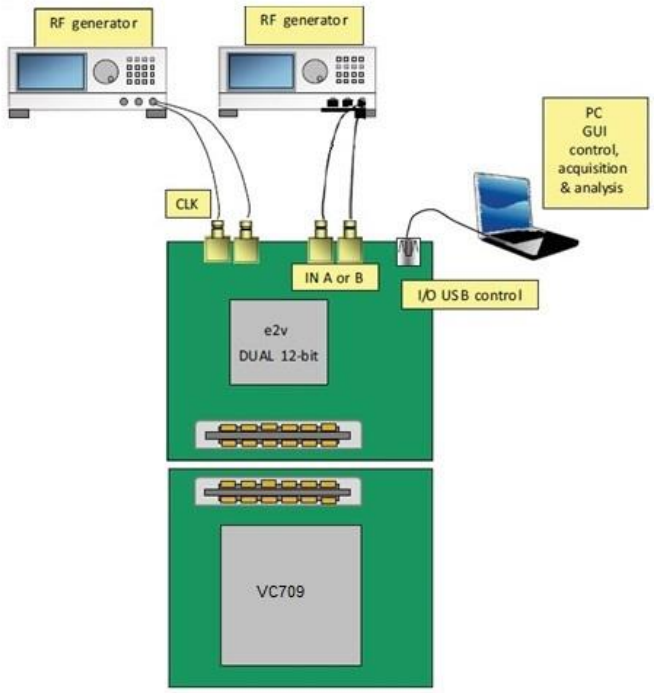
Depending on SPI code, the LVDS mode or serial mode is activated. Both interfaces cannot be enabled simultaneously.

1.3 Eval Kit

The user has 2 choices to connect the EV12AD5x0x board:

- with VC709 Virtex 7 evaluation board from Xilinx (not provided)
- with Data interface board

Figure 1-4. Eval Kit EV12AD5x0x-EK System with VC709



The complete system is built with the Teledyne e2v Eval Kit and the VC709 evaluation board from. Teledyne e2v Eval Kit contains the following items:

- DUAL 12-bit ADC Eval Kit with EV12AD5x0x ADC
- Cables & Power Supply
  - Universal 12V power adapter & cables
  - USB Cables to communicate with a PC (control of ADC settings and settings for data acquisition)
- USB key or CD ROM with GUI Software, VC709 FPGA software
- Data Interface Board

Note: The Virtex 7 FPGA VC709 with XC7VX690T-2FFG1761C FPGA is not supplied within the Teledyne e2v kit and should be purchased separately from Xilinx or its authorized distributors.

Acquisition and formatting of ADC digital output data are done within the FPGA.

Data is then transmitted again to the ADC Eval Kit.

A USB driver on the ADC Eval Kit allows data transmission to the computer that performs the display and processing of ADC output data (FFT).

Software and graphical User Interface are provided with the Eval Kit.

The provided software operates using Labview Run Time (no license required).

1.4 External equipment

The EV12AD5x0x Eval Kit needs very little external hardware.

RF generator for clock input:

- The EV12AD5x0x can sample signals up to 1.5Gsps.
- For optimum performance this generator must have a low phase noise. Please see Table 1-1. “Example of RF Generators” below.
- Balun should be used to provide a differential input.

RF generator for analog input signal:

- The EV12AD5x0x has a bandwidth up to 5300MHz.
- For optimum performance this generator must have a low phase noise. Please see Table 1-1. “Example of RF Generators” below.
- Filter should be used to remove input generator harmonics and balun should be used to provide a differential input.

Cables & Power Supply (provided by Teledyne e2v):

- Universal 12V power Adapter & Cables.
- USB Cable to communicate with a PC (control of ADC settings and acquisition settings).

Note: The Eval Kit allows external control of power supplies (Cables not provided). See Section 3.7.

PC with windows:

- Windows XP or Windows 7 (32 and 64bit). Please see Section 4.2. “Configuration”.

FPGA evaluation board is compatible with VITA57 FMC Standard:

- This Eval Kit board has been especially designed to be connected to the Xilinx Virtex-7 evaluation board VC709.
- The EV12AD5x0x Eval Kit could be used with other FPGA evaluation boards compatible with VITA57 FMC Standard. However, an assessment of connections should be done prior to connecting the FPGA board in order to ensure full compatibility.
- FPGA code to interface with GUI is provided only for VC709.

Table 1-1. Example of RF sources

Signal generator	**SSB phase noise @1GHz (20 KHz offset)**
Agilent E4424B 250KHz 2GHz (High spectral purity)	< -134dBc/Hz
Agilent E4426B 250KHz 4GHz (High spectral purity)	< -134dBc/Hz
SMA100A 9 KHz 6GHz (High spectral purity)	< -140dBc/Hz
PLL LTC6946-3	< -140dBc/Hz (1MHz Offset)
PLL STW81200	< -156dBc/Hz (1MHz Offset)

Section 2. QUICK START

2.1 Basic configuration of the board

The board is delivered in the following configuration.

Jumpers

- JP1 – JP9 – JP10 – JP6 – JP7 and JP8 are set to “LDO” so that internal supply is provided to the ADC. See Section 3.7 for details.
- JP3 – JP4 –JP5 are connected
- JP2 is set on EXT
- JP17 is connected
- JP11 is connected so that 100µA current source is ON for diode voltage measurement. See Section 3.5 for details.

Red Switches

- S3 is set on FLASH
- S4 is on µC
- S5 is set on µC
- S6 is set on FPGA
- S10 is set on ADC

Black Switches

- All tips of S8 are OFF
- For AD550, all tips of S9 are OFF
- For AD500, all tips of S9 are ON except S9-1 that is ON

2.2 Operating procedure

In the following procedures, supply of ADC is provided by the board LDO and diode current is provided by the internal current source (100µA). In this configuration, ADC consumption currents cannot be monitored.
To modify this initial setup, please refer to Section 3.5 and Section 3.7.

To insure a proper start of the Eval Kit, the chronological order as described below should be respected.

2.2.1 Using VC709

1. Install the software as described in section 4 Software Tools.
2. Load the FPGA program (see Section 5 « FPGA Code»).
3. Check that the Heatsink/Fan is properly fixed to the ADC board.
4. Connect the EV12AD5x0x Eval Kit to VC709 Xilinx evaluation board.
5. Connect the power supplies of EV12AD5x0x Eval Kit and FPGA board.
6. Connect the USB cable to connector J20 on EV12AD5x0x board.
7. Connect a RF generator on clock input and preset clock frequency and level (make sure the losses of baluns and filters are taken into account when applying clock level)
8. Turn ON power supply of EV12AD5x0x Eval Kit.
9. Turn ON power supply of VC709 Xilinx Evaluation Board.
10. Turn ON clock generator.
11. Push once on S7 µC_reset and S1 RSTN-DUT buttons
12. Launch the EV12AD5x0x.exe software.
13. On the software,
    - Click on reset then SYNC buttons to initialize ADC (see Section 4 for details)
    - Turn the mode ADC test ramp active.
    - Launch acquisition
14. Check if the acquisition is correct

At this stage main connections are validated.

To perform an acquisition, starting from previous stage:

15. Return to normal mode (Turn OFF Test mode).
16. Connect a RF generator on analog input and preset input signal frequency and level
17. Configure the ADC on the software (Parallel or serial mode, calibration loaded or not…). A SYNC may be necessary.
18. Turn ON the RF generator.
19. Set signal frequency and clock frequency in “Acquisition” tab (see Section 4.9 for details)
20. Launch acquisition.

2.2.2 Using Data Interface Board

If data interface board is used, switch S6 should be set on EXT.

1. Install the software as described in section 4 Software Tools.
2. Check that the Heatsink/Fan is properly fixed to the ADC board.
3. Connect the EV12AD5x0x Eval Kit to Data Interface Board.
4. Connect the power supplies of EV12AD5x0x Eval Kit.
5. Connect the USB cable to connector J20 on EV12AD5x0x board.
6. Connect a RF generator on Clock input and preset clock frequency and level (make sure the losses of baluns and filters are taken into account when applying clock level)
7. Turn ON power supply of EV12AD5x0x Eval Kit.
8. Turn ON clock generator.
9. Push once on S7 µC_reset and S1 RSTN-DUT buttons
10. Launch the EV12AD5x0x.exe software.
11. On the software,
    - Click on reset then SYNC buttons to initialize ADC (see Section 4 for details)
    - Turn the mode ADC test ramp active.
    - Launch acquisition
12. Check if the acquisition is correct

At this stage main connections are validated.

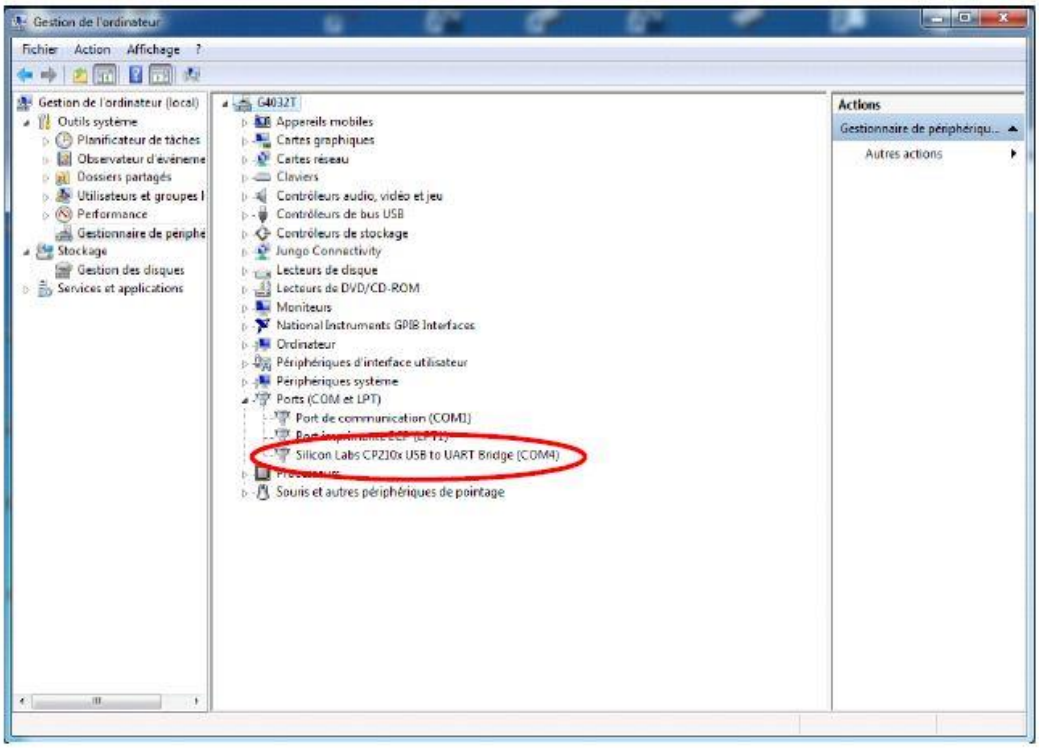
To perform an acquisition, starting from previous stage:

13. Return to normal mode (Turn OFF Test mode).
14. Connect a RF generator on Analog input and preset input signal frequency and level
15. Configure the ADC on the software (Parallel or serial mode, calibration loaded or not…). A SYNC may be necessary.
16. Turn ON the RF generator.
17. Launch acquisition.

2.3 Troubleshooting

2.3.1 Installation

Check that you own rights to write in the directory (administrator rights).
Check for the available disk space.
Check that the USB port is free and properly configured. It should appear in the device manager as shown below.



2.3.2 Start-up procedure

Verify that the board is properly configured as described in Section 2.1.

Check that boards are properly supplied.

Check if the Xilinx FPGA evaluation board VC709 is properly configured with correct software.
If LED4 on VC 709 is blinking regularly then the FPGA program has been correctly loaded.
Check if EV12AD5x0x Eval Kit is properly plugged into FPGA connector and its LED3 is ON. It detects the presence of the VC709 board. See Figure 2-1 below.

Check if USB connector is properly plugged on J20.

Figure 2-1. LED3 that indicates VC709 board connection

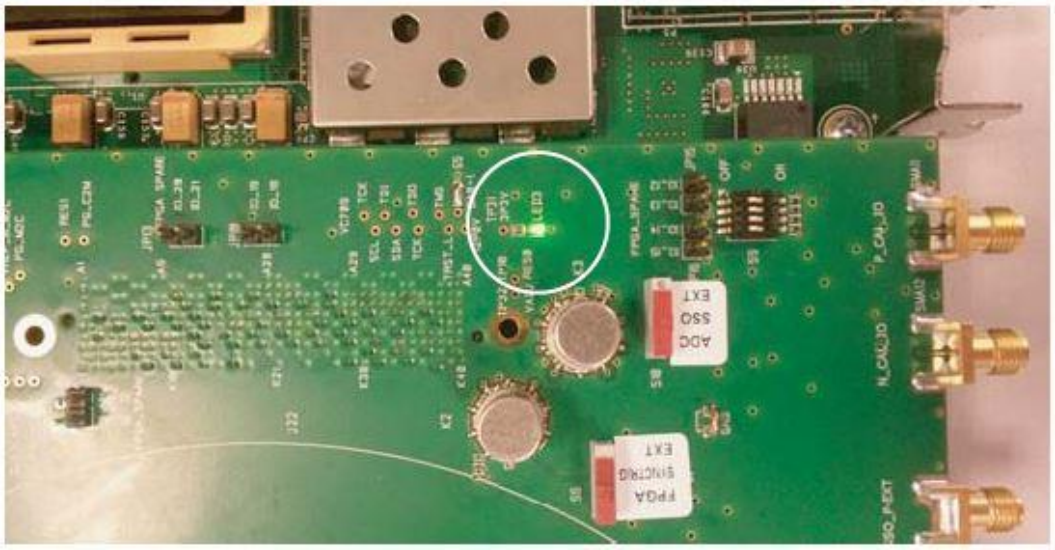


Figure 2-2. Software output if no FPGA board detected

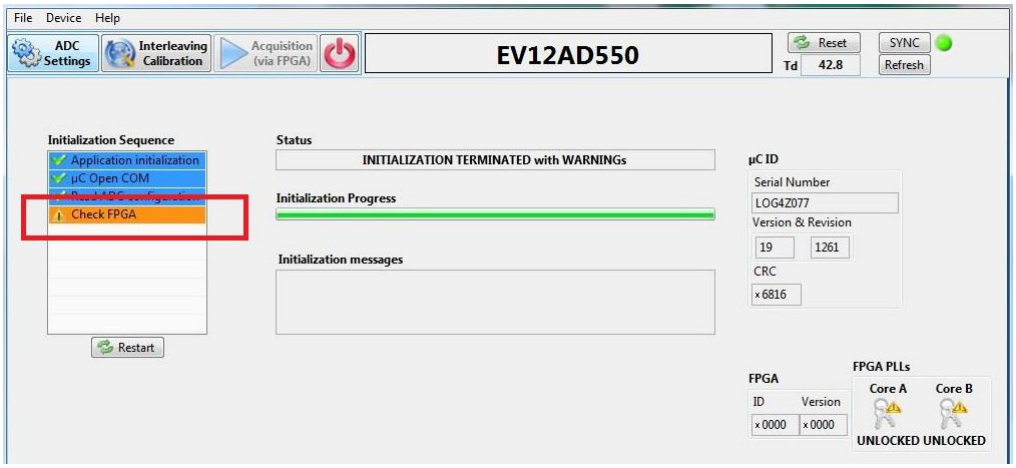
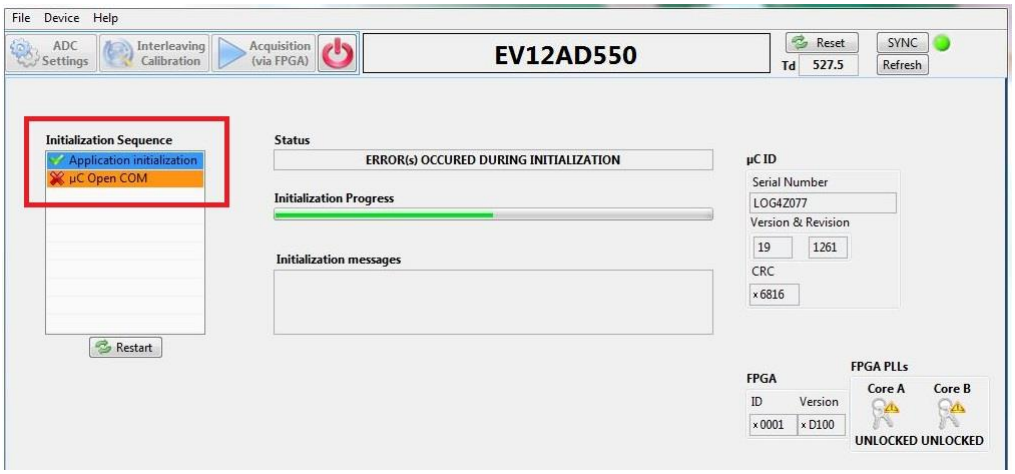


Figure 2-3. Software output if no microcontroller detected



2.3.3 Measurements

Check if EV12AD5x0x is properly configured in normal mode.

- Check if test mode is OFF.
- Check if acquisition mode is correctly configured.

In case of doubt, click on RESET and re-configure ADC.

If no windowing is used and signal is not coherent, reconstructed signal of Figure 2-4 is obtained.

Figure 2-4. Reconstructed signal without windowing and not coherent signal

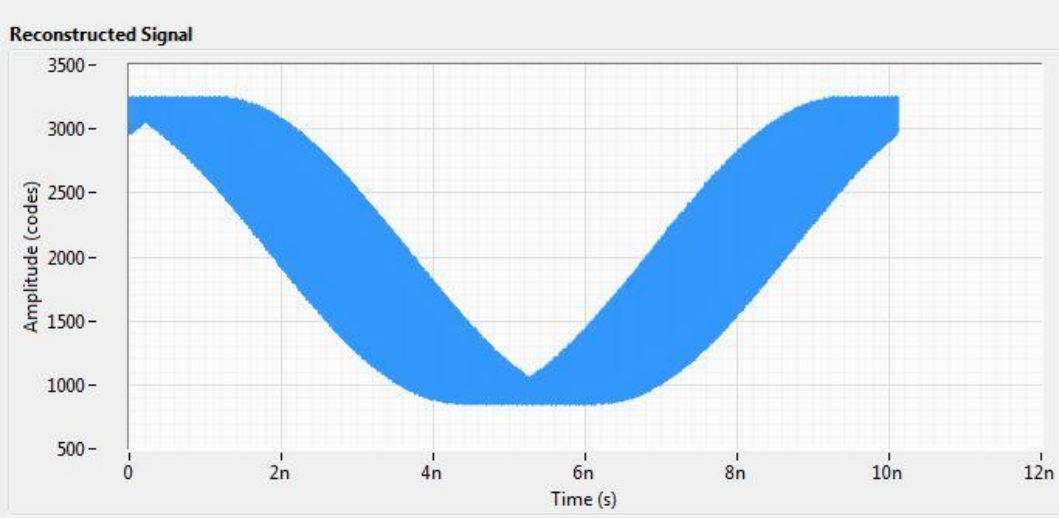
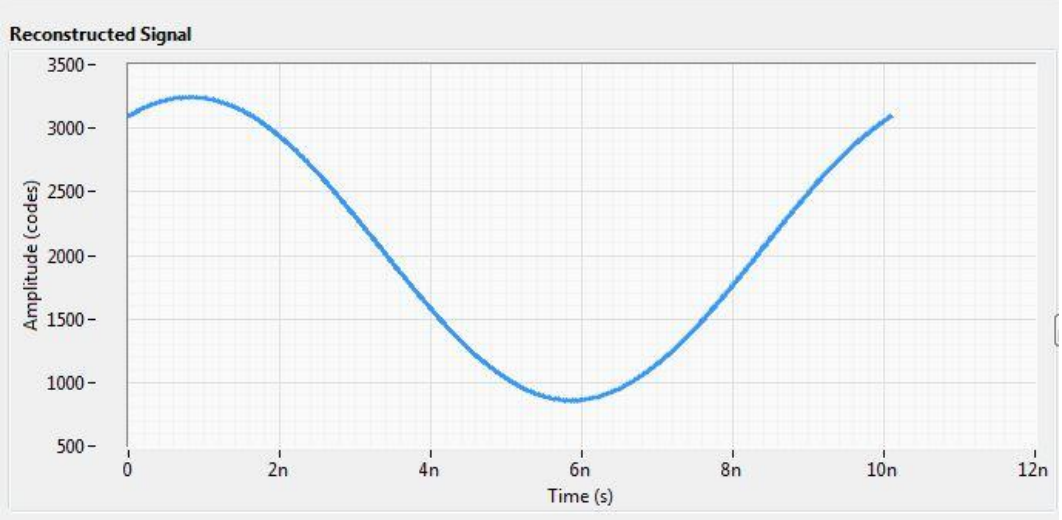


Figure 2-5. Reconstructed signal with windowing or coherent signal



Check that the junction temperature of EV12AD5x0x is lower than 110°C and that heatsink is properly connected.
Check EV12AD5x0x board connection to FPGA or data interface board.
Verify that board is properly configured as described in Section 2.1.
Check if all RF cables are properly connected to CLK and inputs of EV12AD5x0x board.
Make sure applied levels of clock and input signals are high enough taking into account the losses of filters and baluns.

Section 3. Main Functions

3.1 VC709 board or Data Interface board

Our EK can be connected either to the Data Interface Board or VC709 board.

Figure 3-1. Data Interface Board

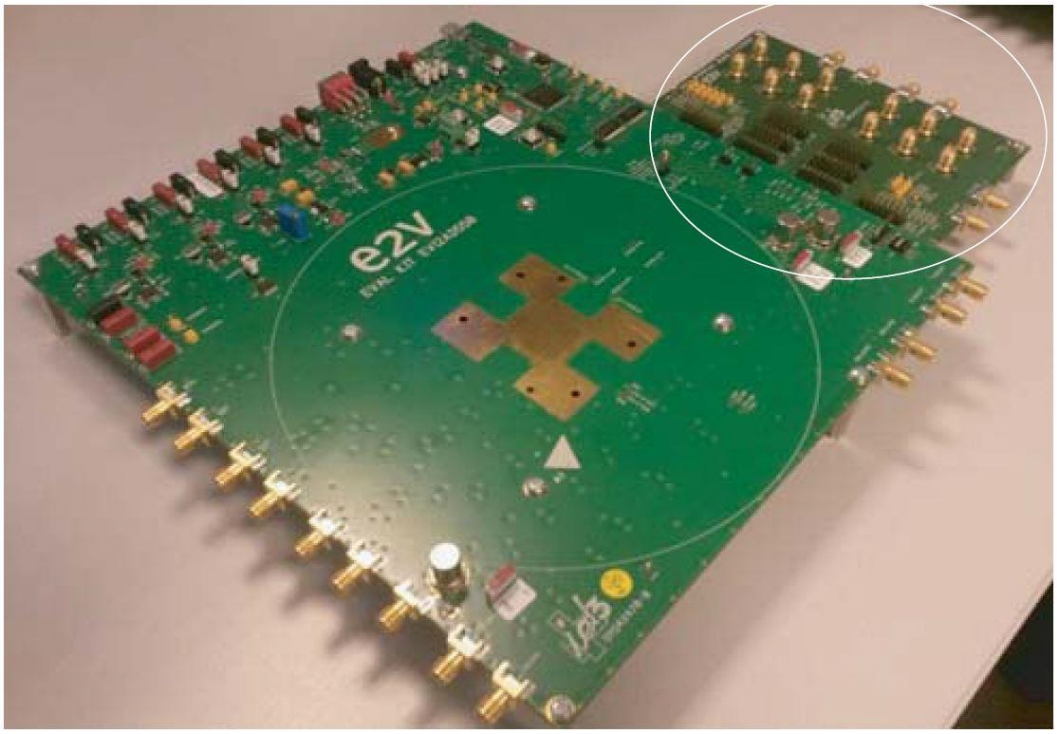


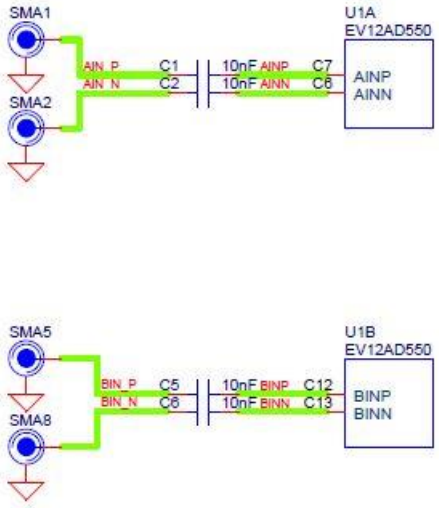
Figure 3-2. VC709 Board

To change configuration, make sure that all the evaluation boards are turned off and then disconnect the boards.

3.2 Analog input signal

The user needs to provide an analog signal at the input. This signal is digitized by the ADC. It is mandatory to drive the ADC by a differential input signal.

Figure 3-3. Analog input schematics

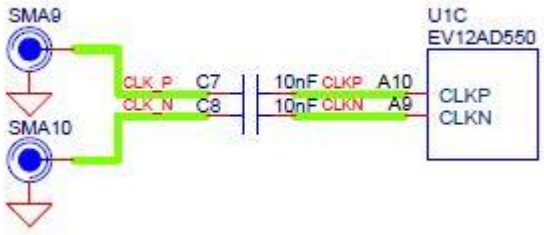


Analog inputs A or B can be used in DC configuration mode by replacing C1, C2 and C5, C6 by a 0Ω resistor.

3.3 ADC Clock input signal

The user needs to provide a differential analog clock.

Figure 3-4. Clock input schematics



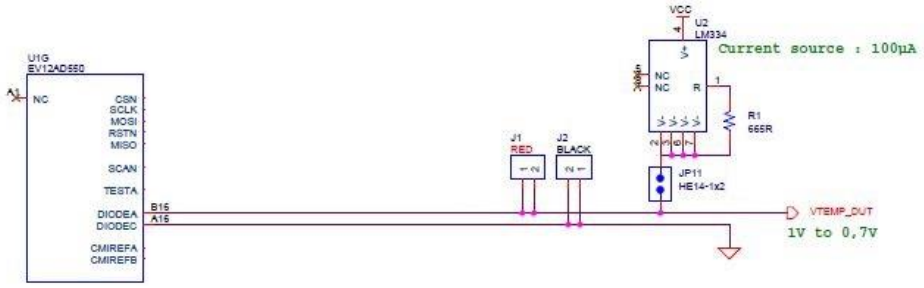
3.4 Control of ADC settings

The Graphical User Interface allows complete monitoring and control of all the settings of EV12AD5x0x such as Gain, Offset, Phase and Test Mode.
Please see Section 4.5 Operating Modes and refer to datasheet EV12AD5x0x for more information.

3.5 ADC Junction Temperature Monitoring

ADC junction temperature can be monitored by temperature sensor from component U2 (LM334). The configuration is done for 100µA; it can be changed via R1.
By default, this 100µA current source is used as JP11 is plugged on board.

Figure 3-5. Junction temperature monitoring



ADC junction temperature can be displayed on the PC via the GUI.
The Eval Kit provides an external heat sink with internal fan.

The use of the internal current source is not mandatory. The user can monitor Vdiode through a multimeter plugged on J1 and J2 connectors. Then the user must take 2 precautions:

- disconnect J11
- check which current is delivered by the multimeter and modify the temperature coefficients (See Section 4.5.2 and Figure 4-18)

3.6 SYNC

The EV12AD5x0x requires a SYNC signal when the internal configuration is changed.

3.6.1 Nominal case

If the board is in the initial configuration as described in Section 2.1 then:

- When VC709 is connected (§2.2.1), SYNC is done by the FPGA
- When Data Interface Board is connected (§2.2.2), SYNC is done by the µC.

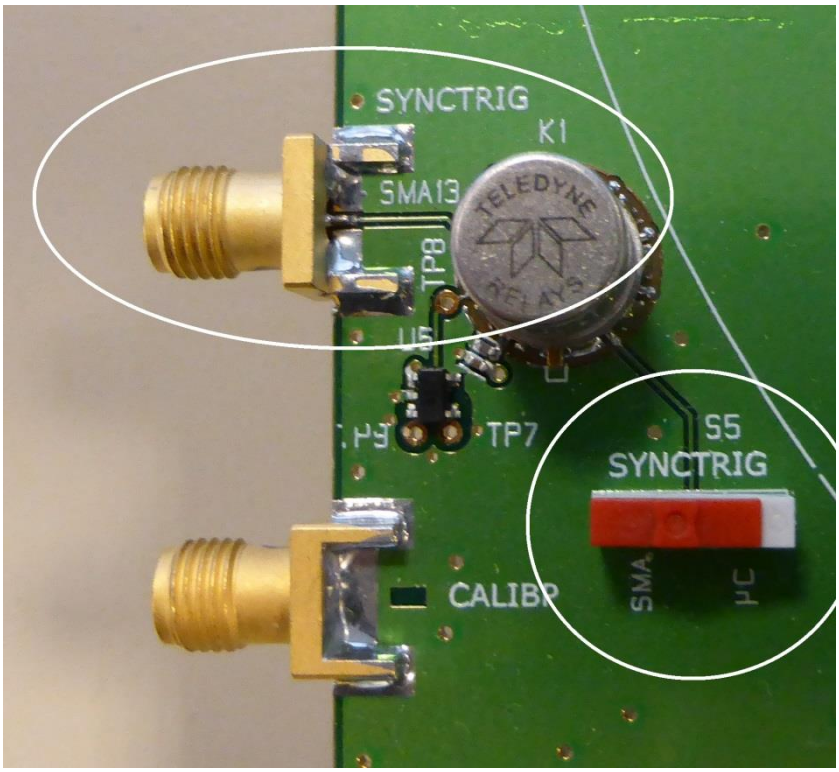
3.6.2 Advanced case

The user has other possibilities to do a SYNC.

3.6.2.1 SYNC done by SYNC TRIG on ADC board

In this case, SMA13 is used to input the SYNC signal.
Switch S5 must be set on SMA.
Refer to the datasheet to identify the input pulse signal to be applied.

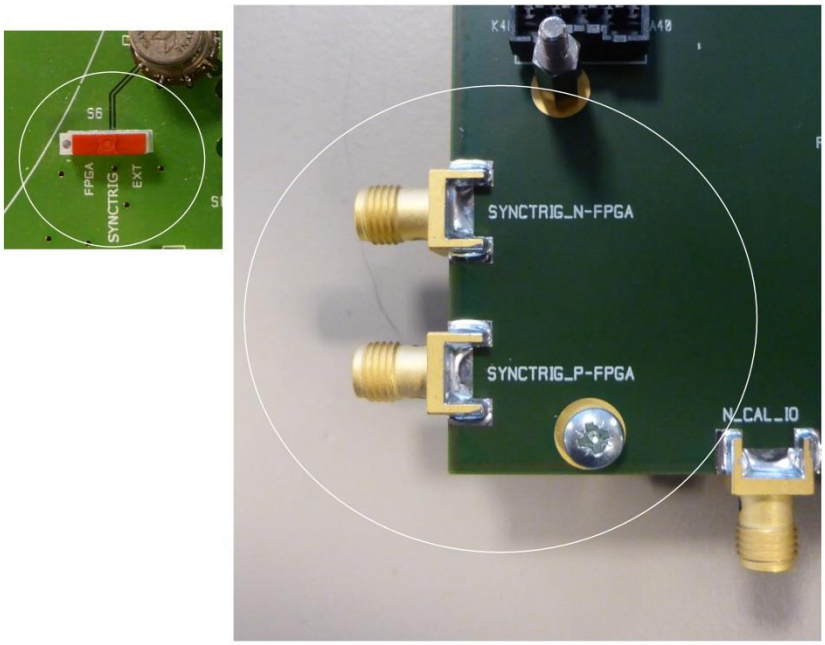
Figure 3-6. Switch S5; SMA13 on board



3.6.2.2 SYNC done by SYNC TRIG on Data Interface Board

In this case, SMA2 and SMA4 of the Data Interface Board are used to input the SYNC signal.
Switch S6 must be set on EXT.
Refer to the datasheet to identify the input pulse signal to be applied.

Figure 3-7. Switch S6 on ADC board; SMA2 and SMA4 on Data interface board

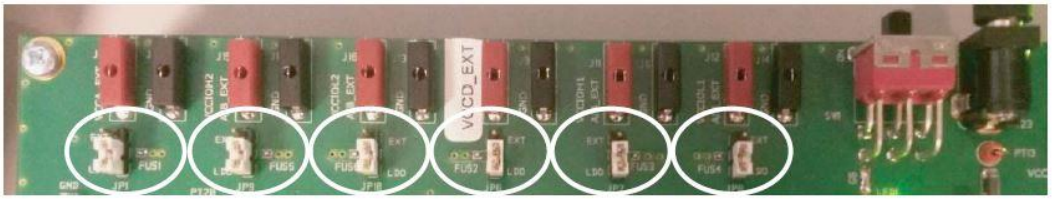


3.7 DC/DC converter

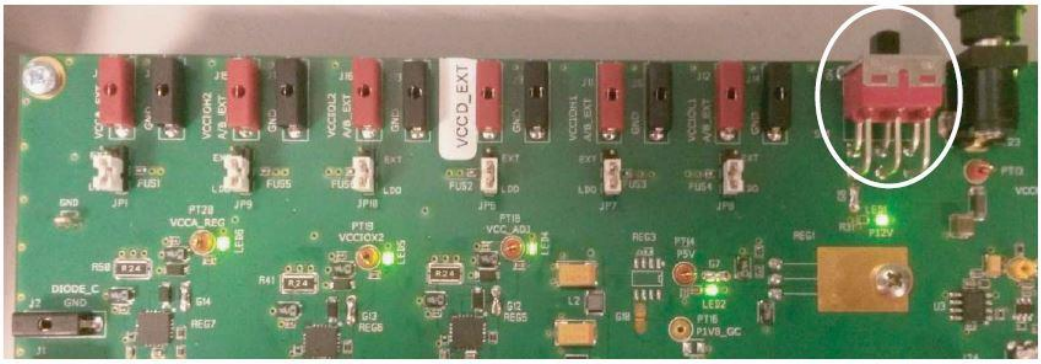
The user has the possibility to use on-board LDO or external power supply.
The 12V jack must be connected whatever external or internal supply option is selected.

3.7.1 To use on-board LDO

1. Connect the 12V Jack
2. Put the jumpers on LDO label (JP1, JP9, JP10, JP6, JP7, JP8)



3. Switch on SW1



4. All the LEDs (LED1, LED2, LED4, LED5 and LED6) must be lighted on.

If the user chooses the solution with the 12V jack, the user can monitor the power supply of VCCD and VCCIOx1 between 2.5V and 3.4V thanks to R40.

Figure 3-8. 2.5V or 3.4V schematics

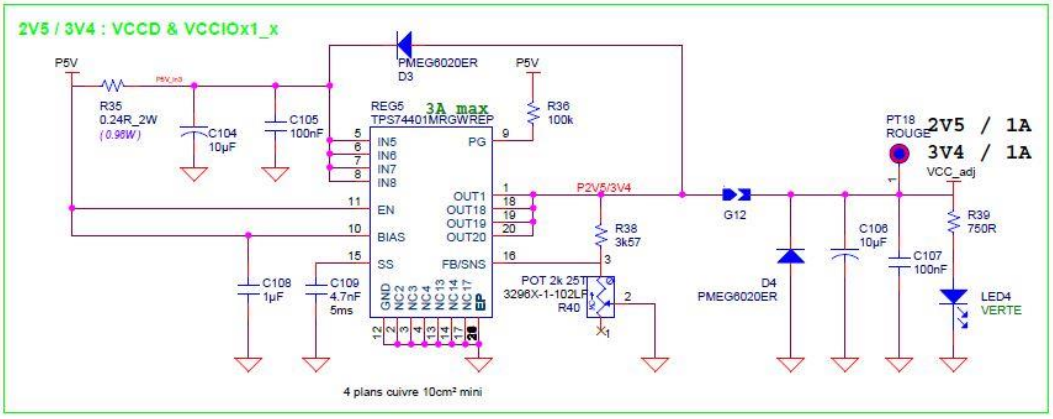
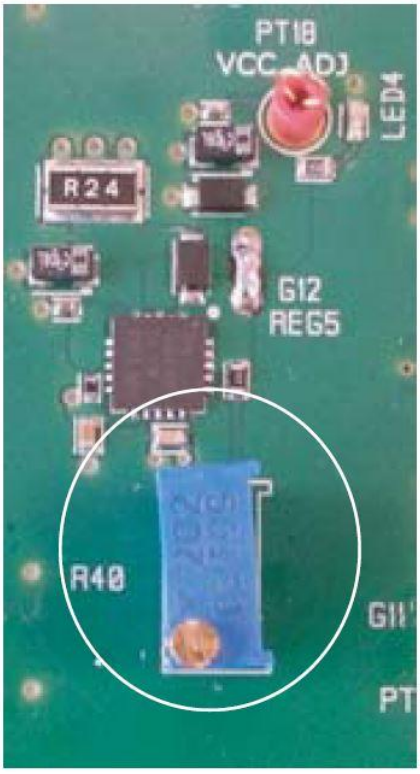
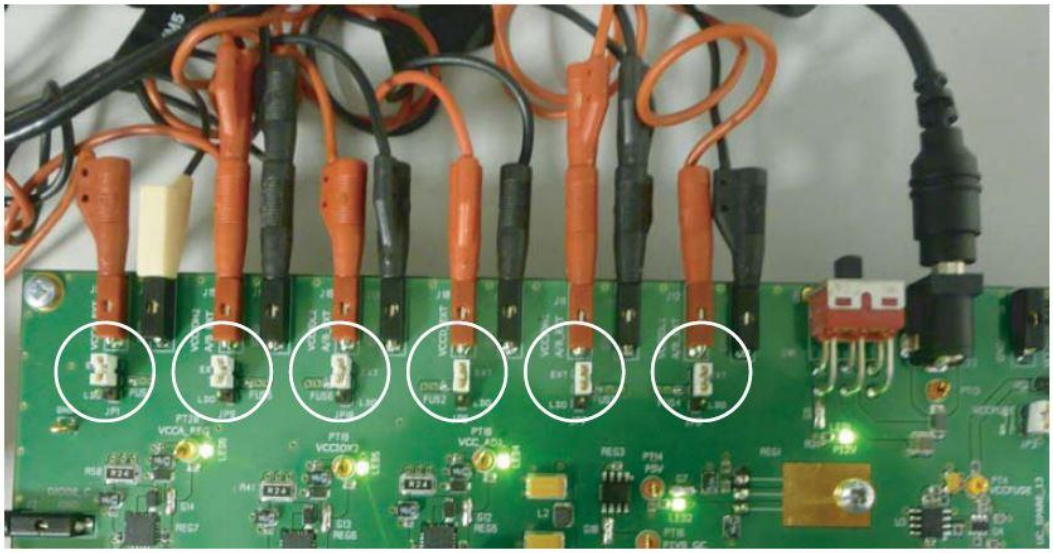


Figure 3-9. 2.5V or 3.4V on evaluation board

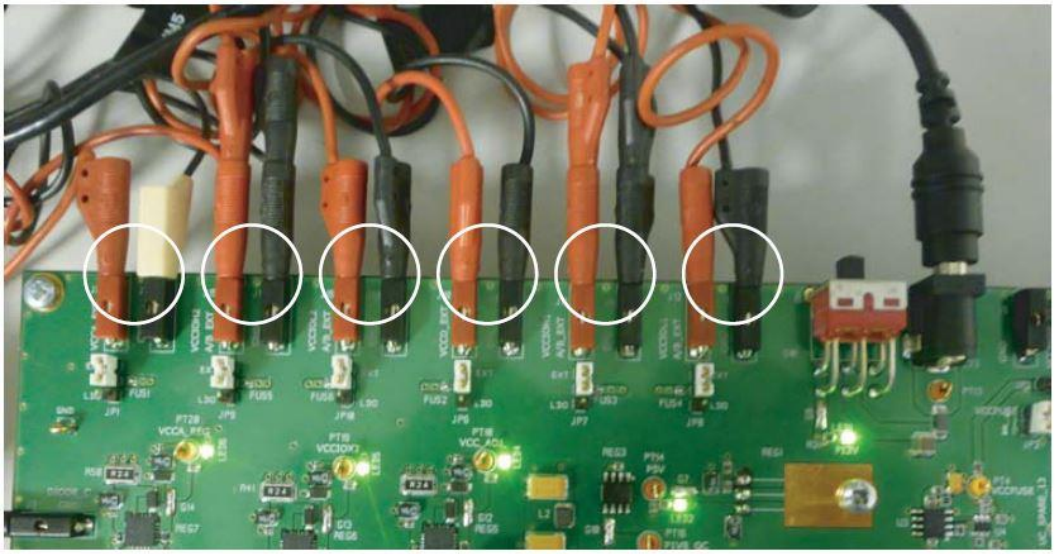


3.7.2 To use external power supplies

1. Connect the 12V Jack
2. Put the jumpers on EXT label (JP1, JP9, JP10, JP6, JP7, JP8)



3. Connect the external supplies to the board



4. Switch on SW1
5. Switch on external supplies
6. All the LEDS (LED1, LED2, LED4, LED5 and LED6) must be lighted on.

Note that the chronological order in which power supplies are set ON has no effect on the ADC behavior.

3.8 SSO signal

SSO signal can be provided via the ADC or through the two SMA connectors: SSO_N-EXT and SSO_P-EXT.
The selection is done manually with a switch S10.

Figure 3-10. SSO schematics

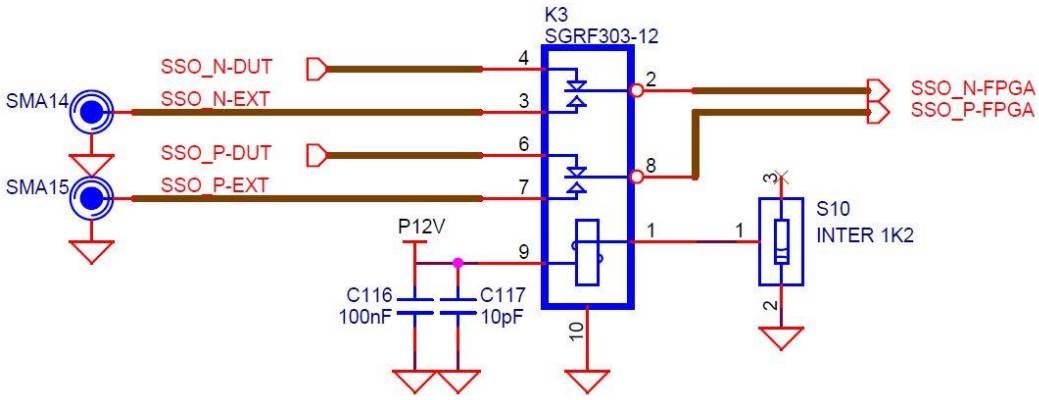
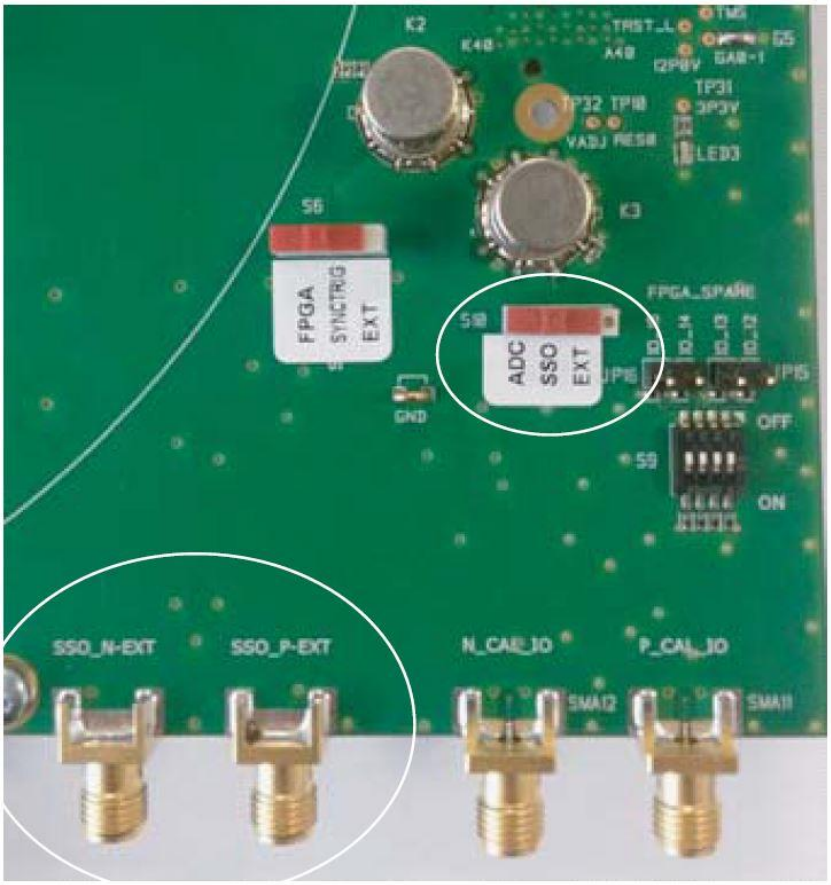


Figure 3-11. Switch S10 on evaluation board

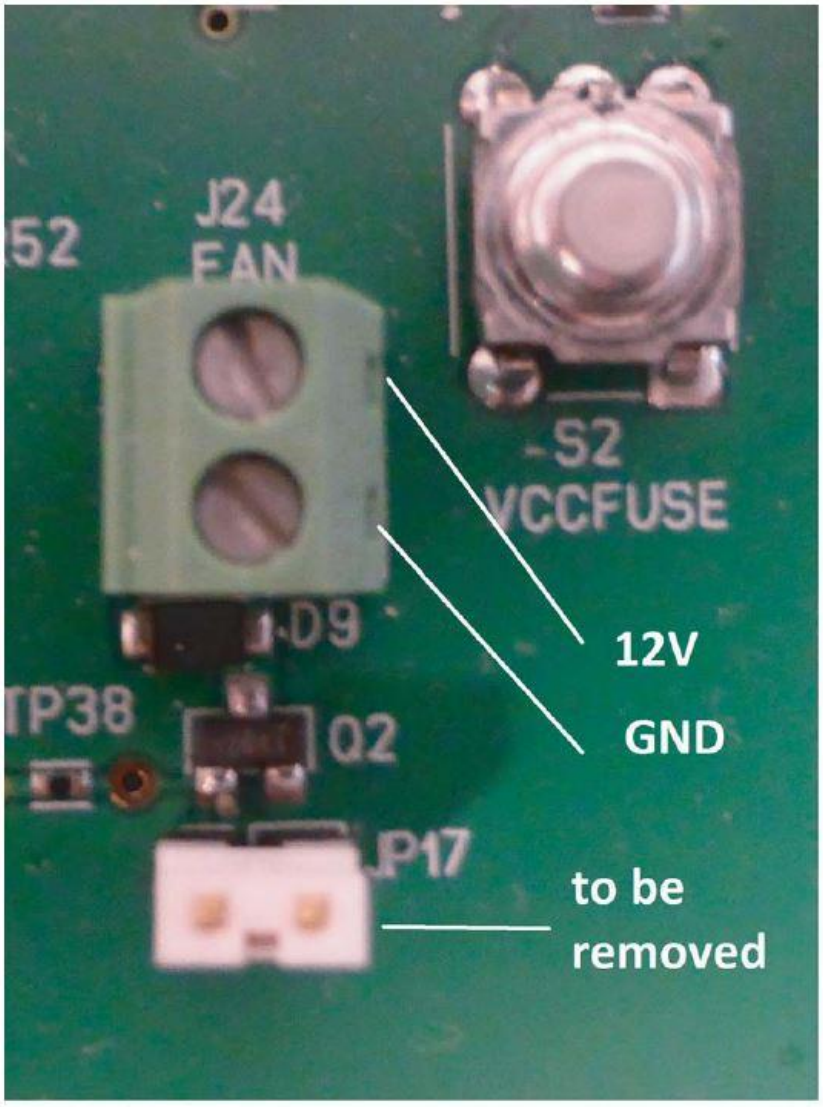


Refer to the datasheet to get details on SSO function.

3.9 Fan power supply

The fan can be powered through the 12V jack of the evaluation board.
To do so, the fan cables must be connected to the [J24 fan] as shown on figure below. JP17 must be removed.

Figure 3-12. Fan power supply



Section 4. Software Tools

4.1 Overview

The Eval Kit board needs three different kinds of software tools:

- FPGA Software (do not consider this point if you use Data Interface board)

The Eval Kit board can be plugged with XILINX VIRTEX 7 evaluation board EK-V6-VC709-G (http://www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html).
Teledyne e2v provides FPGA program to be used with EV12AD5x0x Eval Kit.

- User Interface Software

The User Interface software is a Labview compiled graphical interface that does not require a license to run on Window 7/XP.
The software uses intuitive push-buttons and pop-up menus to configure the ADC and recover the ADC samples.
Revision 1.0.1 is the GUI version for EV12AD5x0A.
Revision 1.2.5 is the GUI version for EV12AD5x0B.

4.2 Configuration

The advised configuration for Windows 7 is:

- PC with core i3 or equivalent
- Memory of at least 1GB
- Office 2010 (for data recovering)

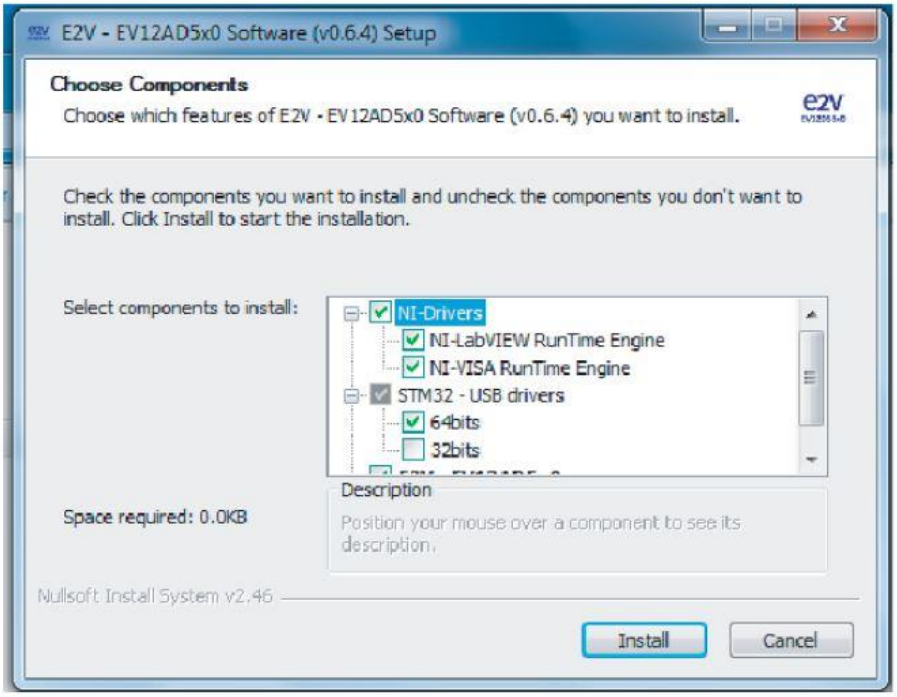
Note: The GUI is not compatible with Office 2003

4.3 User interface installation

Install the DUAL ADC Eval Kit application on your computer by launching the install.exe (please make sur proper GUI version is installed: 1.0.1 for EV12AD5x0A, 1.2.5 for EV12AD5x0B).
Installation is intuitive. Simplified guide with main steps follows. Others windows than the ones described below can pop-up. Then clicking on “Next” should be done.

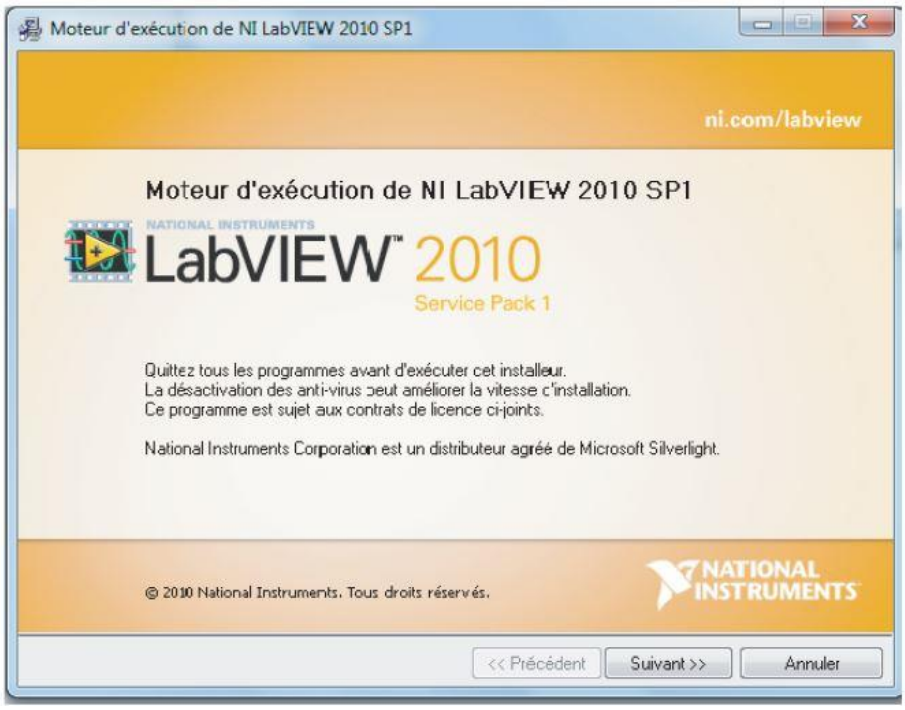
- On first window, select the applications you want to install.

Figure 4-1. Selection



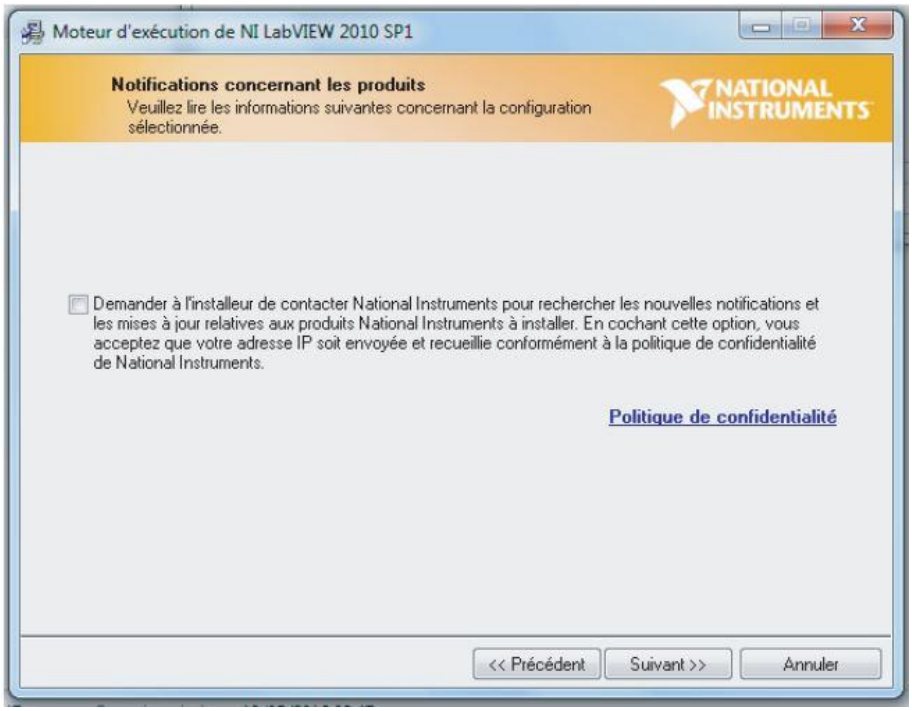
- On each following window that pops up, click on “Next”.

Figure 4-2. Labview installation start



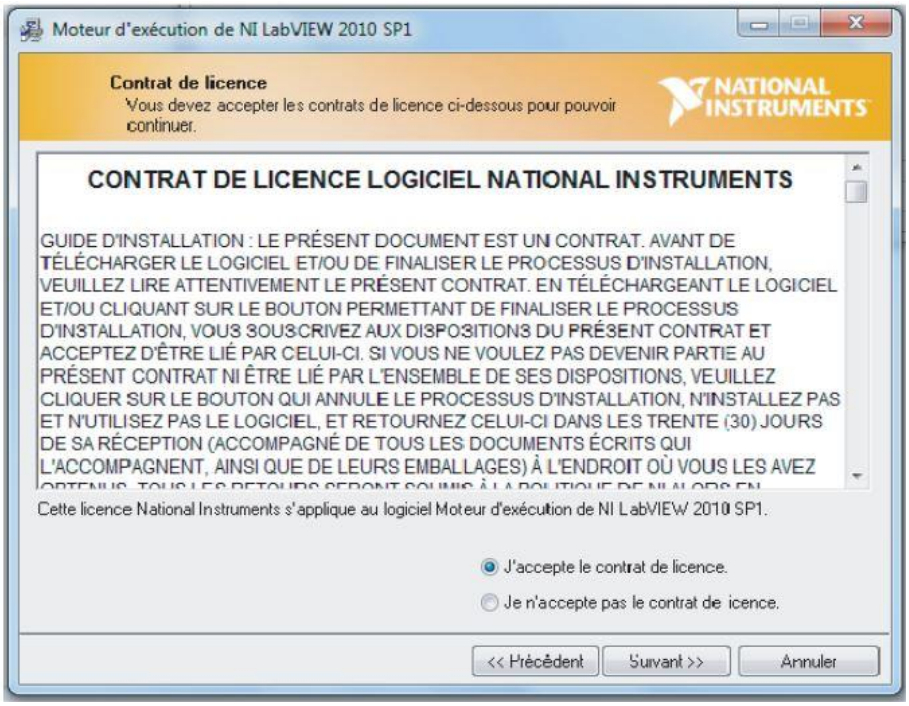
- On page shown on Figure 4-3, please uncheck the box.

Figure 4-3. Labview notifications



- Please accept the licenses when suggested. See Figure 4-4.

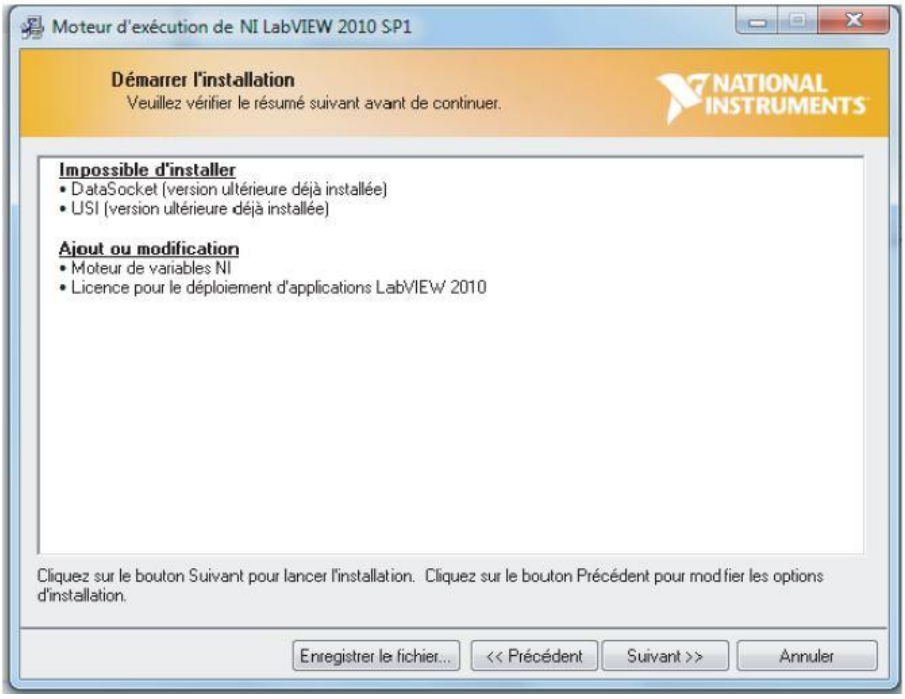
Figure 4-4. Licenses



- The tool provides the list of applications which are already installed and those which are not. See Figure 4-5.

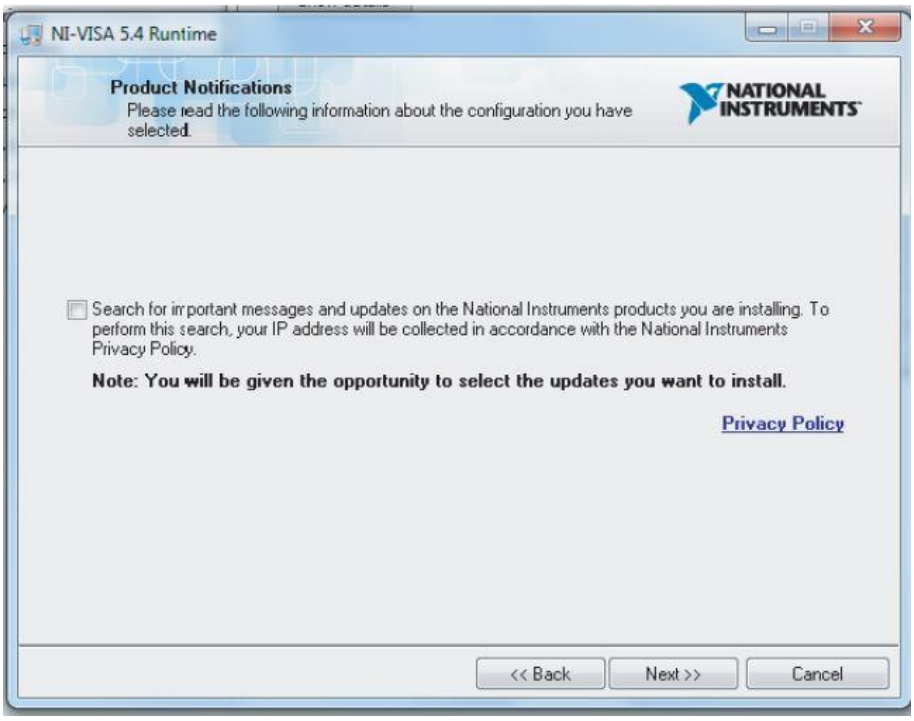
Just click on “Next”.

Figure 4-5. List of applications



- On NI window, please uncheck the box.

Figure 4-6. NI product notifications

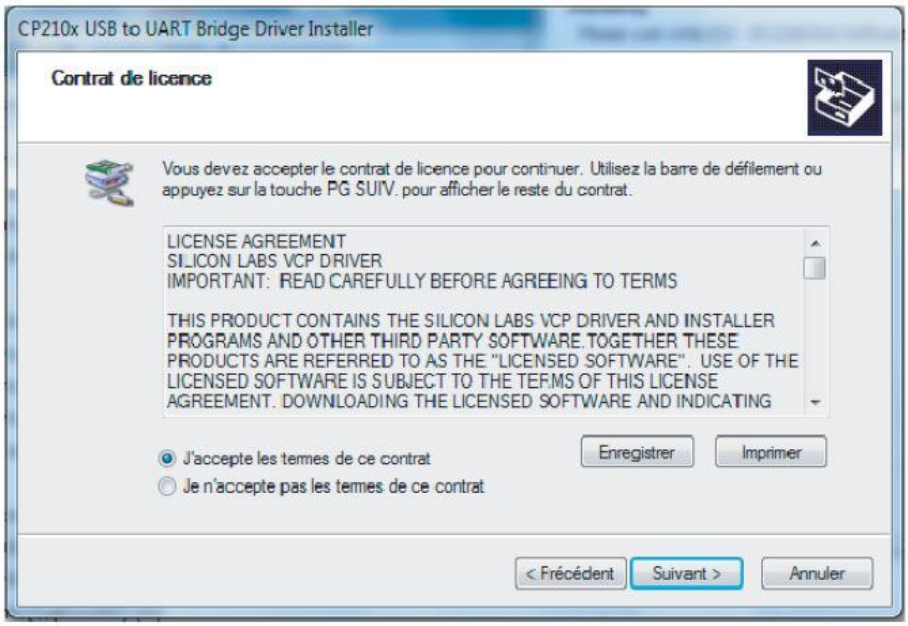


- Installation of VSB driver proceeds the same way.

Figure 4-7. USB driver installation

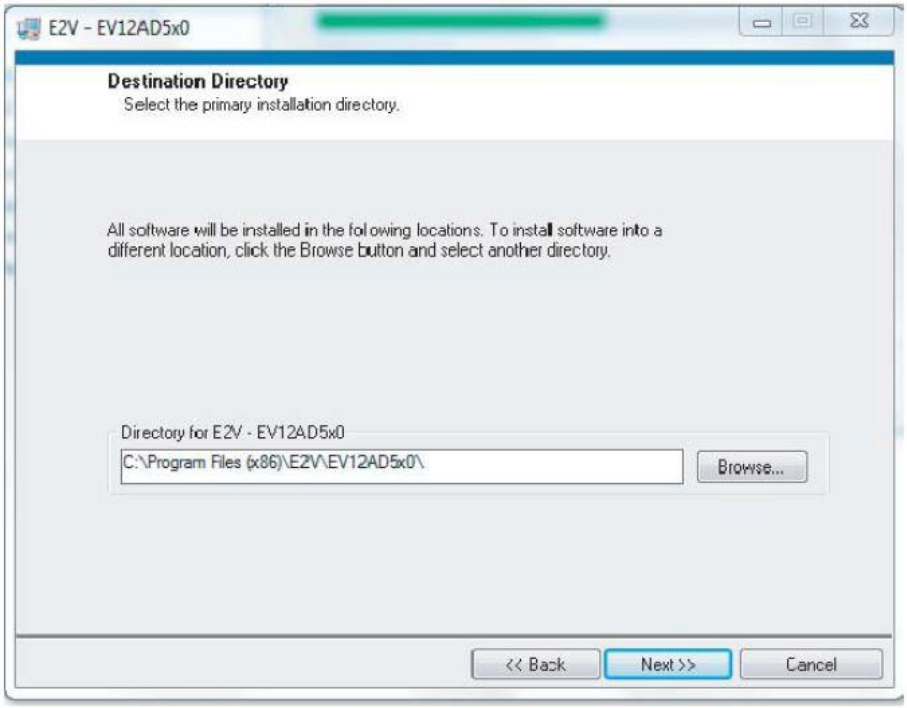
- Please accept licenses as done previously.

Figure 4-8. USB driver license



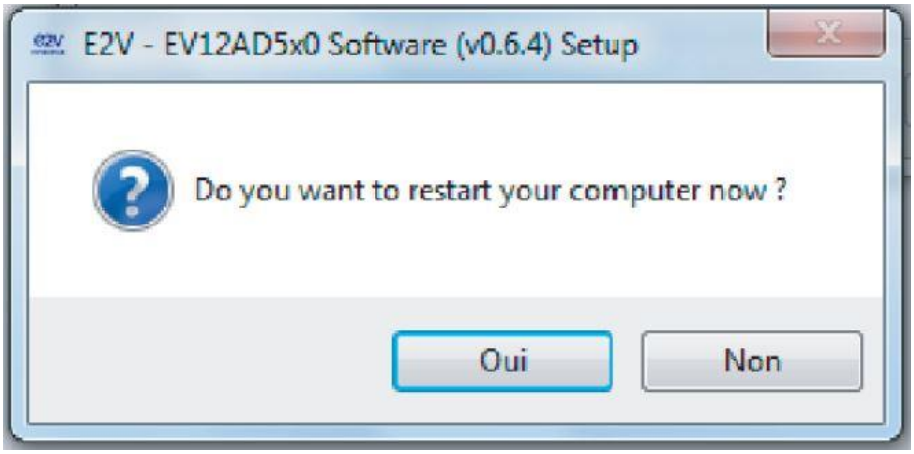
- Select where you wish application to be registered (Default directory is recommended).

Figure 4-9. Destination directory



- At the end, restart your computer.

Figure 4-10. End of application



4.4 USB driver installation

After installation, EV12AD5x0x Eval Kit can be powered up and connected to a PC with USB cable.

At the first connection a USB driver installation will be launched.

The installation is normally fully automatic. If it is not launched automatically, please install with CP210x VCPInstaller_x64.exe or CP210x VCPInstaller_x86.exe which are available on CD / USB key.

4.5 Operating modes

The EV12AD5x0x software included with the Eval Kit provides a Graphical User Interface to configure the ADC.

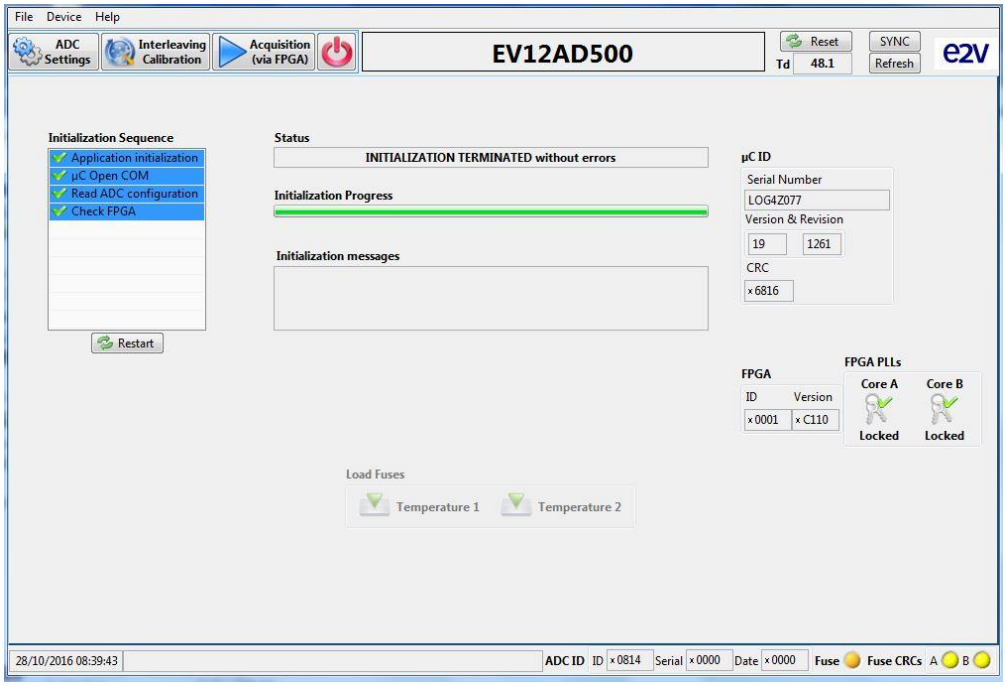
Push buttons, popup menus and capture windows allows easy:

1. ADC Settings
2. Interleaving Calibration
3. FPGA Post-Processing
4. Acquisition

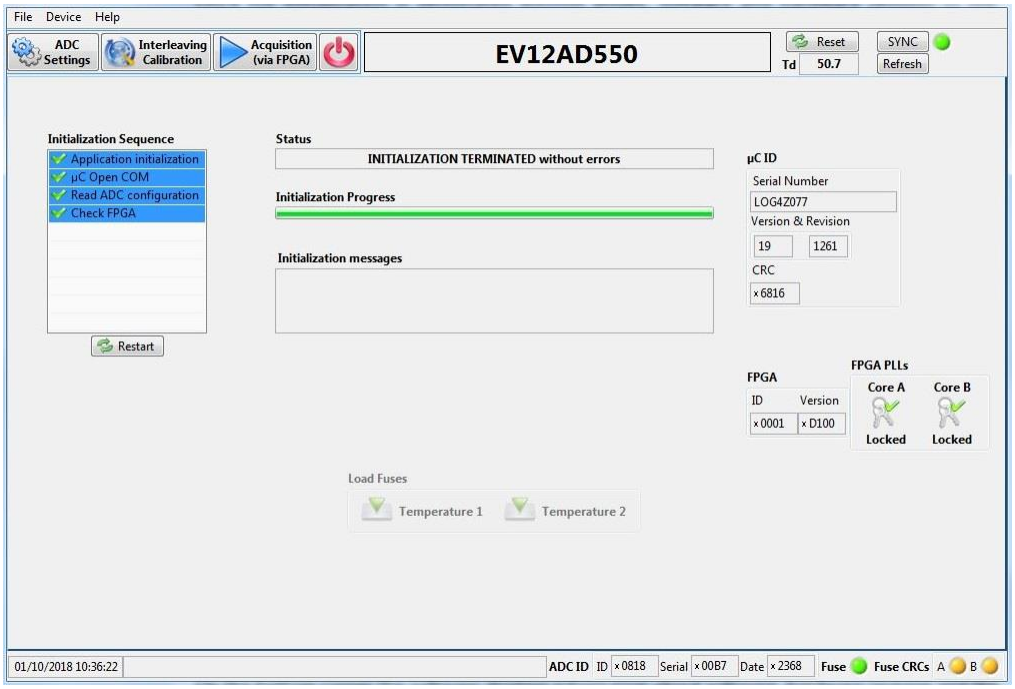
After the SW is launched, first window is the “login page” as shown on Figure 4.11.
Once the initialization is terminated without errors, software and hardware revision of the microcontroller and the FPGA code appear on the right.

Figure 4-11. Login page

On AD5x0A (GUI 1.0.1)



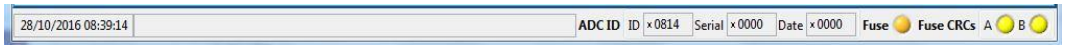
On AD5x0B (GUI 1.2.5)



On the bottom corner the software displays information about software, hardware revision and the component state:

- Date
- ADC ID
- ADC Serial
- ADC Date
- Fuse
- Fuse CRCs

Figure 4-12. Component state



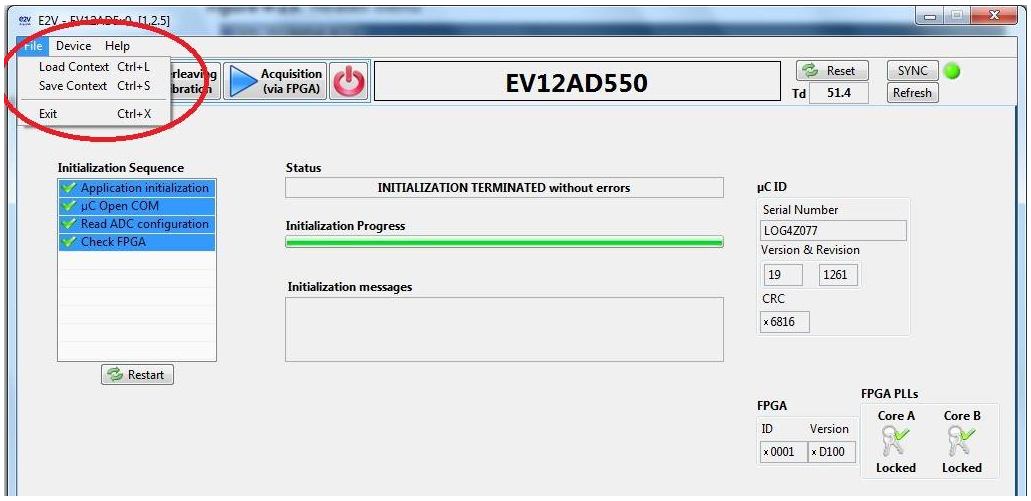
On the top of the window, there are 3 menus:

1. File
2. Device
3. Help

Figure 4-13. Header menu

4.5.1 File

Figure 4-14. File menu



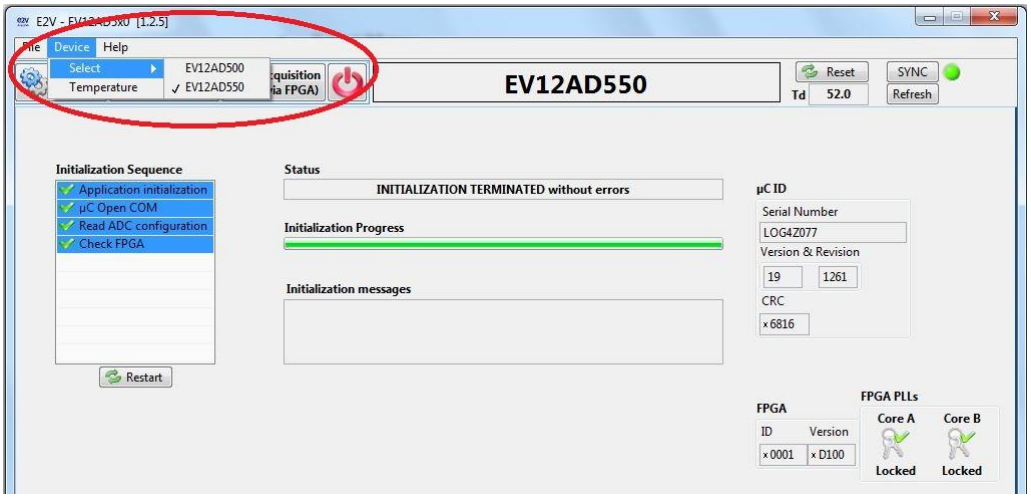
It is possible to save the context of the Eval Kit for later uses. Then it can be reloaded.
Settings and configurations of the ADC are saved (mode, calibrations …) but the acquisition parameters filled in 'Acquisition sheet' are not saved.

4.5.2 Device

- Select Menu:

This menu is very important as the choice impacts the visible features in the GUI. You have to correctly choose the device you want to measure: EV12AD500x or EV12AD550x.

Figure 4-15. Device choice menu - Select



Note that device choice menu can be modified only when login page is selected. On any other page "device select" is disabled.
By default, AD550x is selected.

- Temperature Menu:

Figure 4-16. Device choice menu - Temperature

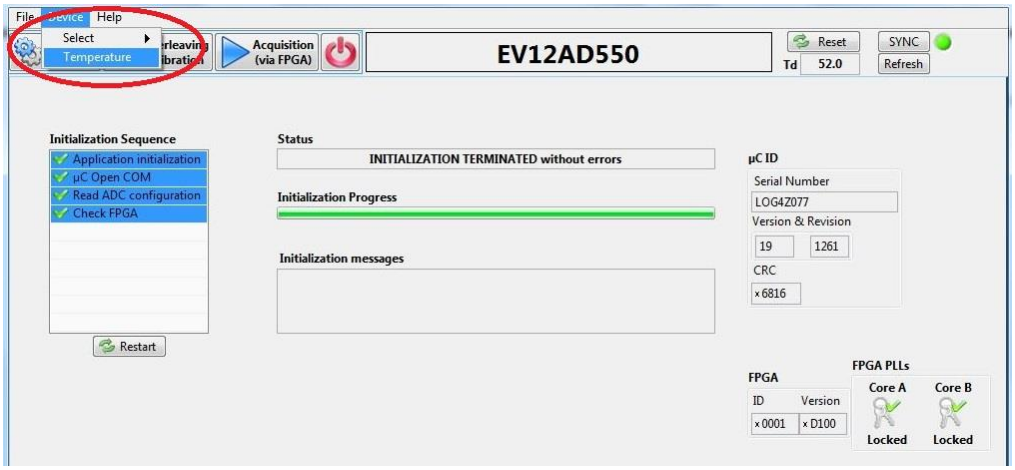


Figure 4-17. Temperature coefficients for 1 mA temperature sensor

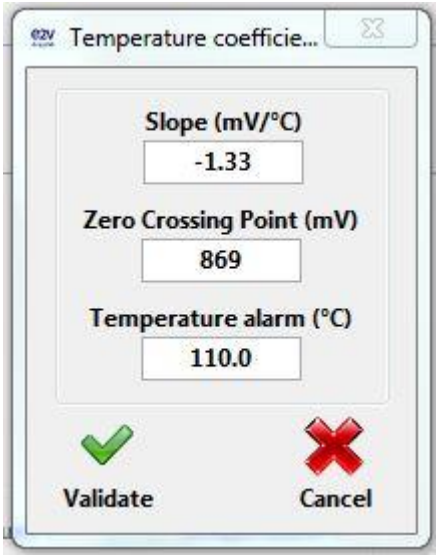
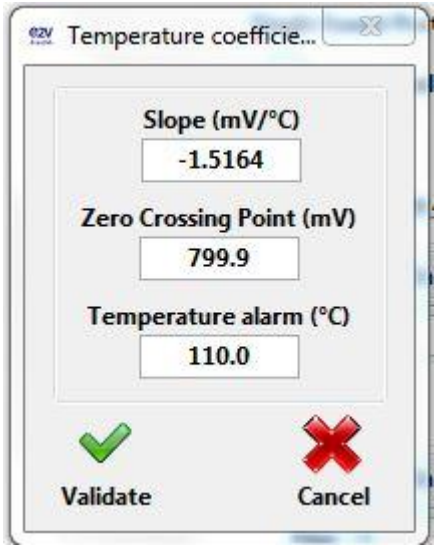


Figure 4-18. Temperature coefficients for 100µA temperature sensor



Slope and Zero Crossing Point are indicated by Teledyne e2v in the datasheet (die junction temperature monitoring diode). Theses indications allow the GUI to give the diode temperature of the component.

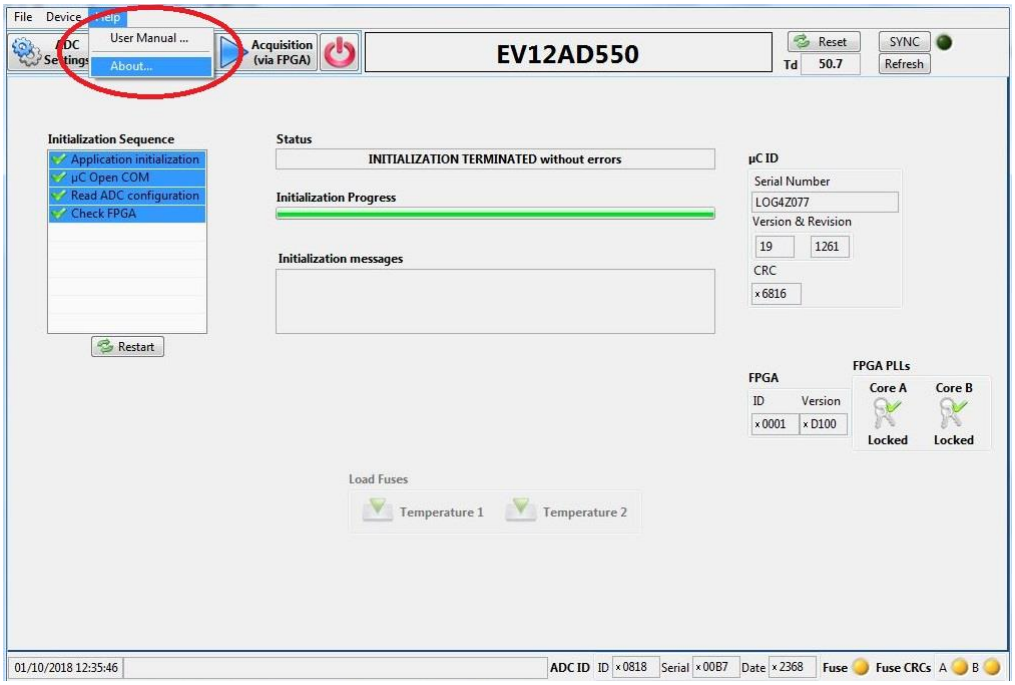
Temperature alarm allows the user to indicate a temperature from which it will flash in red on the main screen.

By default, values with 100µA are registered in the GUI.

Note that the coefficients given above are valid for AD5x0xA products and will be re-evaluated on second run.

4.5.3 Help

Figure 4-19. Help menu



By clicking on ‘User Manual’, the user guide will open.
By clicking on ‘About’, our logo will appear.

4.5.4 Fuses & Stored calibration

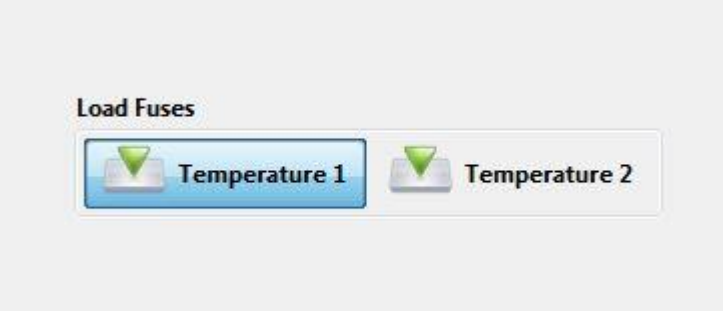
Two calibrations set are stored and fused in the device:

- Calibration 1 done at ambient temperature
- Calibration 2 done at hot temperature

Refer to datasheet to select the best calibration set versus temperature.

Figure 4-20. Component state bar when calibrations are fused

Figure 4-21. Calibration set selection



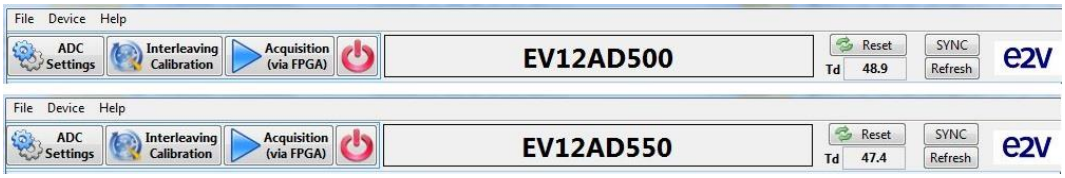
The user needs to click on any of the calibration set to get it loaded in the device.

1157F–BDC–10/18

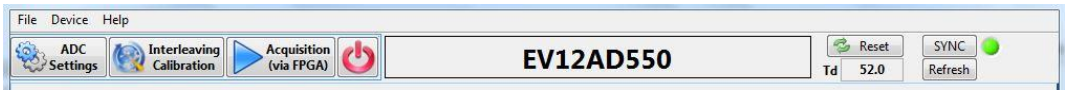
4.6 Control display

Figure 4-22. Control display

On AD5x0A (GUI 1.0.1)



On AD5x0B (GUI 1.2.5)



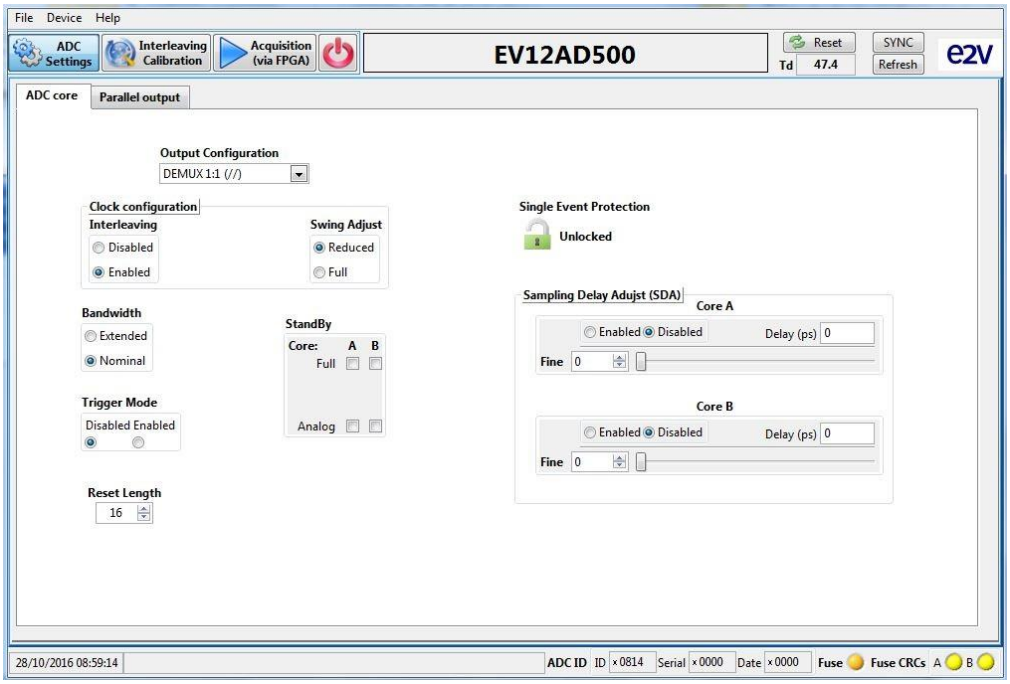
- Reset: A reset is sent to the ADC, the FPGA and the microcontroller.
- Refresh: Data on the active screens are refreshed.
- Td: The diode temperature is displayed in °C. This indicator may flash if the target temperature is reached.
- SYNC: A SYNC is sent to the ADC. On AD5x0B, the lamp closed to SYNC helps to validate either it has been taken into account or not.

4.7 ADC settings

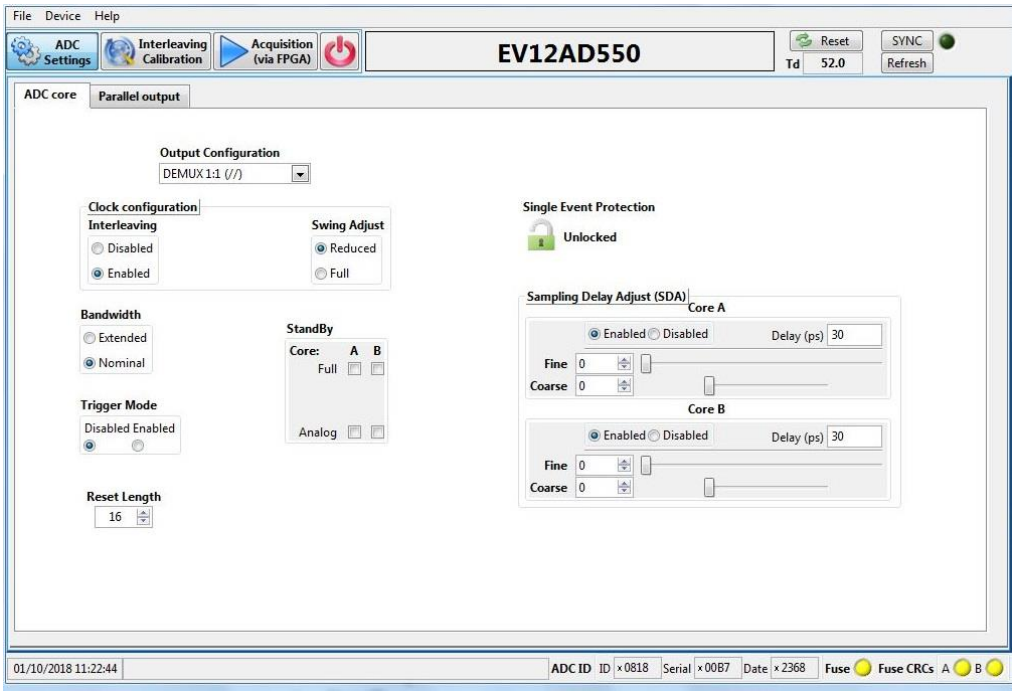
4.7.1 ADC core

Figure 4-23. User interface Eval Kit – ADC core

On AD5x0A (GUI 1.0.1)



On AD5x0B (GUI 1.2.5)



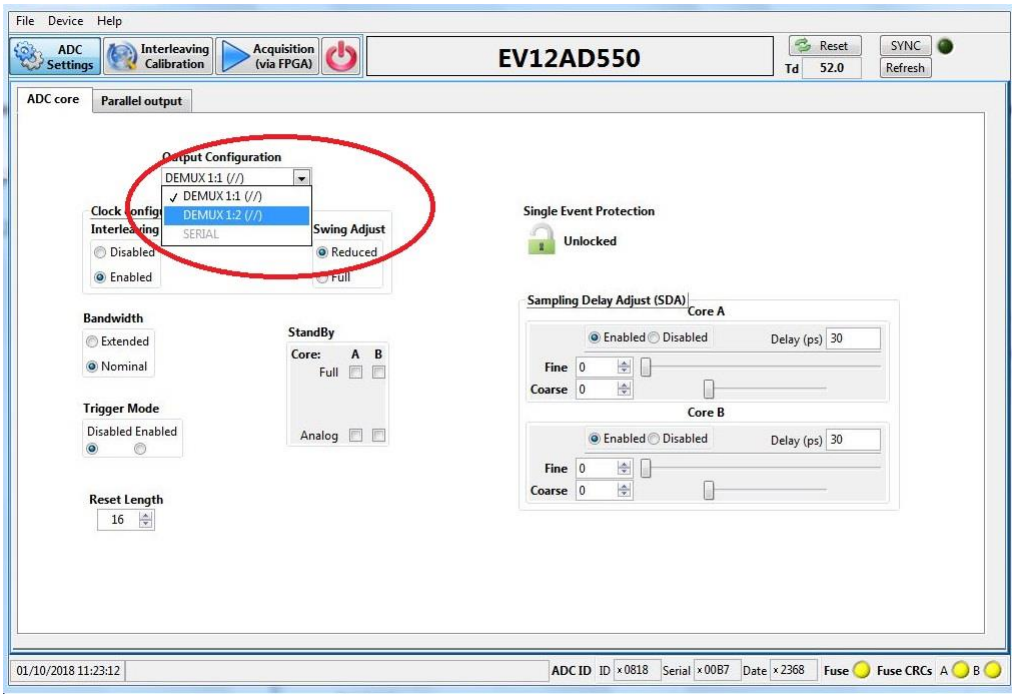
In this window "ADC Core", the following functions are available:

- Output Configuration
- Clock Configuration
- Bandwidth
- Trigger Mode
- Reset Length
- StandBy
- Sampling Delay Adjust (SDA)
- Single Event Protection

4.7.1.1 Output configuration

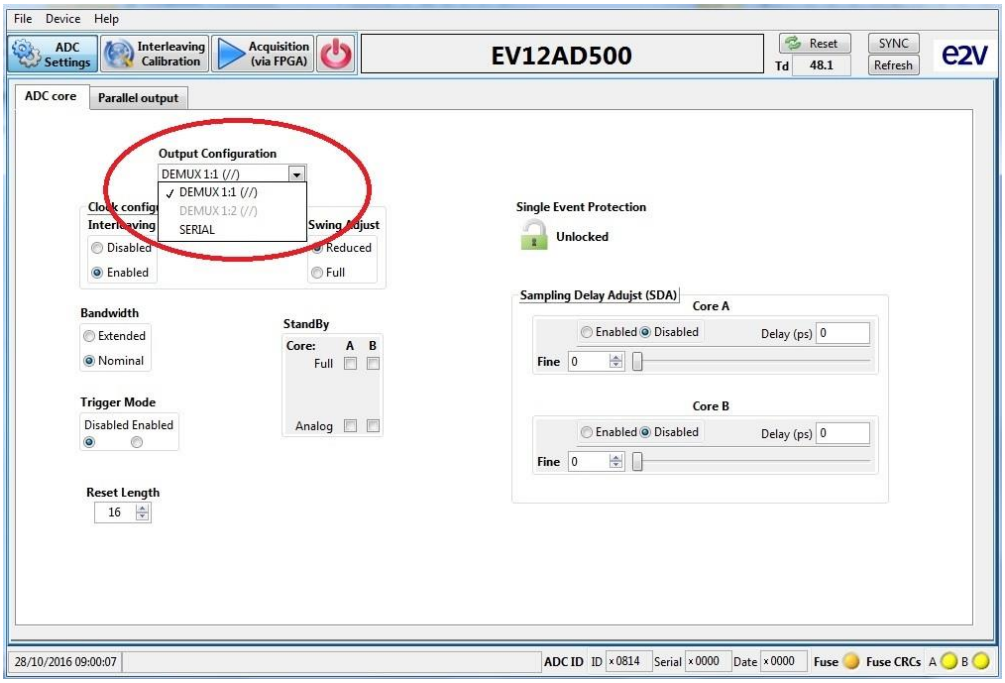
If you have selected EV12AD550x, Demux 1:1 or Demux 1:2 can be chosen.

Figure 4-24.EV12AD550x Output Configuration



If you have selected EV12AD500x, Demux 1:1 or SERIAL can be chosen.

Figure 4-25.EV12AD500x Output Configuration



4.7.1.2 Clock configuration

Figure 4-26.Clock Configuration

- Interleaving:

The two ADC cores can work in phase (sampling clocks aligned) or interleaved.

- Swing Adjust (clock):

Identical to swing adjust LVDS. It controls SYNCO and SSO output swings.

4.7.1.3 Bandwidth

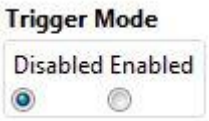
The ADC cores have a tunable bandwidth depending on the package (refer to the datasheet for details).

Figure 4-27.Bandwidth selection

4.7.1.4 Trigger mode

When disabled (default mode), the SYNC TRIG input acts as the SYNC.
When enabled, the SYNC TRIG input acts as the TRIGGER.

Figure 4-28.Trigger Mode



To put the device in TRIGGER mode, it is mandatory to set Trigger Mode on Enabled. It is not sufficient; the control bits detailed in sections 4.7.2.3 for LVDS mode and 4.7.3.3 in serial mode must also be programmed properly.

4.7.1.5 Reset Length

The reset length after a SYNC can be configured. This reset length translates into a certain number of data period where the data ready is maintained at low level after a RESET, when working with LVDS output.

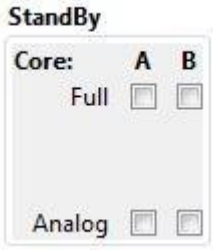
Figure 4-29.Reset Length

The configuration by default is 16 data periods.
The minimum is 2 data periods and the maximum is 63 data periods.

4.7.1.6 StandBy

The user can put the analog part of the device in standby mode.
Full mode allows putting a core in a complete standby mode. Each box is independent.
Refer to the datasheet for details on StandBy modes.

Figure 4-30.Standby



4.7.1.7 Single Event protect

Figure 4-31.Single event protection

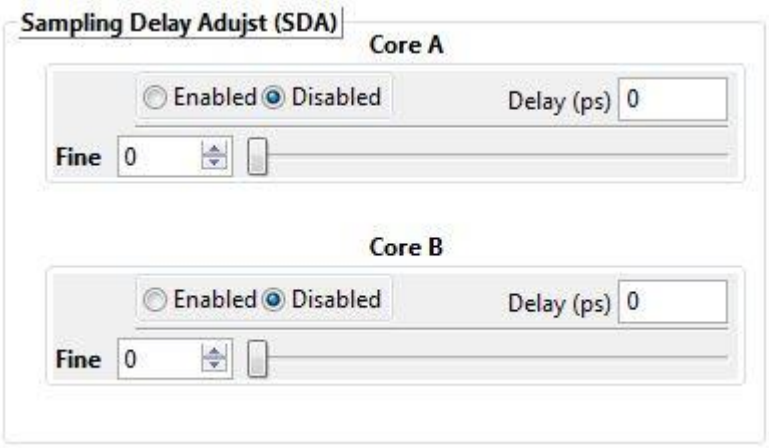
If the padlock is green, the configuration of the device can be changed.
If the padlock is red, no change is possible.
A simple click on the padlock allows user to unlock/lock again.

4.7.1.8 Sample Delay Adjust

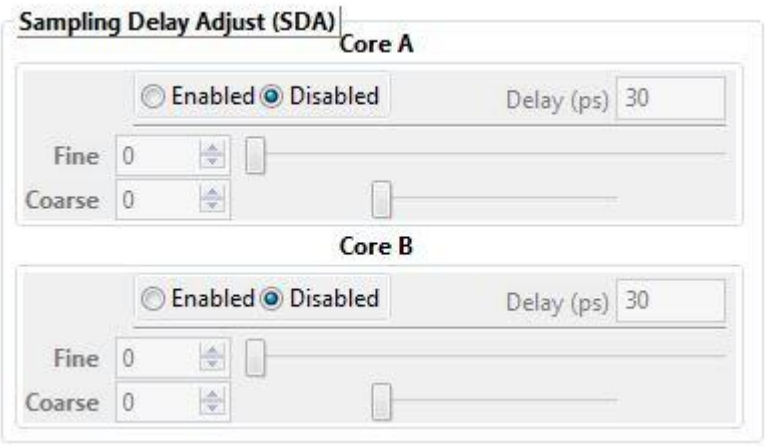
The effective sampling instant of each ADC is adjustable independently thanks to the built-in fine internal clock shifter. Refer to the datasheet for further details.

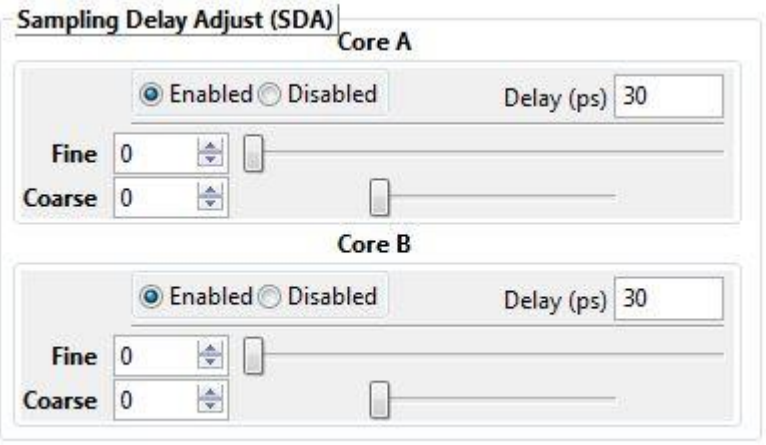
Figure 4-32.Sampling delay Adjust

On AD5x0A (GUI 1.0.1)



On AD5x0B (GUI 1.2.5)





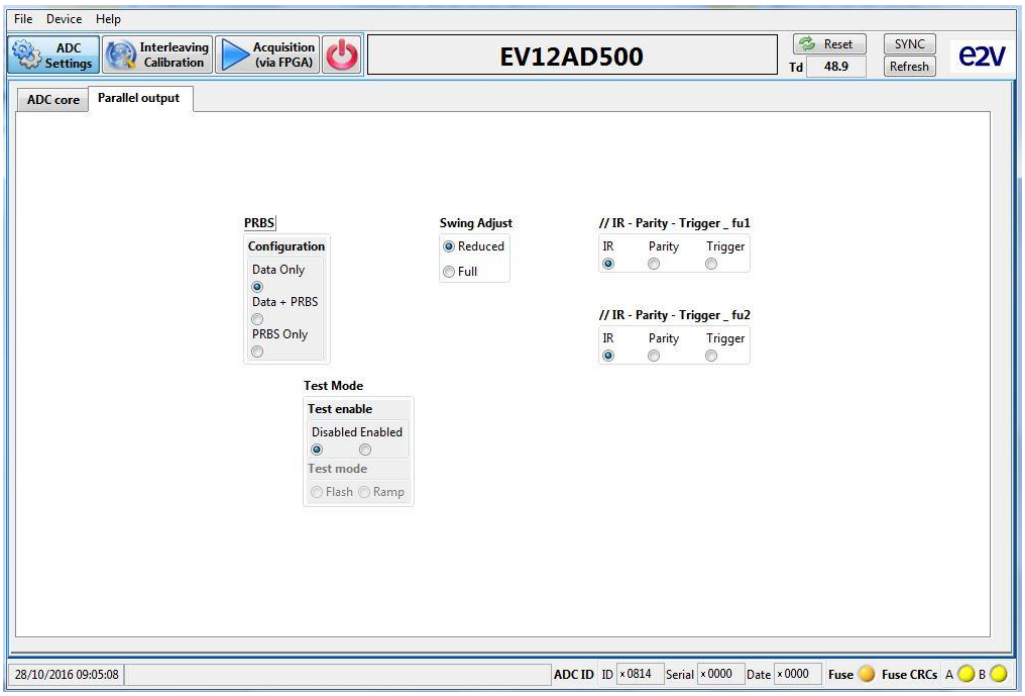
By default, SDA is disabled (by-passed). Activating the SDA has an impact on the jitter performance of the device.

On AD5x0A version, only fine steps can be used.
On AD5x0B version, fine and coarse steps can be selected. When SDA is enabled on core A it is also enabled on core B and vice-versa.

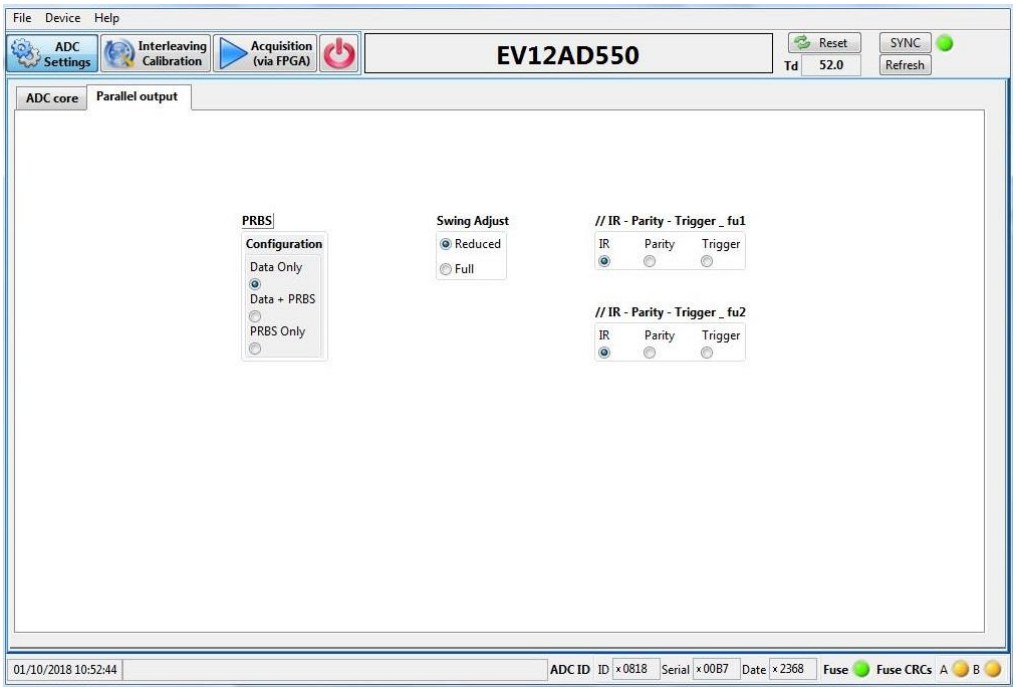
4.7.2 Parallel output

Figure 4-33.User Interface Eval Kit – Parallel output (for EV12AD550x and EV12AD500x)

On AD5x0A (GUI 1.0.1)



On AD5x0B (GUI 1.2.5)



In this window "Parallel Output", the following functions are available:

- PRBS (Pseudo-Random Binary Sequence)
- Swing Adjust (output data)
- //IR - Parity - Trigger_fu1 and //IR - Parity - Trigger_fu2
- Test Mode (on AD5x0A only)

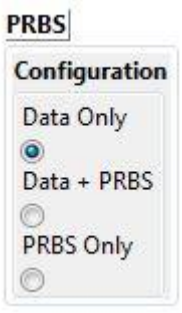
4.7.2.1 PRBS

Pseudo Random Bit Sequence can be generated for LVDS output.
It can be:

- Disabled
- Scrambling the data
- Output alone

The PRBS used is based on the sequence X7 + X6 + 1. When used with the LVDS output (in DEMUX 1:1 or 1:2), the same pseudo-random sequence is output on every digital data bit.

Figure 4-34. PRBS configuration

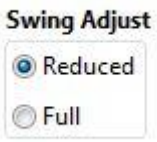


By default, Data Only is selected.

4.7.2.2 Swing Adjust

IO's consumption represents a non-negligible part of dissipation. In case of short routing (in the range of 10 cm) or lower receiver input swing, it is possible to reduce the output dynamic and the consumption by using "swing adjust".
In parallel mode, the swing is reduced by 1/3.

Figure 4-35.Swing Adjust



By default, reduced swing is selected.

4.7.2.3 //IR - Parity -Trigger_fu1/fu2

In case of LVDS output, InRange (IR), Parity or Trigger (TRIG) signals are multiplexed on pad AFU1 and AFU2 for core A, on pad BFU1 and BFU2 for core B.
In Demux 1:1, InRange, Parity or Trigger, selected through SPI command, can be output:

- On AFU1/AFU2 for A high port
- On BFU1/BFU2 for B high port.

In Demux 1:2, InRange, Parity or Trigger, selected through SPI command, can be output:

- On AFU1 for A high port
- On AFU2 for A low port
- On BFU1 for B high port
- On BFU2 for B low port

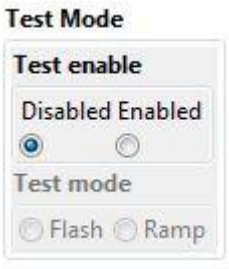
Figure 4-36. //IR - Parity -Trigger_fu1/fu2

See the datasheet to get explanations on the role of each bit.

Those bits work properly only if the trigger mode described in section 4.7.1.4 is put on Enabled.

4.7.2.4 Test Mode on AD5x0A only

Figure 4-37. Test Mode



To access the test mode function, click on enabled button. In test mode selection, checking the box enables the relevant test mode.
Two test modes are available:

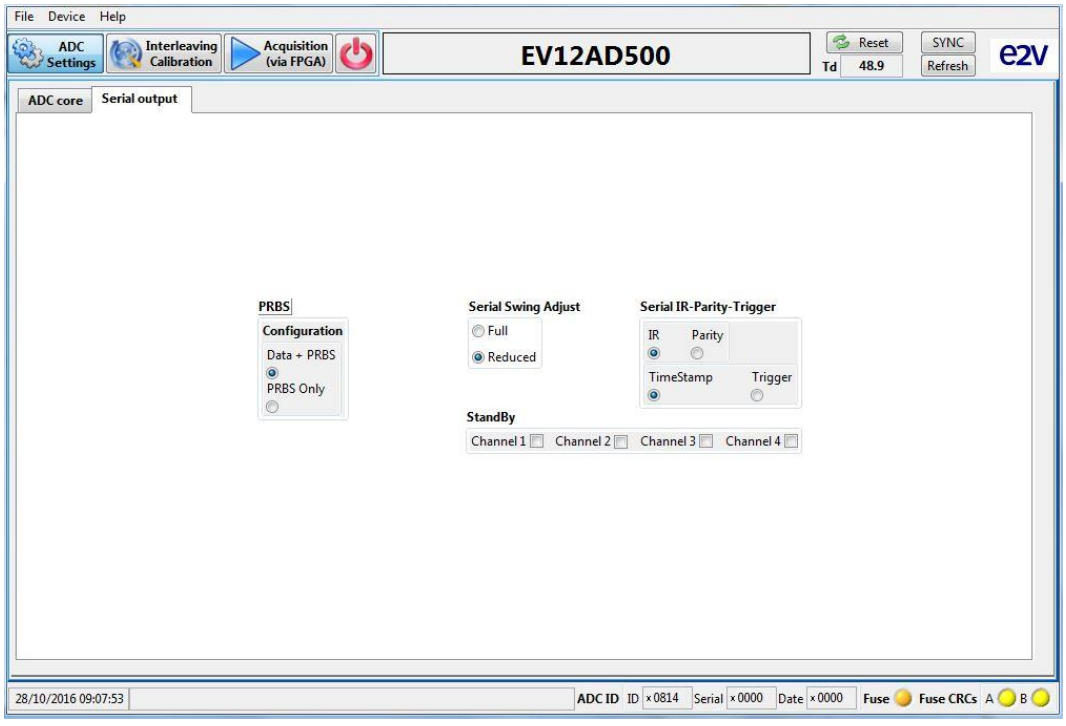
- Flash mode
- Ramp mode

Both are described in the datasheet.

Due to the FPGA code and the LVDS interface synchronization, it is not possible to use the test flash mode with the flash_length setting under 16 when interleaving the 2 cores and using the LVDS interface (DMUX 1:1 and 1:2).

4.7.3 Serial output

Figure 4-38. User Interface Eval Kit – Serial Output (for EV12AD500x only)



In this window "Serial Output", the following functions are available:

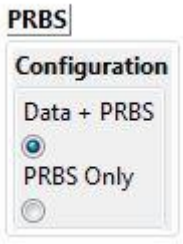
- PRBS (Pseudo-Random Binary Sequence)
- Serial Swing Adjust (output data)
- Serial IR - Parity - Trigger
- StandBy

Note: This window is accessible only if you have selected EV12AD500x in the Device Menu and SERIAL mode in ADC core tab.

4.7.3.1 PRBS

There is an option to output the scrambled data (data + PRBS) according to ESIstream protocol or just the scrambling (PRBS only) on the serial interface. This can be used as a test mode to verify correct function of the serial interface. In PRBS only, the sampled data should be 0x000.
Please refer to the datasheet for details on these functions.

Figure 4-39. PRBS configuration

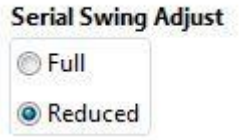


By default, (Data + PRBS) is enabled.

4.7.3.2 Swing Adjust

IO's consumption represents a non-negligible part of dissipation. In case of short routing (in the range of 10 cm) or lower receiver input swing, it is possible to reduce the output dynamic and so the consumption by using "swing adjust". In serial mode, the reduction is 1/2.

Figure 4-40. Serial Swing Adjust



4.7.3.3 Serial IR – Parity - Trigger

In case of serial link interface, InRange (IR) is multiplexed with Parity on output frame bit 12, trigger (TRIG) is multiplexed with a timestamp (PRBS sequence) on output frame bit 13.

The timestamp can be used to identify the samples order and/or check the synchronization of the serial interface.

Please refer to the datasheet for details on these functions.

By default, InRange and TimeStamp are selected.

Figure 4-41. Serial IR – Parity - Trigger

Those bits work properly only if the trigger mode described in section 4.7.1.4 is put on Enabled.

4.7.3.4 StandBy

Figure 4-42. StandBy

Each channel can be put in Standby mode by checking the relevant box.

By default, all channels are active.

4.8 Interleaving calibration

Figure 4-43. User interface Eval Kit – Interleaving calibration

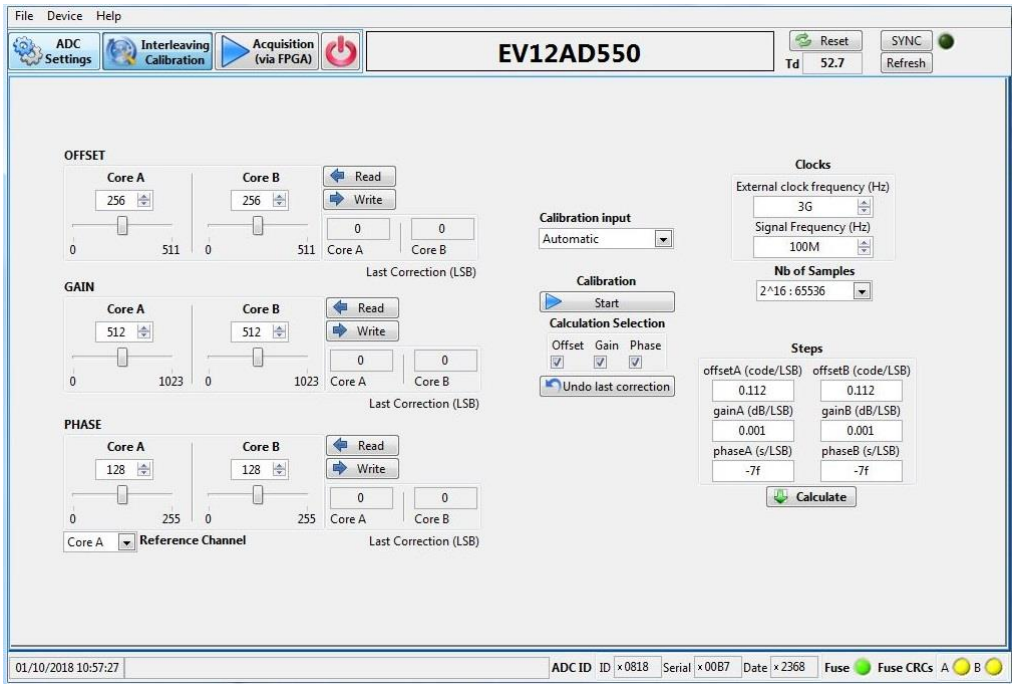
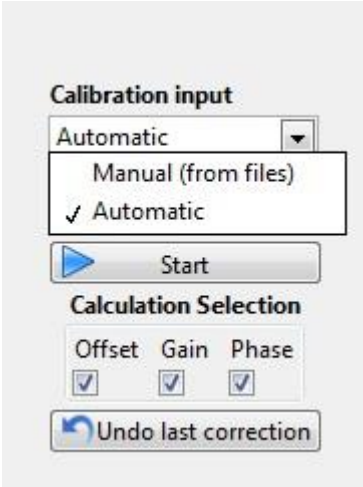


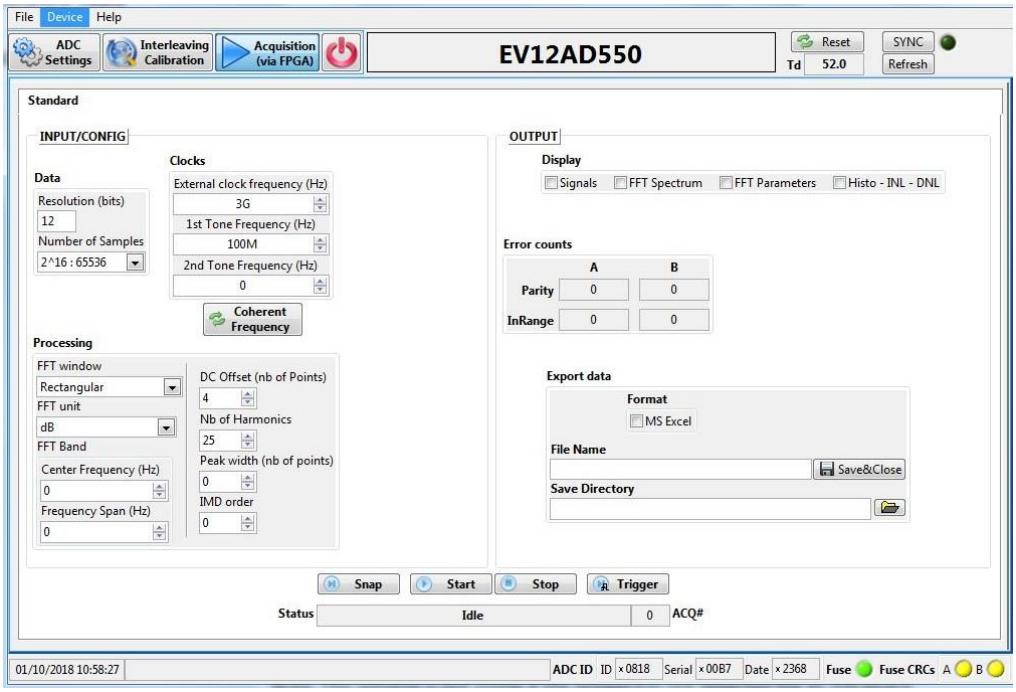
Figure 4-44. Automatic or Manual calibration



The user has the choice between an automatic calibration done by the GUI and a manual calibration. Besides, the user can calibrate each part separately (Offset and/or Gain and/or Phase).
Please refer to dedicated Application Note to run an interleaving calibration.

4.9 Acquisition (via FPGA)

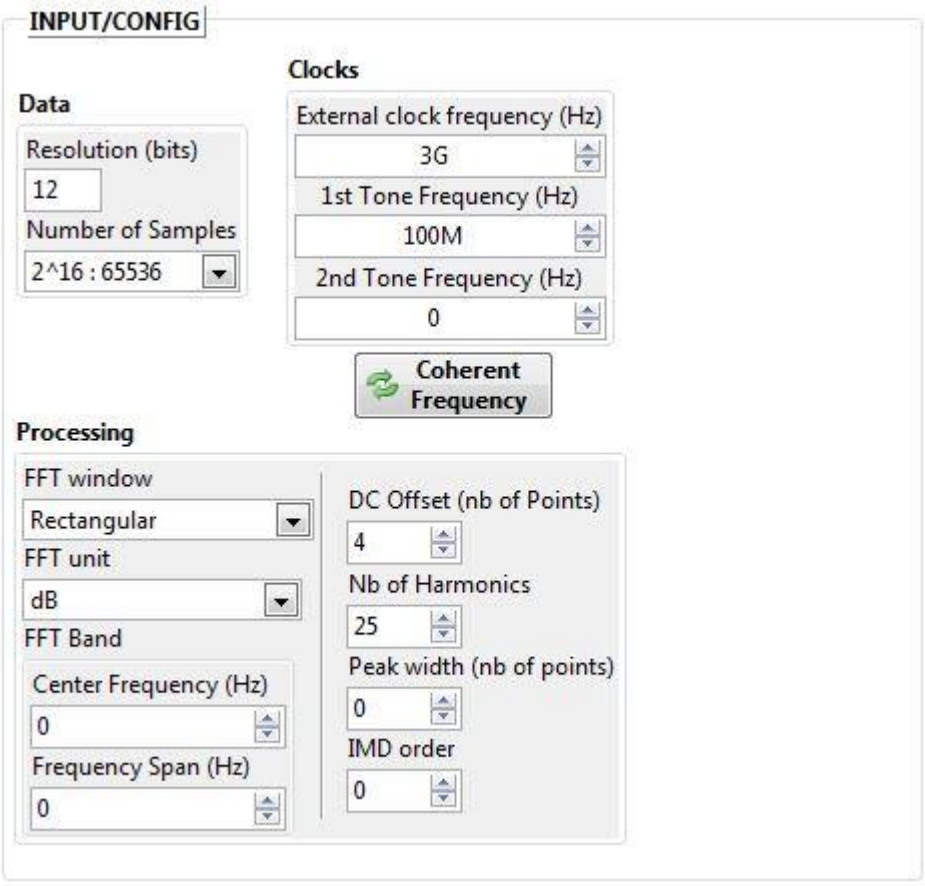
Figure 4-45. User interface Eval Kit – Acquisition (via FPGA)



Note: This window is not visible if the system has not detected the VC709 board.

4.9.1 INPUT/CONFIG

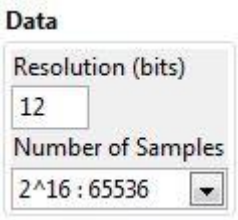
Figure 4-46. INPUT/CONFIG



- **Data**

Resolution (bits): Resolution of the ADC (Read Only).
Number of samples: Number of samples considered for acquisition (Must be a 2^n).

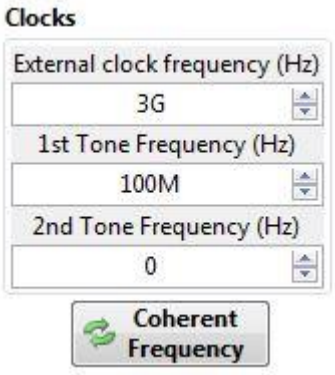
Figure 4-47. Data



By default, a number of 65536 sampling points is selected.

- **Clocks**

Figure 4-48. Clocks



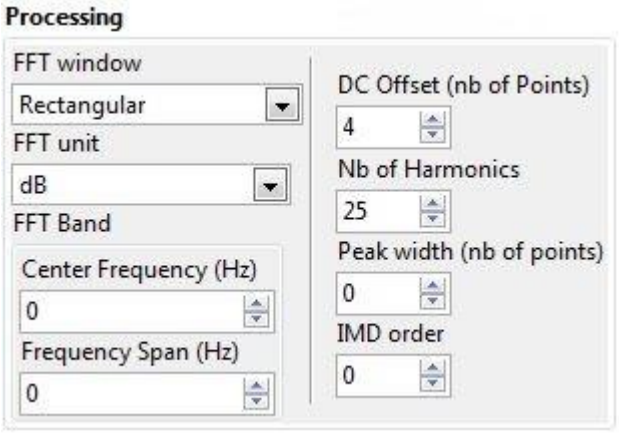
In order to ensure proper signal reconstruction and FFT calculation, the user has to fill in the following frequency values:

- External clock frequency (Hz): Master clock RF generator frequency.
- 1st Tone Frequency (Hz): Analog RF generator frequency.
- 2nd Tone Frequency (Hz): In case of Dual Tone measurement, second Analog RF generator frequency.
- Coherent Frequency: Calculation of the coherent frequency versus total number of points and clock frequency.

Note: Number of Samples, Fclock, Fin, Interleaving mode can change the coherent frequency. Do not forget to re-click on the coherent frequency button when parameters are modified.

- **Processing**

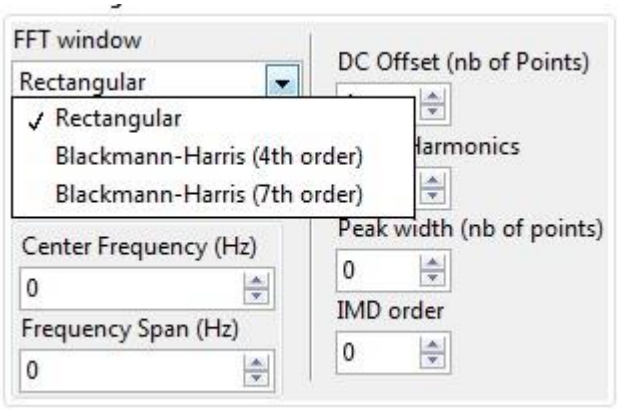
Figure 4-49. Processing



- FFT window:

When the analog input signal and the sampling clock are not coherent signals, a FFT window has to be applied to obtain a correct result.
By default, rectangular is selected.
Blackmann-Harris (4th order) and Blackmann-Harris (7th order) are also available.

Figure 4-50. FFT Window



- FFT unit: Results can be expressed in dB or dBc.

- FFT band, center frequency and frequency span:

FFT calculations can be computed over a smaller range than Nyquist. To do so, center frequency and frequency span must be filled in.

- DC offset (number of points):

Number of points to be excluded from calculations to bypass DC peak (to ensure DC peak is not taken into account when computing FFT calculations).
Default value depends on the selected FFT window.

- Nb of Harmonics:

Number of Harmonics considered for THD and SNR calculation (Default value is 25 harmonics).

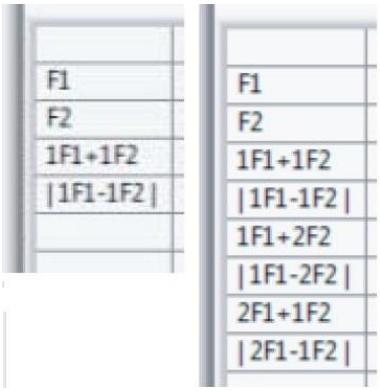
- Peak width:

When a FFT window is applied the harmonic signal is composed of several points.
The number to be filled in corresponds to the number of points that should be removed from the calculations on each side of the fundamental and harmonic signals.
As an example, if Peak Width = 4 then 4 points will be removed on the left of the peak and 4 points on the right of the peak; a total amount of 9 points will be removed (exclusion on left + exclusion on right + harmonic itself).
Default value depends on the selected FFT window.

- IMD order:

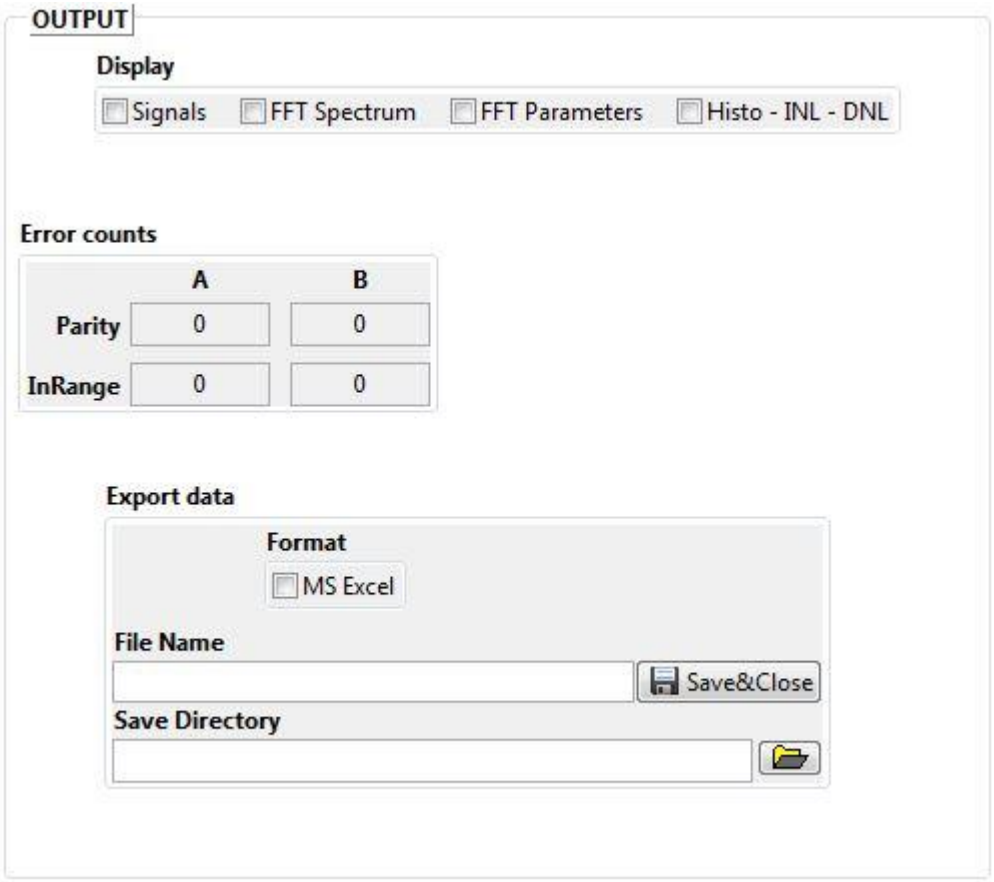
In the case of dual-tone measurement, this box allows to choose the number of intermodulation harmonics to be computed.

Figure 4-51. Example of IMD order = 2 and IMD order = 3



4.9.2 OUTPUT

Figure 4-52. OUTPUT



- **Display**

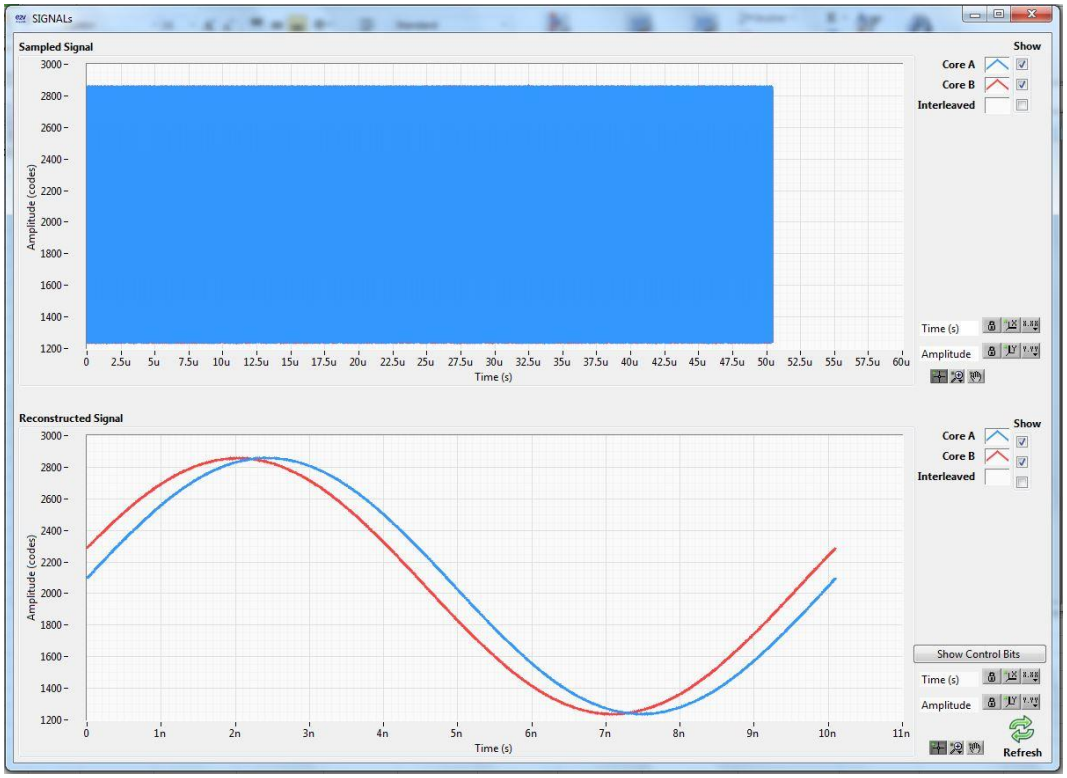
Figure 4-53. Display

By checking the boxes the user can select the data to be displayed. A dedicated window will then open.
On each opened window, refresh and zoom options are available. Also window sizes can be modified.

- Signals

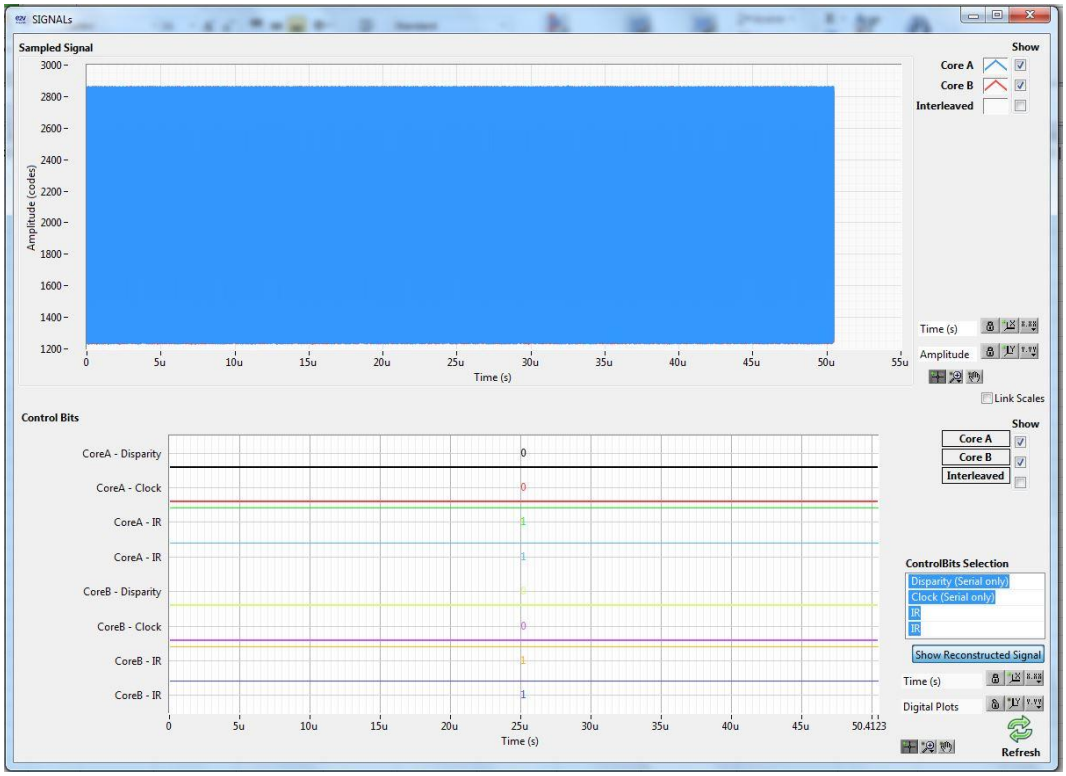
In this window, sampled and reconstructed signals are visible.

Figure 4-54. Signal window with Reconstructed Signal



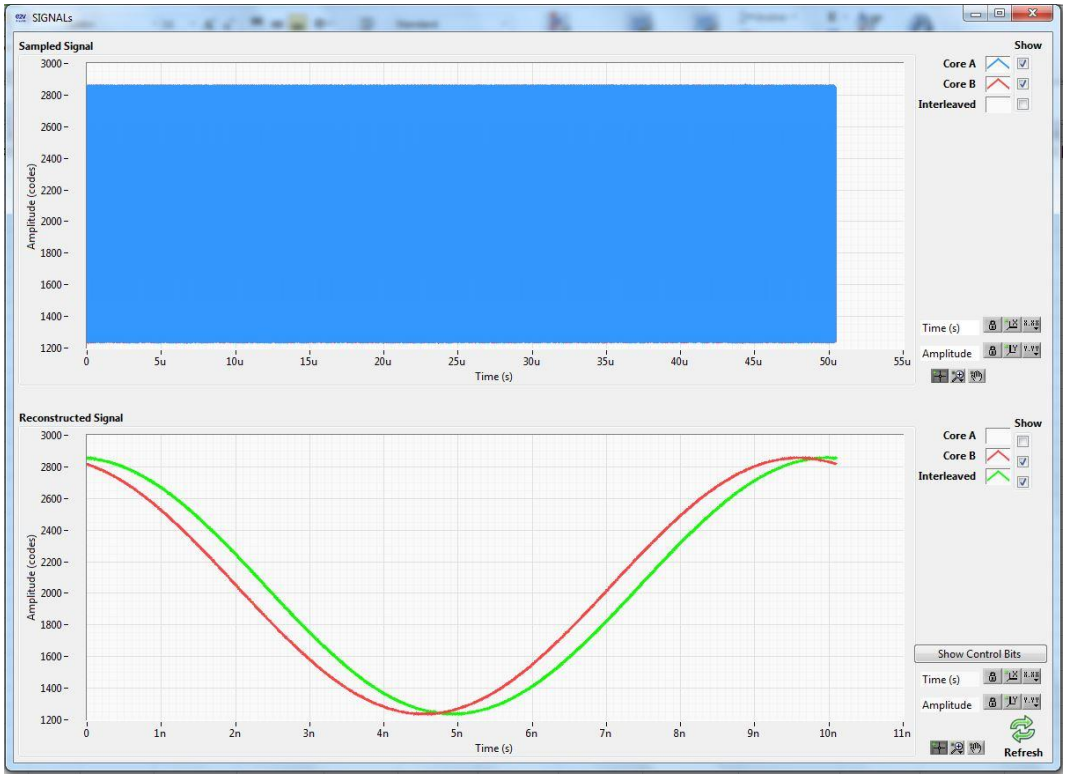
Control bits can be displayed using buttons on bottom left.
All the control bits for core A and core B can then be visible.

Figure 4-55. Signal window with Control Bits



In interleaving mode, core A, core B and interleaved [A, B] can be visible together or separately.

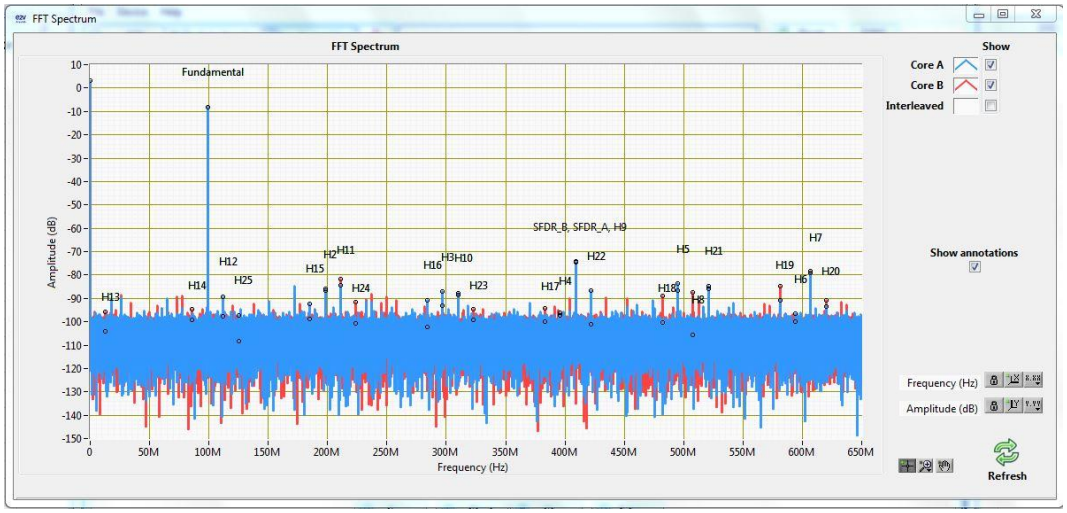
Figure 4-56. Signal window with non-interleaved signal and interleaved signal



- FFT spectrum

Core A alone, Core B alone and interleaved can be displayed separately.
'Show annotations' box can be disabled.

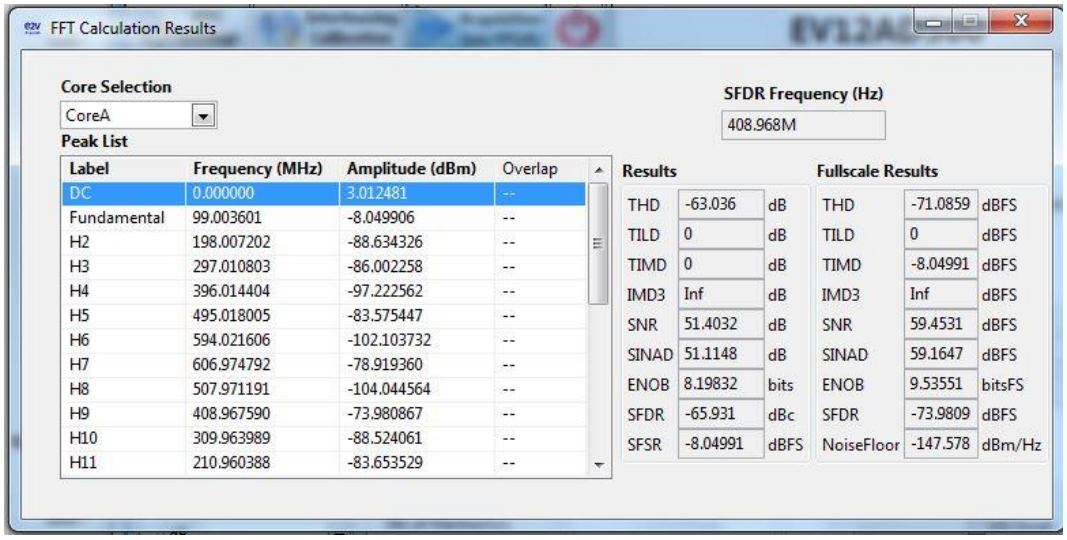
Figure 4-57. FFT spectrum window



- FFT parameters

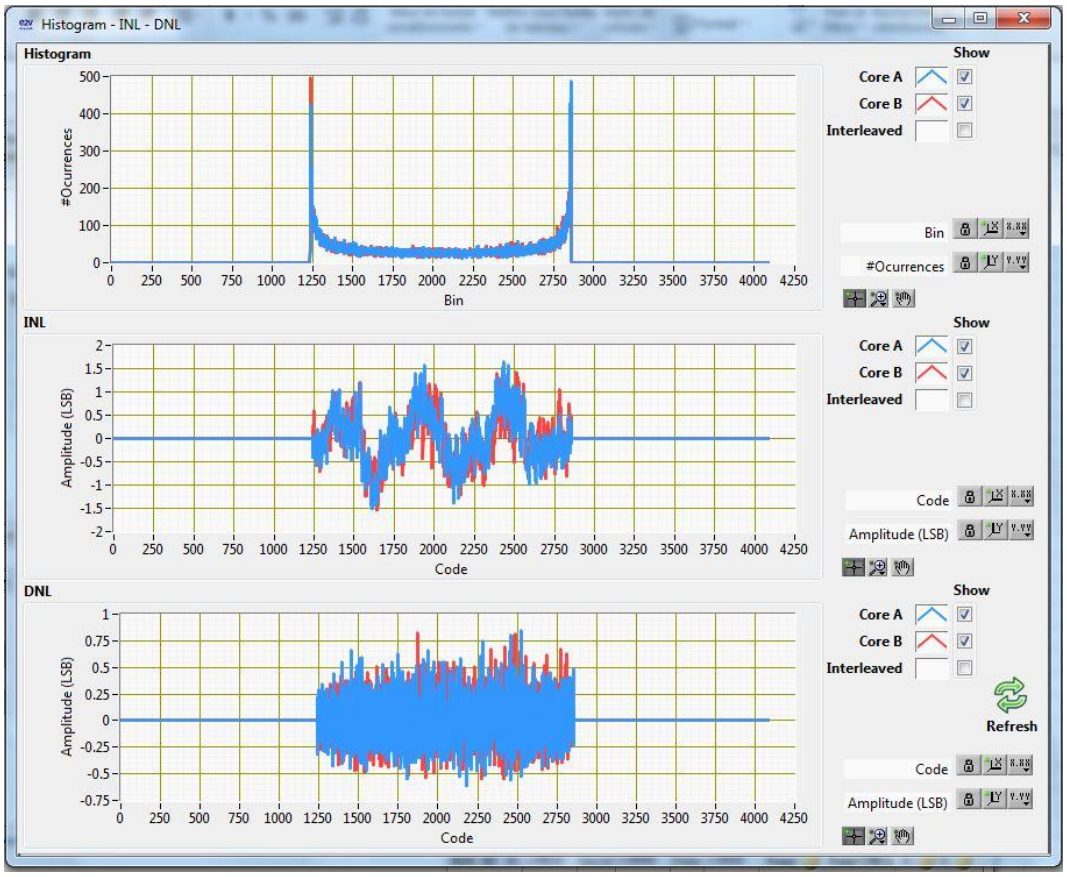
This window allows reading the values of each parameter on core A or core B or interleaving.
Results are given in dBc and dBFS.

Figure 4-58. FFT calculation window



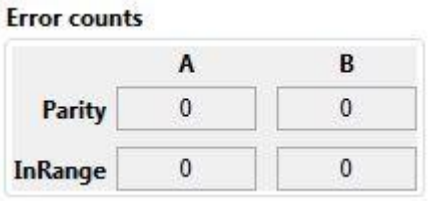
- Histo- INL-DNL

Figure 4-59. Histogram- INL- DNL window



- **Error counts**

Figure 4-60. Error counts

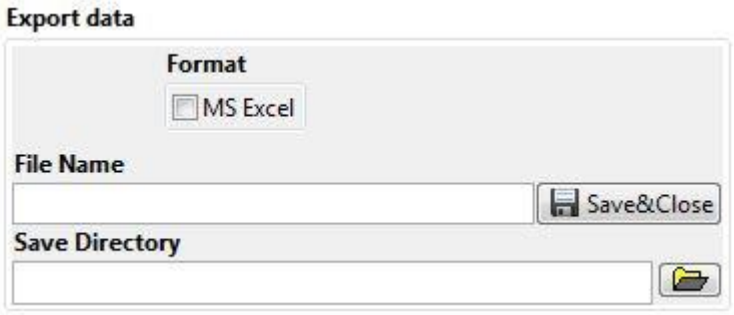


This indicator displays errors relative to Parity and InRange bits for both cores depending on AFU 1/2, BFU 1/2 user selection.
The InRange bit indicates whether the input signal is within the ADC dynamic range or not. When the ADC input signal is over the ADC dynamic range, the InRange bit is low and it generates a +1 on the error indicator.
The Parity of the 12 output bits of each data is calculated by performing a XOR combination between the 12 bits of output data. It is output at the same time as the 12-bits data.

Refer to the datasheet for details on those functions.

- **Export Data**

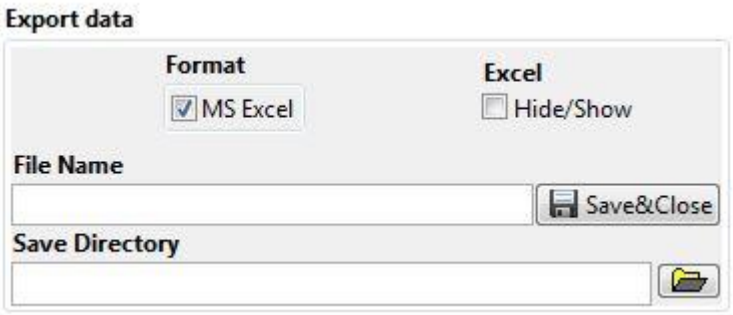
Figure 4-61. Export Data



Data can be exported in Excel format.

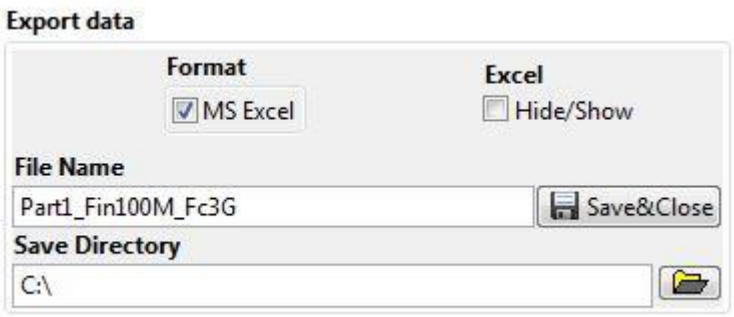
Once MS Excel is checked, Excel Hide/show box appears. If the box is not checked, the recording is done but the file does not appear.

Figure 4-62. Excel Hide/Show



To save the data in Excel format, the user needs to create a File Name and choose the Directory in which the file will be recorded.

Figure 4-63. File Name and Directory



From then onwards, each acquisition launched through 'SNAP' or 'START' buttons is recorded.

Figure 4-64. SNAP/START-STOP

The user has the possibility to uncheck and then recheck the box "MS Excel" to select some acquisitions to be recorded and some to be run with recording data.

In the excel file, data are recorded one after the other. If a file is closed and reopened later, the existing data will not be deleted.

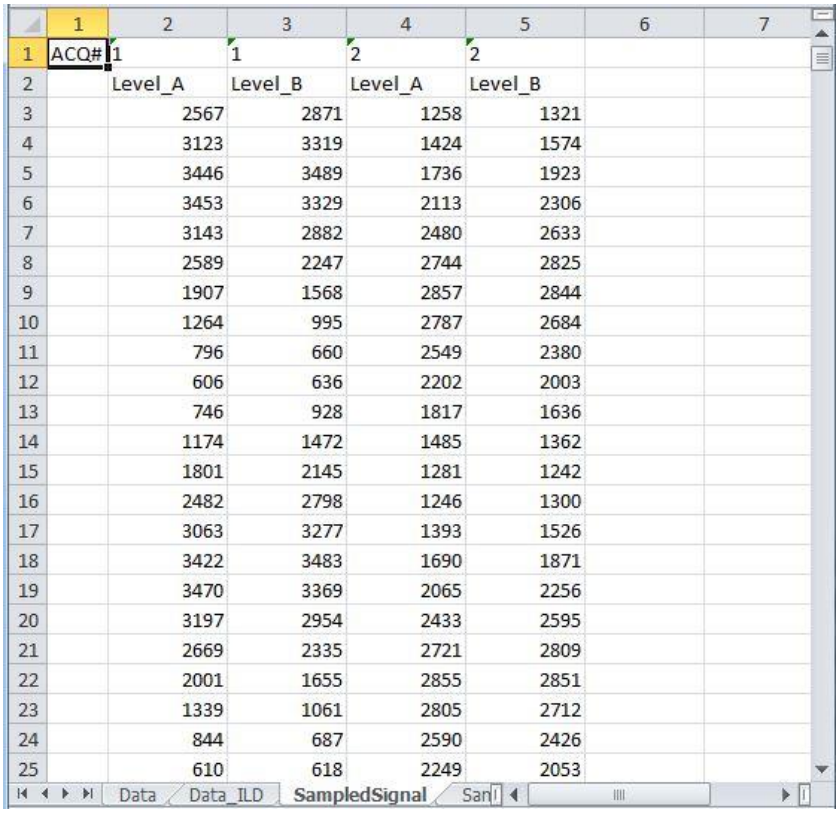
The following figures show examples of the excel file with 2 acquisitions on core A and core B.

Figure 4-65. Data tab

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1			MHz	MHz	MHz	MHz	Mhz			dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS
2	ACQ#	Core	Fc	Fin1	Fin2	FFT Band	FFT Band Width	Parity	InRange	THD	THD_FS	TIMD	TIMD_FS	TILD	TILD_FS	TD	TD_FS	SINAD	SINAD_F
3	1	A	2600	99.00360107	0	0	0	0	0	-70.22556126	-73.27817272	0	-3.052611459	0	0	-70.22556126	-73.27817272	55.92277435	58.9753
4	1	B	2600	99.00360107	0	0	0	0	0	-71.01516949	-74.07531156	0	-3.060142076	0	0	-71.01516949	-74.07531156	56.06177284	59.1219
5	2	A	2600	99.00360107	0	0	0	0	0	-62.78562839	-70.82776207	0	-8.042133676	0	0	-62.78562839	-70.82776207	51.07936797	59.1215
6	2	B	2600	99.00360107	0	0	0	0	0	-63.2380164	-71.29040355	0	-8.052387152	0	0	-63.2380164	-71.29040355	51.20248279	59.2548
7																			

Data | Data_ILD | SampledSignal | SampledSignal_ILD | ControlBits | ControlBits_ILD | ReconstructedSign

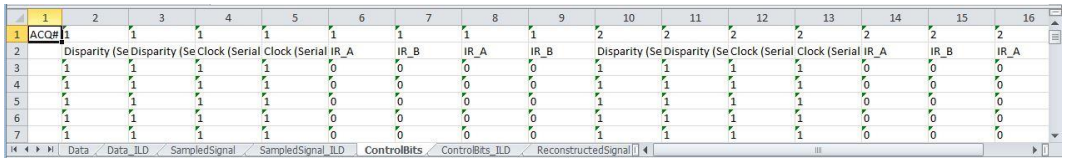
Figure 4-66. Sampled tab



	1	2	3	4	5	6	7
1	ACQ#	1	1	2	2		
2		Level_A	Level_B	Level_A	Level_B		
3		2567	2871	1258	1321		
4		3123	3319	1424	1574		
5		3446	3489	1736	1923		
6		3453	3329	2113	2306		
7		3143	2882	2480	2633		
8		2589	2247	2744	2825		
9		1907	1568	2857	2844		
10		1264	995	2787	2684		
11		796	660	2549	2380		
12		606	636	2202	2003		
13		746	928	1817	1636		
14		1174	1472	1485	1362		
15		1801	2145	1281	1242		
16		2482	2798	1246	1300		
17		3063	3277	1393	1526		
18		3422	3483	1690	1871		
19		3470	3369	2065	2256		
20		3197	2954	2433	2595		
21		2669	2335	2721	2809		
22		2001	1655	2855	2851		
23		1339	1061	2805	2712		
24		844	687	2590	2426		
25		610	618	2249	2053		

Data | Data_ILD | **SampledSignal** | San

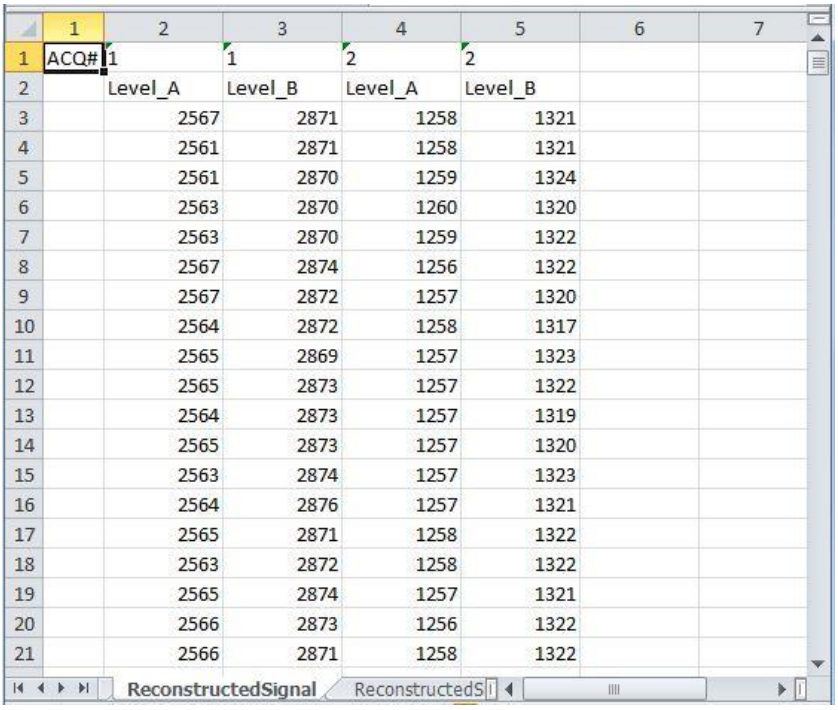
Figure 4-67. ControlBits tab



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	ACQ#	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2
2		Disparity (Se	Disparity (Se	Clock (Serial	Clock (Serial	IR_A	IR_B	IR_A	IR_B	Disparity (Se	Disparity (Se	Clock (Serial	Clock (Serial	IR_A	IR_B	IR_A
3		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
4		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
5		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
6		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
7		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0

Data | Data_ILD | SampledSignal | SampledSignal_ILD | **ControlBits** | ControlBits_ILD | ReconstructedSignal

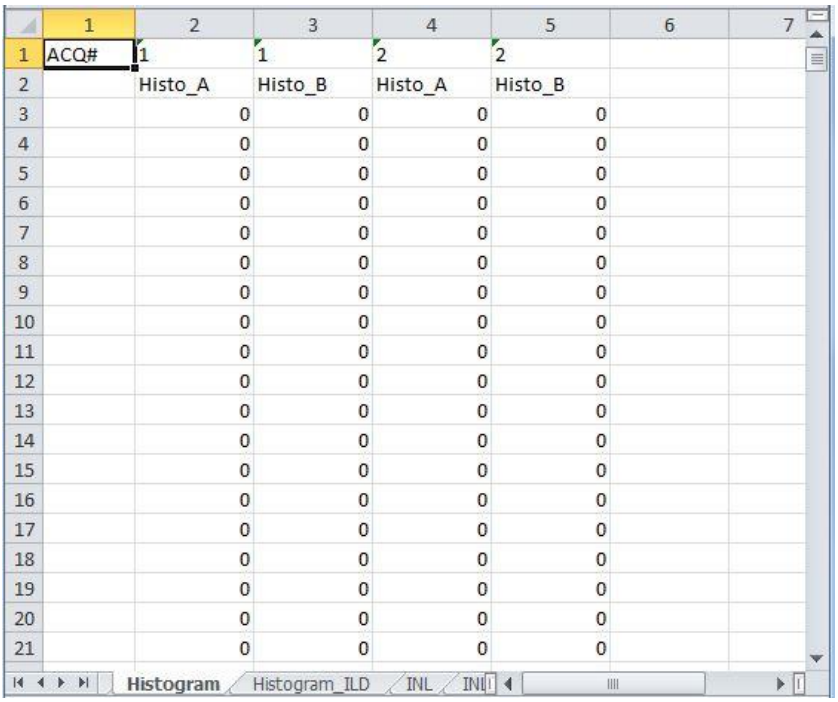
Figure 4-68. ReconstructedSignal tab



	1	2	3	4	5	6	7
1	ACQ#	1	1	2	2		
2		Level_A	Level_B	Level_A	Level_B		
3		2567	2871	1258	1321		
4		2561	2871	1258	1321		
5		2561	2870	1259	1324		
6		2563	2870	1260	1320		
7		2563	2870	1259	1322		
8		2567	2874	1256	1322		
9		2567	2872	1257	1320		
10		2564	2872	1258	1317		
11		2565	2869	1257	1323		
12		2565	2873	1257	1322		
13		2564	2873	1257	1319		
14		2565	2873	1257	1320		
15		2563	2874	1257	1323		
16		2564	2876	1257	1321		
17		2565	2871	1258	1322		
18		2563	2872	1258	1322		
19		2565	2874	1257	1321		
20		2566	2873	1256	1322		
21		2566	2871	1258	1322		

ReconstructedSignal | ReconstructedS

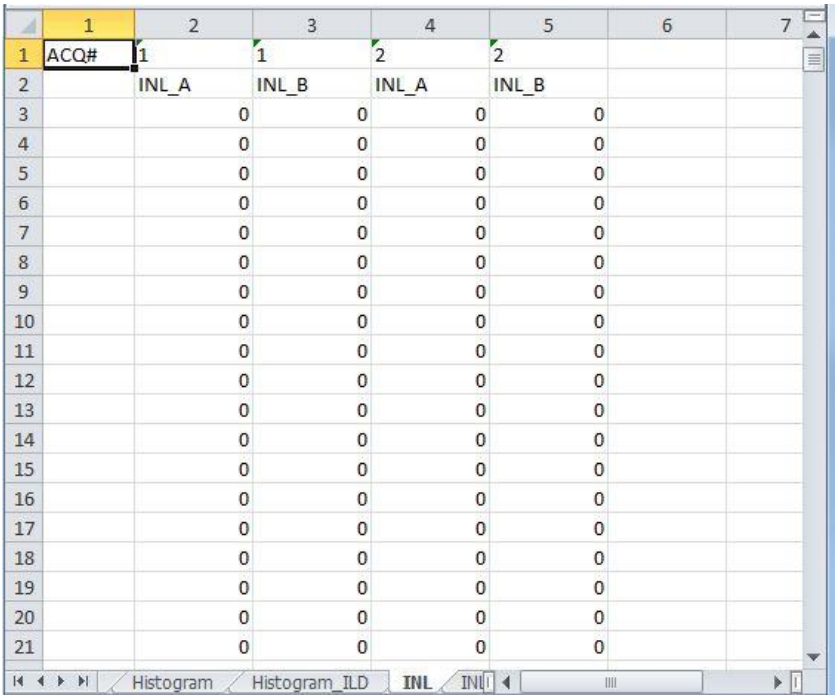
Figure 4-69. Histogram Tab



	1	2	3	4	5	6	7
1	ACQ#	1	1	2	2		
2		Histo_A	Histo_B	Histo_A	Histo_B		
3		0	0	0	0		
4		0	0	0	0		
5		0	0	0	0		
6		0	0	0	0		
7		0	0	0	0		
8		0	0	0	0		
9		0	0	0	0		
10		0	0	0	0		
11		0	0	0	0		
12		0	0	0	0		
13		0	0	0	0		
14		0	0	0	0		
15		0	0	0	0		
16		0	0	0	0		
17		0	0	0	0		
18		0	0	0	0		
19		0	0	0	0		
20		0	0	0	0		
21		0	0	0	0		

Histogram | Histogram_ILD | INL | INL

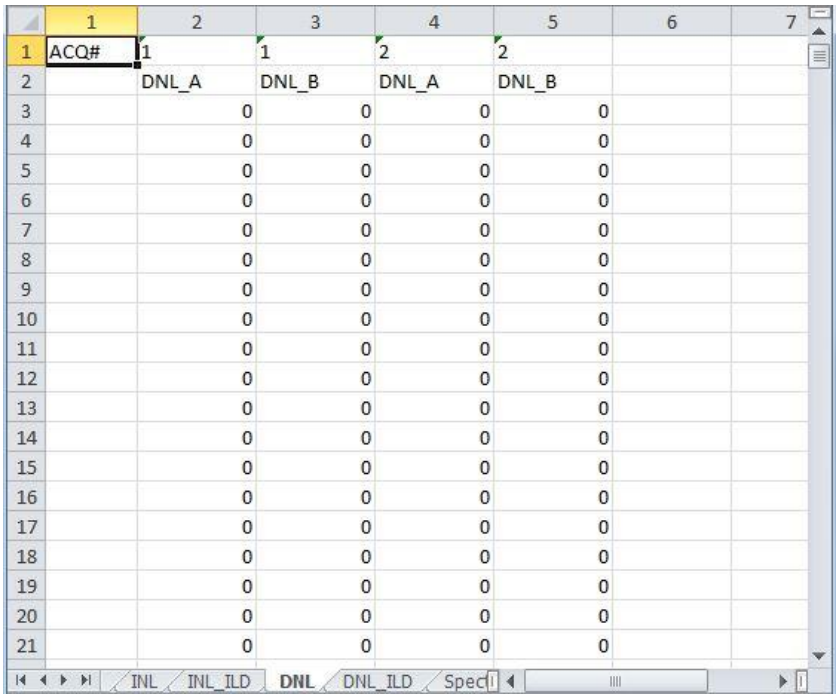
Figure 4-70. INL Tab



	1	2	3	4	5	6	7
1	ACQ#	1	1	2	2		
2		INL_A	INL_B	INL_A	INL_B		
3		0	0	0	0		
4		0	0	0	0		
5		0	0	0	0		
6		0	0	0	0		
7		0	0	0	0		
8		0	0	0	0		
9		0	0	0	0		
10		0	0	0	0		
11		0	0	0	0		
12		0	0	0	0		
13		0	0	0	0		
14		0	0	0	0		
15		0	0	0	0		
16		0	0	0	0		
17		0	0	0	0		
18		0	0	0	0		
19		0	0	0	0		
20		0	0	0	0		
21		0	0	0	0		

Histogram | Histogram_ILD | **INL** | INL

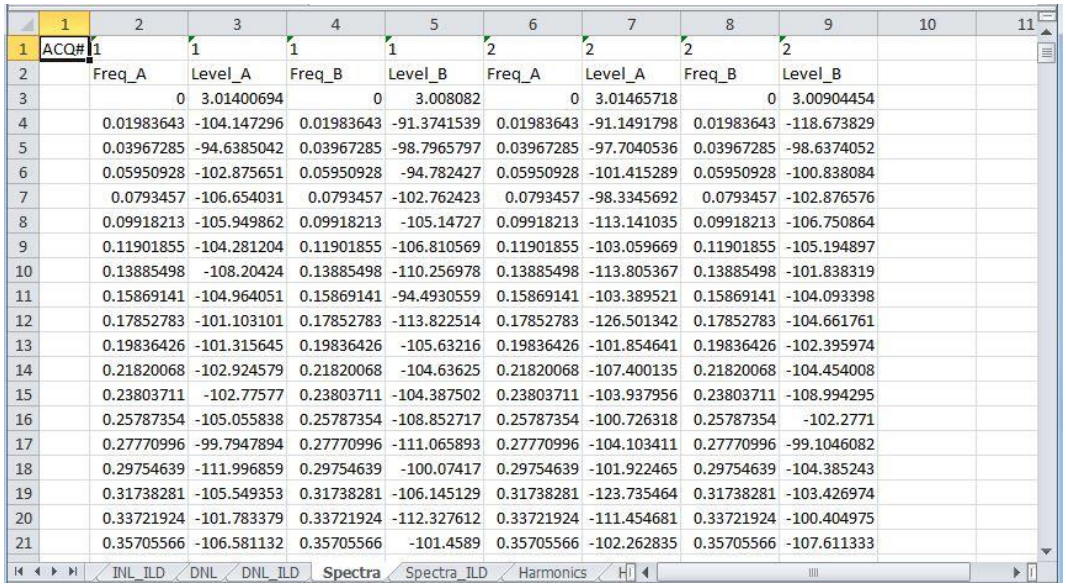
Figure 4-71. DNL Tab



	1	2	3	4	5	6	7
1	ACQ#	1	1	2	2		
2		DNL_A	DNL_B	DNL_A	DNL_B		
3		0	0	0	0		
4		0	0	0	0		
5		0	0	0	0		
6		0	0	0	0		
7		0	0	0	0		
8		0	0	0	0		
9		0	0	0	0		
10		0	0	0	0		
11		0	0	0	0		
12		0	0	0	0		
13		0	0	0	0		
14		0	0	0	0		
15		0	0	0	0		
16		0	0	0	0		
17		0	0	0	0		
18		0	0	0	0		
19		0	0	0	0		
20		0	0	0	0		
21		0	0	0	0		

INL | INL_ILD | **DNL** | DNL_ILD | Spec

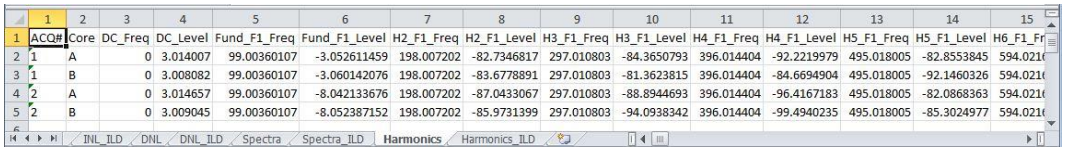
Figure 4-72. Spectra Tab



	1	2	3	4	5	6	7	8	9	10	11
1	ACQ#	1		1		1		2		2		2	
2		Freq_A	Level_A	Freq_B	Level_B	Freq_A	Level_A	Freq_B	Level_B		
3		0	3.01400694	0	3.008082	0	3.01465718	0	3.00904454		
4		0.01983643	-104.147296	0.01983643	-91.3741539	0.01983643	-91.1491798	0.01983643	-118.673829		
5		0.03967285	-94.6385042	0.03967285	-98.7965797	0.03967285	-97.7040536	0.03967285	-98.6374052		
6		0.05950928	-102.875651	0.05950928	-94.782427	0.05950928	-101.415289	0.05950928	-100.838084		
7		0.0793457	-106.654031	0.0793457	-102.762423	0.0793457	-98.3345692	0.0793457	-102.876576		
8		0.09918213	-105.949862	0.09918213	-105.14727	0.09918213	-113.141035	0.09918213	-106.750864		
9		0.11901855	-104.281204	0.11901855	-106.810569	0.11901855	-103.059669	0.11901855	-105.194897		
10		0.13885498	-108.20424	0.13885498	-110.256978	0.13885498	-113.805367	0.13885498	-101.838319		
11		0.15869141	-104.964051	0.15869141	-94.4930559	0.15869141	-103.389521	0.15869141	-104.093398		
12		0.17852783	-101.103101	0.17852783	-113.822514	0.17852783	-126.501342	0.17852783	-104.661761		
13		0.19836426	-101.315645	0.19836426	-105.63216	0.19836426	-101.854641	0.19836426	-102.395974		
14		0.21820068	-102.924579	0.21820068	-104.63625	0.21820068	-107.400135	0.21820068	-104.454008		
15		0.23803711	-102.77577	0.23803711	-104.387502	0.23803711	-103.937956	0.23803711	-108.994295		
16		0.25787354	-105.055838	0.25787354	-108.852717	0.25787354	-100.726318	0.25787354	-102.2771		
17		0.27770996	-99.7947894	0.27770996	-111.065893	0.27770996	-104.103411	0.27770996	-99.1046082		
18		0.29754639	-111.996859	0.29754639	-100.07417	0.29754639	-101.922465	0.29754639	-104.385243		
19		0.31738281	-105.549353	0.31738281	-106.145129	0.31738281	-123.735464	0.31738281	-103.426974		
20		0.33721924	-101.783379	0.33721924	-112.327612	0.33721924	-111.454681	0.33721924	-100.404975		
21		0.35705566	-106.581132	0.35705566	-101.4589	0.35705566	-102.262835	0.35705566	-107.611333		

INL_ILD | DNL | DNL_ILD | **Spectra** | Spectra_ILD | Harmonics | H

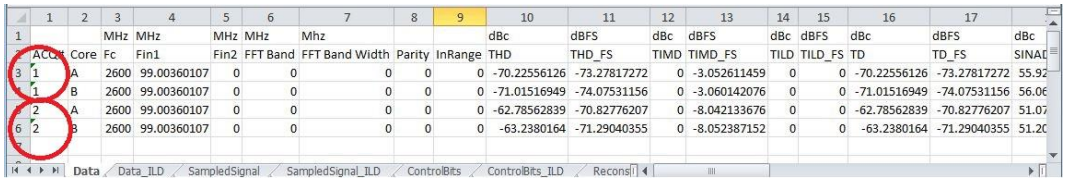
Figure 4-73. Harmonics Tab



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	ACQ#	Core	DC_Freq	DC_Level	Fund_F1_Freq	Fund_F1_Level	H2_F1_Freq	H2_F1_Level	H3_F1_Freq	H3_F1_Level	H4_F1_Freq	H4_F1_Level	H5_F1_Freq	H5_F1_Level	H6_F1_Fr
2	1	A	0	3.014007	99.00360107	-3.052611459	198.007202	-82.7346817	297.010803	-84.3650793	396.014404	-92.2219979	495.018005	-82.8553845	594.021
3	1	B	0	3.008082	99.00360107	-3.060142076	198.007202	-83.6778891	297.010803	-81.3623815	396.014404	-84.6694904	495.018005	-92.1460326	594.021
4	2	A	0	3.014657	99.00360107	-8.042133676	198.007202	-87.0433067	297.010803	-88.8944693	396.014404	-96.4167183	495.018005	-82.0868363	594.021
5	2	B	0	3.009045	99.00360107	-8.052387152	198.007202	-85.9731399	297.010803	-94.0938342	396.014404	-99.4940235	495.018005	-85.3024977	594.021

INL_ILD | DNL | DNL_ILD | Spectra | Spectra_ILD | **Harmonics** | Harmonics_ILD

Figure 4-74. Identification of the 2 acquisitions on core A and core B

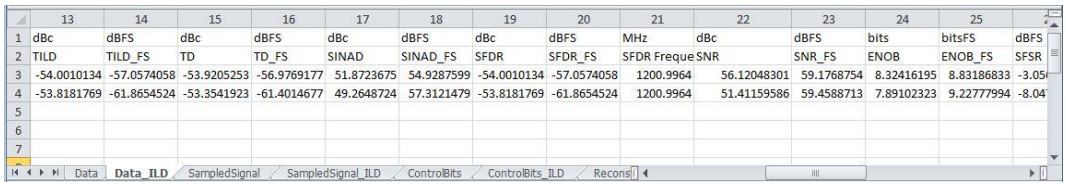


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
1			MHz	MHz	MHz	MHz	Mhz			dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc
2	ACQ#	Core	Fc	Fin1	Fin2	FFT Band	FFT Band Width	Parity	InRange	THD	THD_FS	TIMD	TIMD_FS	TILD	TILD_FS	TD	TD_FS	SINAD
3	1	A	2600	99.00360107	0	0	0	0	0	-70.22556126	-73.27817272	0	-3.052611459	0	0	-70.22556126	-73.27817272	55.92
4	1	B	2600	99.00360107	0	0	0	0	0	-71.01516949	-74.07531156	0	-3.060142076	0	0	-71.01516949	-74.07531156	56.06
5	2	A	2600	99.00360107	0	0	0	0	0	-62.78562839	-70.82776207	0	-8.042133676	0	0	-62.78562839	-70.82776207	51.07
6	2	B	2600	99.00360107	0	0	0	0	0	-63.2380164	-71.29040355	0	-8.052387152	0	0	-63.2380164	-71.29040355	51.20

Data | Data_ILD | SampledSignal | SampledSignal_ILD | ControlBits | ControlBits_ILD | Recons

When interleaving clock is enabled, XXX_ILD tabs are created. In the example below, first line corresponds to the 1st acquisition and second line corresponds to the 2nd acquisition.

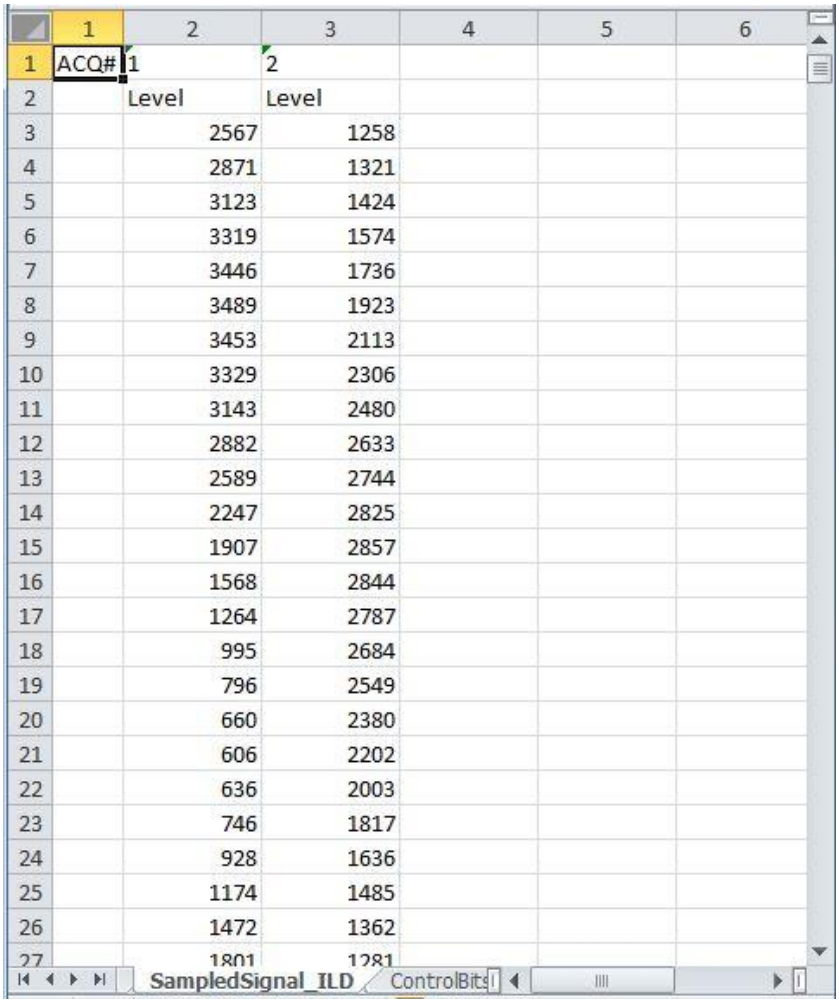
Figure 4-75. Data_ILD Tab



	13	14	15	16	17	18	19	20	21	22	23	24	25	
1	dBc	dBFS	dBc	dBFS	dBc	dBFS	dBc	dBFS	MHz	dBc	dBFS	bits	bitsFS	dBFS
2	TILD	TILD_FS	TD	TD_FS	SINAD	SINAD_FS	SFDR	SFDR_FS	SFDR Freque	SNR	SNR_FS	ENOB	ENOB_FS	SFSR
3	-54.0010134	-57.0574058	-53.9205253	-56.9769177	51.8723675	54.9287599	-54.0010134	-57.0574058	1200.9964	56.12048301	59.1768754	8.32416195	8.83186833	-3.05
4	-53.8181769	-61.8654524	-53.3541923	-61.4014677	49.2648724	57.3121479	-53.8181769	-61.8654524	1200.9964	51.41159586	59.4588713	7.89102323	9.22777994	-8.04
5														
6														
7														

Data | **Data_ILD** | SampledSignal | SampledSignal_ILD | ControlBits | ControlBits_ILD | Recons

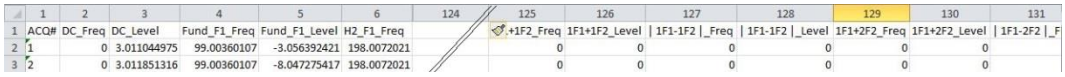
Figure 4-76. Sampled_ILD Tab



	1	2	3	4	5	6
1	ACQ#	1	2			
2		Level	Level			
3		2567	1258			
4		2871	1321			
5		3123	1424			
6		3319	1574			
7		3446	1736			
8		3489	1923			
9		3453	2113			
10		3329	2306			
11		3143	2480			
12		2882	2633			
13		2589	2744			
14		2247	2825			
15		1907	2857			
16		1568	2844			
17		1264	2787			
18		995	2684			
19		796	2549			
20		660	2380			
21		606	2202			
22		636	2003			
23		746	1817			
24		928	1636			
25		1174	1485			
26		1472	1362			
27		1801	1281			

SampledSignal_ILD | ControlBits

Figure 4-77. Harmonics_ILD Tab



	1	2	3	4	5	6	124	125	126	127	128	129	130	131
1	ACQ#	DC_Freq	DC_Level	Fund_F1_Freq	Fund_F1_Level	H2_F1_Freq		+1F2_Freq	1F1+1F2_Level	| 1F1-1F2 | _Freq	| 1F1-1F2 | _Level	1F1+2F2_Freq	1F1+2F2_Level	| 1F1-2F2 | _F
2	1	0	3.011044975	99.00360107	-3.056392421	198.0072021		0	0	0	0	0	0	
3	2	0	3.011851316	99.00360107	-8.047275417	198.0072021		0	0	0	0	0	0	

In Harmonics tab, in addition to all harmonics, there are interleaved spurs [Fclock/2] ± [nFin] where n = 1 or 2.

4.9.3 Acquisition

Four buttons are available for acquisition:

- Snap: the acquisition will be run one single time
- Start: the acquisition will continuously run until a stop is done
- Stop: the acquisition will be stopped as soon as possible
- Trigger: the acquisition is launched once when there is a pulse on SYNC TRIG. The ADC needs to be in TRIGGER mode (Please refer to datasheet).The acquisition is triggered 5 clock cycles after the trigger reception.

The status is visible and the counter of acquisitions is updated.

Figure 4-78. Acquisition running

Figure 4-79. Acquisition launched through START and then STOPPED

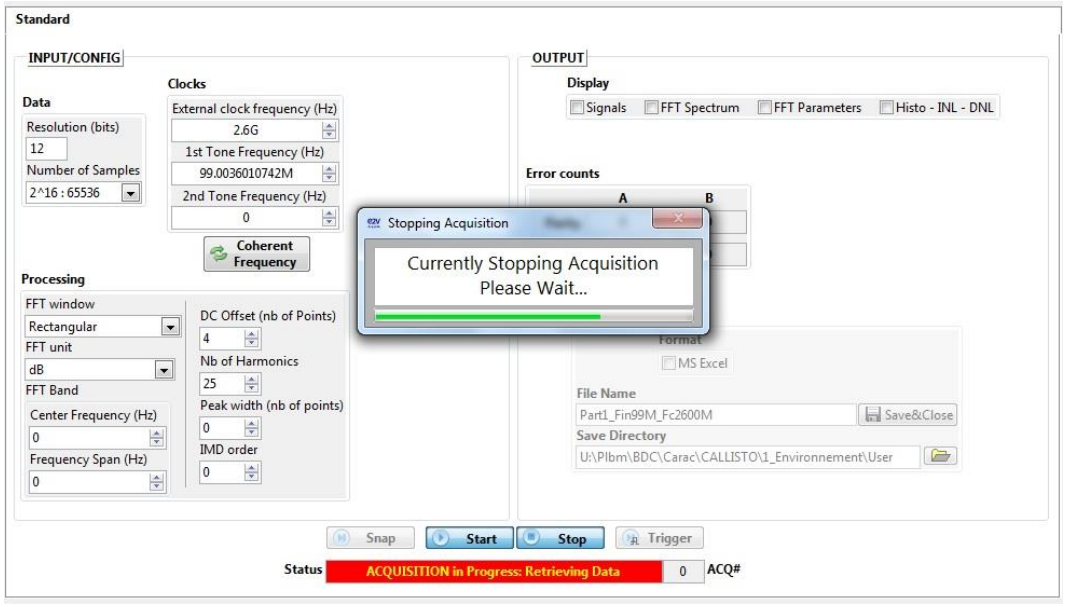


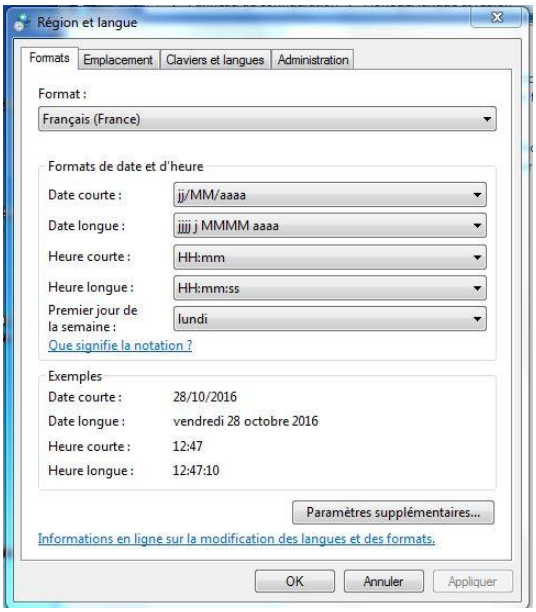
Figure 4-80. Acquisition done

4.10 Regional and language options

Use the Regional Settings window to check if decimal separator is configured with a dot “.”

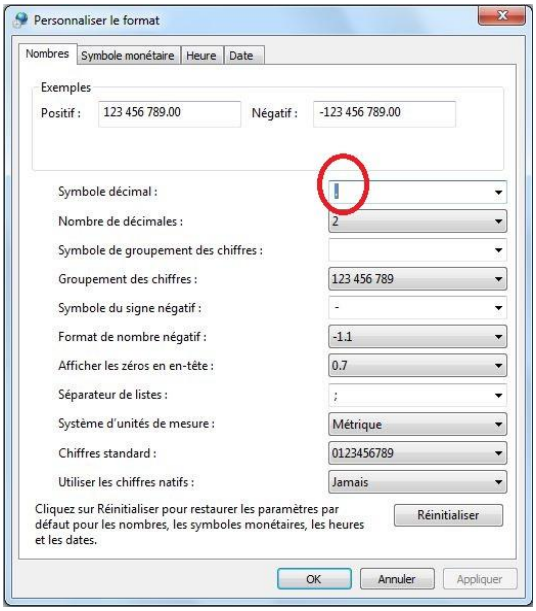
In regional and language options, select “customize this format”

Figure 4-81. Regional and language options window



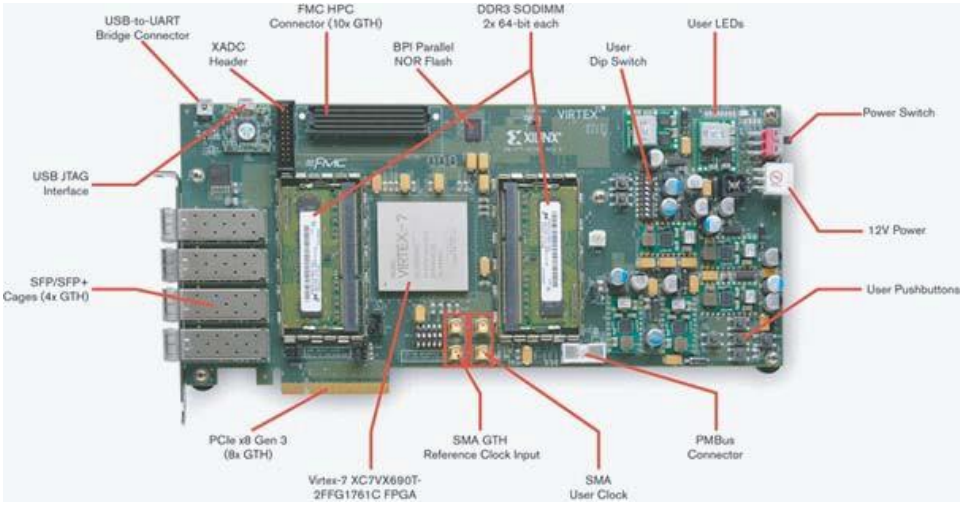
On this tab, the decimal separator must be configured with a dot ".".

Figure 4-82. Customize Regional option sheet numbers



Section 5. FPGA CODE

The FPGA code has been designed to be used with VC709 Xilinx Virtex 7 evaluation board.
Please refer to Xilinx: http://www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html



Warning: Please configure your VC709 evaluation board as follows: SW2: all OFF + SW11: 4 ON and 1/2/3/5 OFF.

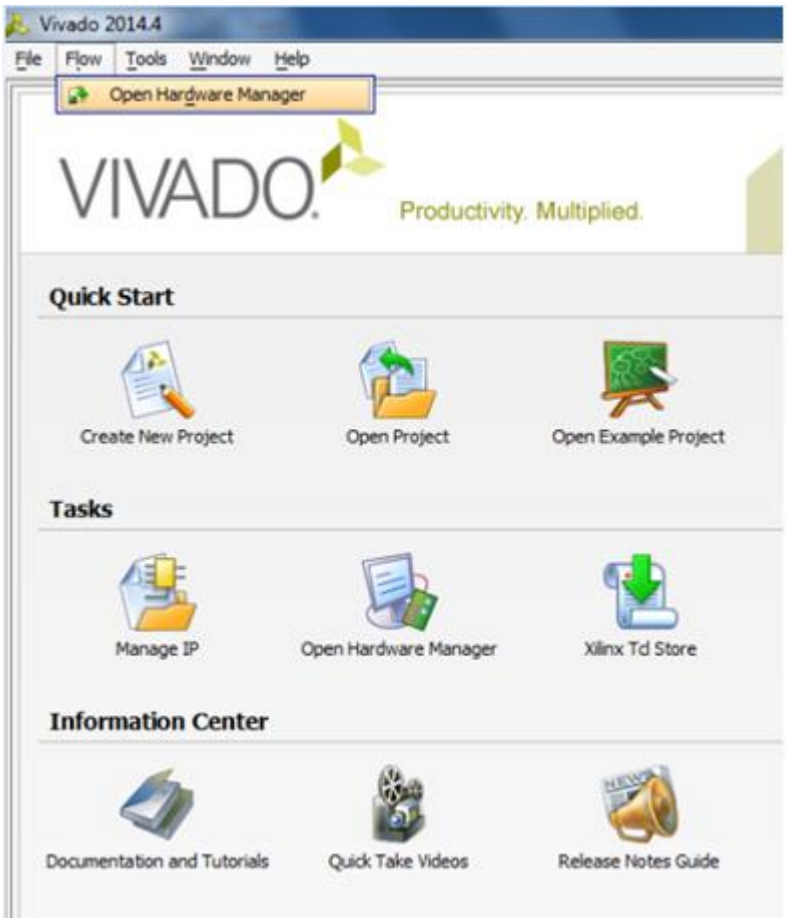
5.1 Software Configuration

Xilinx configuration: Virtex-7 FPGA VC709 Evaluation Kit Vivado 2015.4.

5.2 FPGA binary file

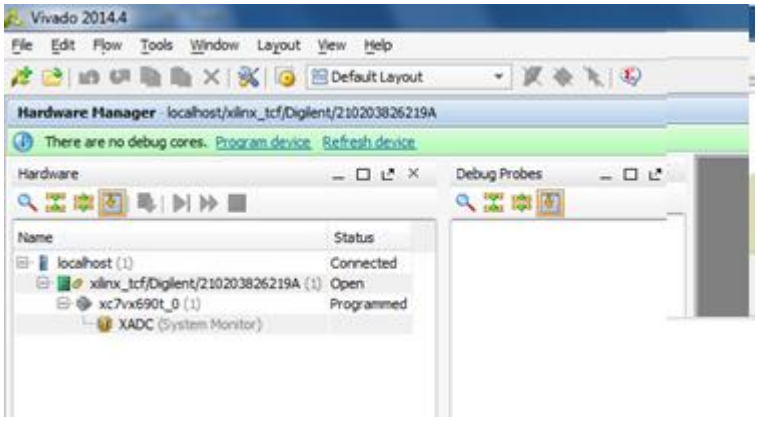
Loading .bit on VC709
Possible with Vivado.

Loading .mcs on VC709
Possible with Vivado 2014.1 onwards.
Start Vivado.
Flow => Open Hardware Manager

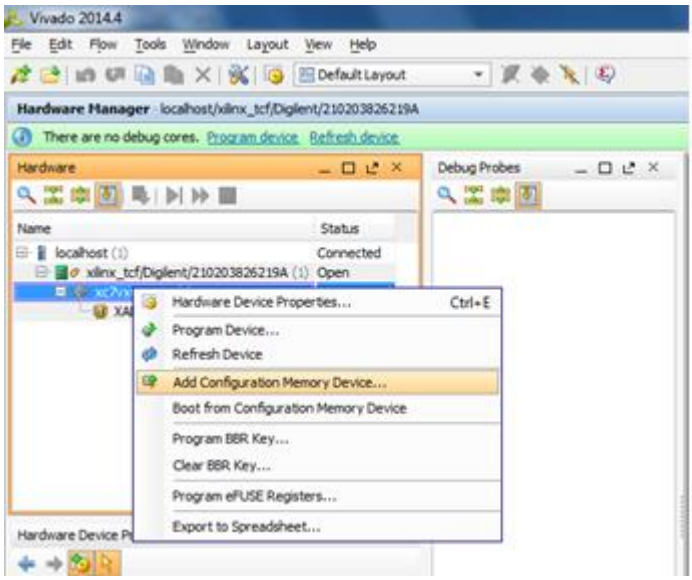


Open target => Auto Connect (The board has to be powered up at this time and the USB cable connected between J20 on board and PC).

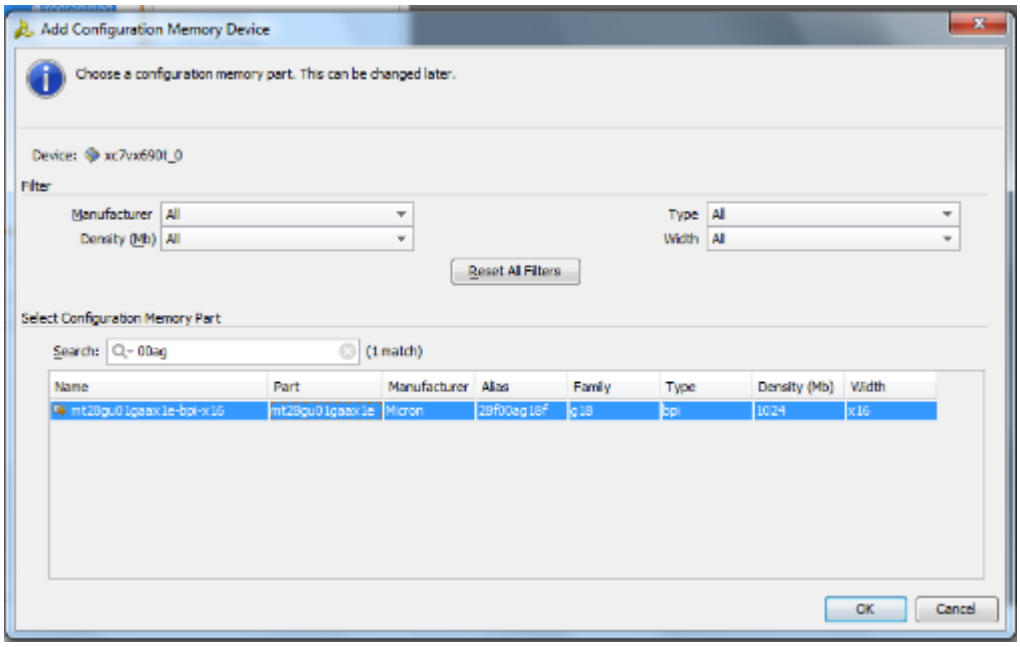
The FPGA is detected.



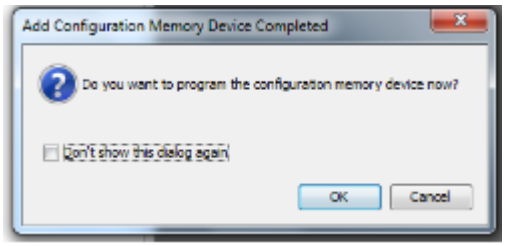
Right click on FPGA (xc7vx690t_0) => Add Configuration Memory Device



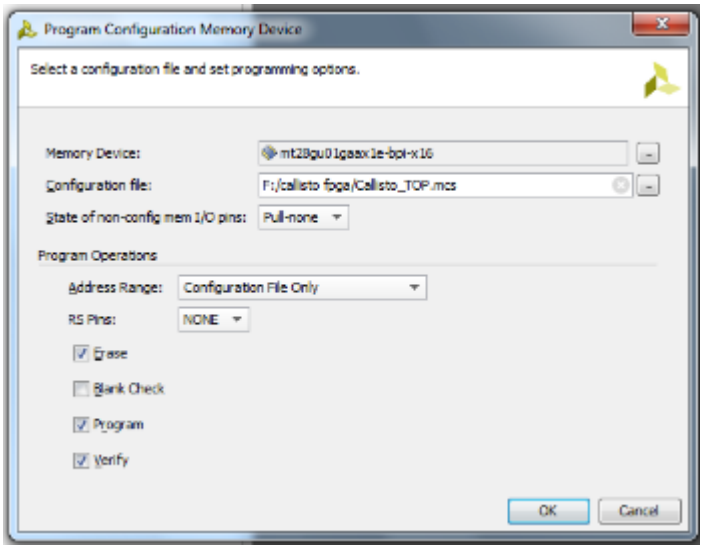
A new window appears to configure the memory device loading. This window asks for memory part number.
For VC709, it is the mt28gu01gaax1e-bpi-x16 (NB: there are 2 different memory part numbers that can be set up on the VC709).



Next pop-up will start the memory loading (if clicked on 'OK').



Next window lets you configure the loading. Keep the default value below and check that the correct .mcs is set up in Configuration file.



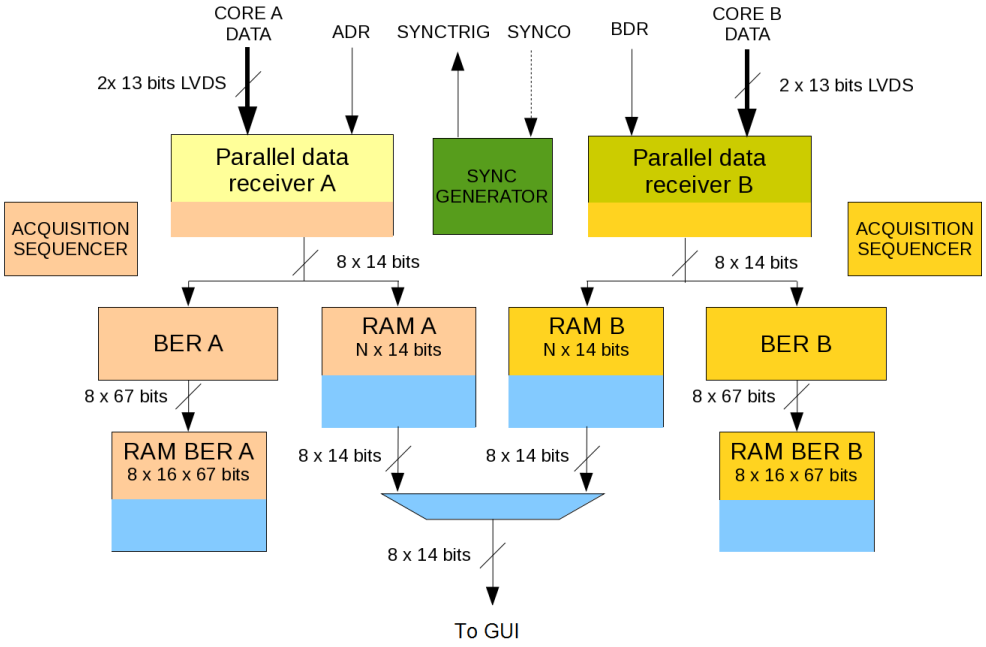
Click ‘OK’, the memory loading starts.

5.3 FPGA program architecture

EV12AD5x0x-EK Eval kit Functional Architecture

- Parallel Interface

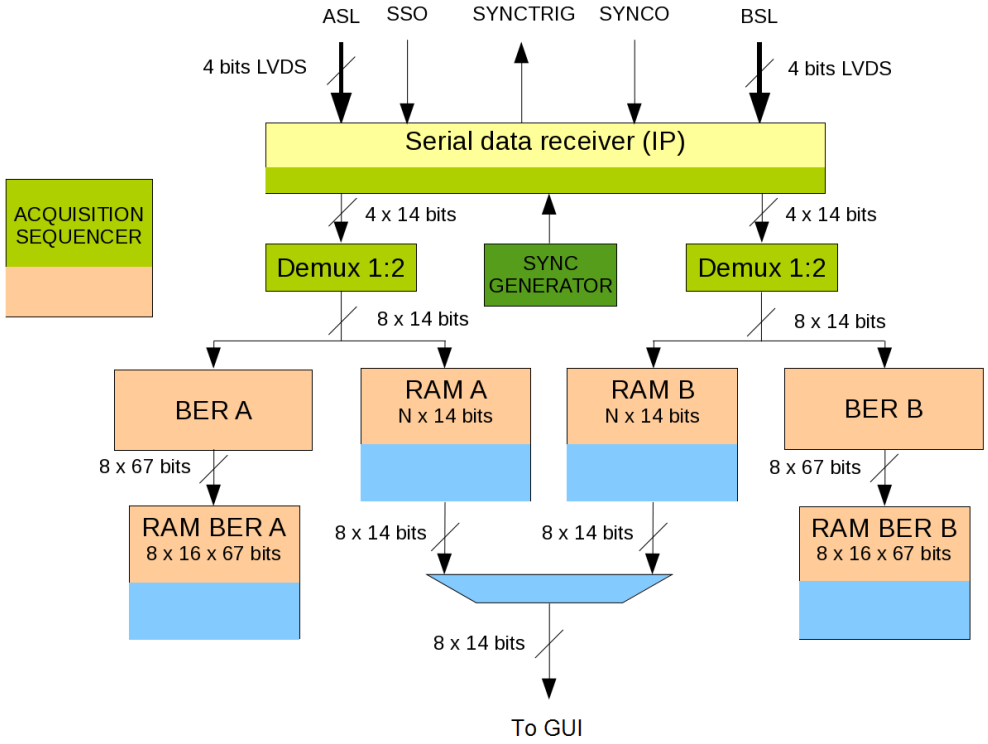
Figure 5-1. Functional architecture for parallel output



Color	Clock	Min frequency	Max frequency	Synchronized with
	Deserializer clock for core A	300 MHz	700 MHz	
	Deserializer clock for core B	300 MHz	700 MHz	Deserializer clock for core A
	Sync generator clock	MCLK freq	200 MHz	MCLK
	RAM and BER clock for core A	75 MHz	175 MHz	1/4 deserializer clock for core A
	RAM and BER clock for core B	75 MHz	175 MHz	1/4 deserializer clock for core B

- Serial Interface

Figure 5-2. Functional architecture for serial output

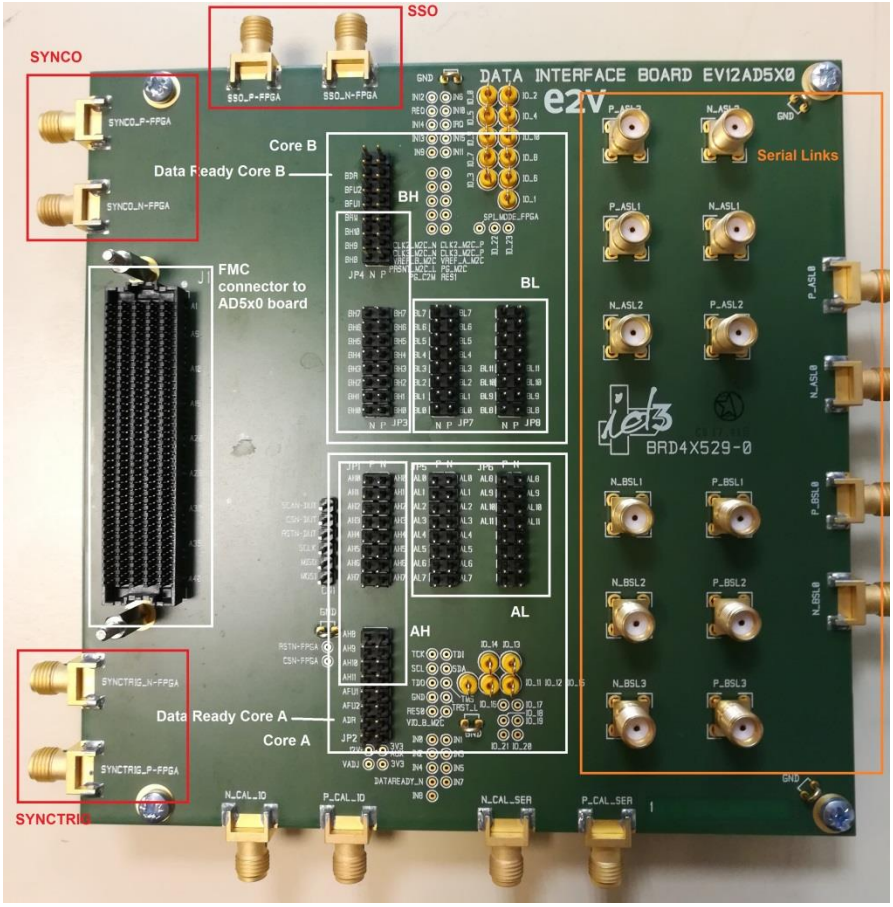


Color	Clock	Min frequency	Max frequency	Synchronized with
	Deserializer clock		6 GHz	
	IP output clock	2 x MCLK freq	375 MHz	
	Sync generator clock	MCLK freq	200 MHz	MCLK
	RAM and BER clock	PCLK freq	187,5 MHz	1/2 IP output clock

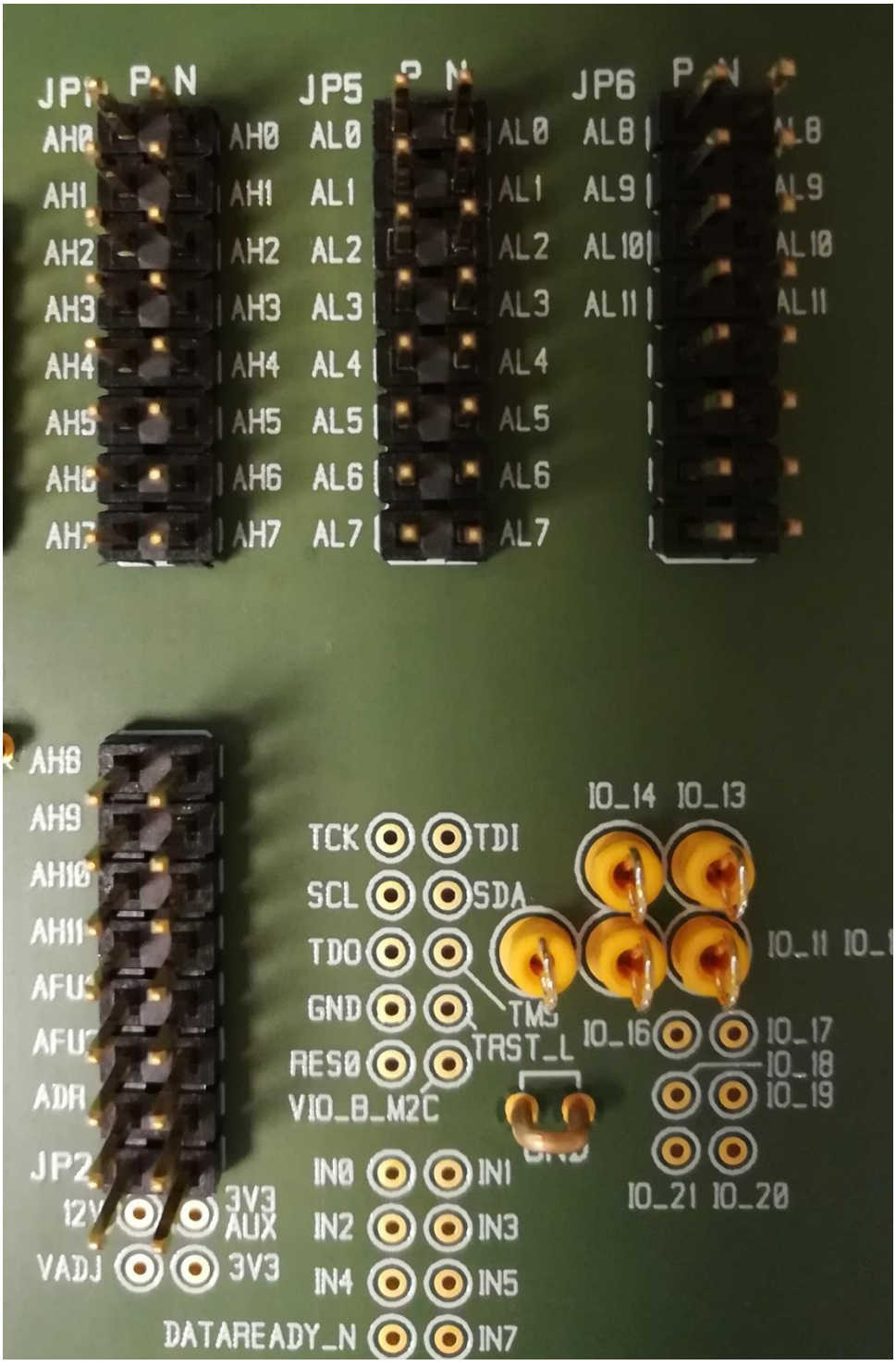
Section 6. DATA INTERFACE BOARD

The data interface board is provided with the evaluation kit. It is intended to be used with a logic analyzer. This section describes the board itself and the recommended connections to logic analyzer.

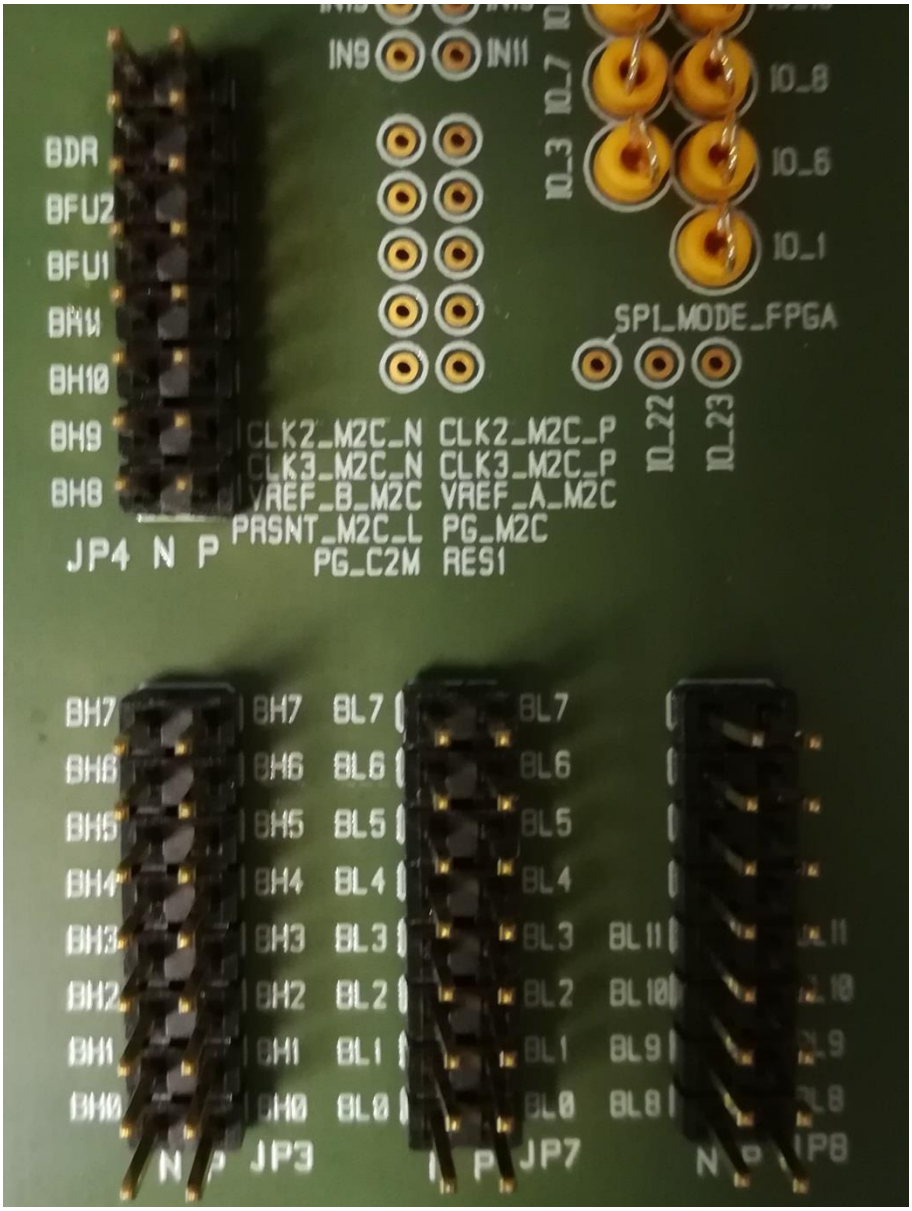
Global overview



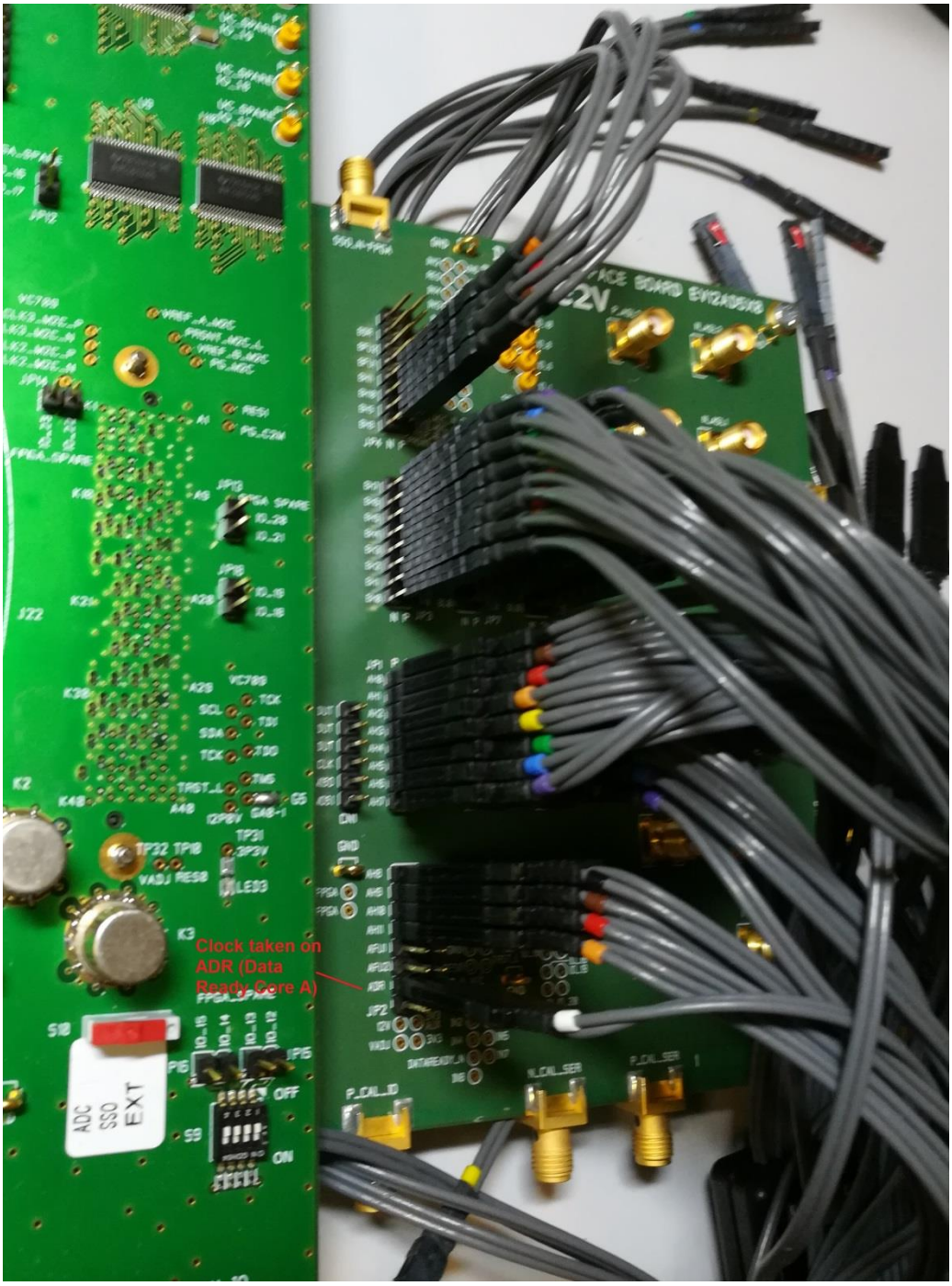
Zoom on core A



Zoom on core B



Board with the 2 boards connected to logic analyzer



Section 7. Ordering Information

Table 7-1. Ordering information

Part Number	Temperature	Comments
EV12AD550A-EK	Ambient	Contact sales for availability
EV12AD550B-EK	Ambient	Contact sales for availability
EV12AD500A-EK	Ambient	ROHS compliant Contact sales for availability

Note: For any technical questions, contact Teledyne e2v hotline (hotline-bdc@teledyne-e2v.com)

Section 8. Glossary

Abbreviation	Term	Definition
DNL	*Differential non-linearity*	The Differential Non Linearity for an output code "i" is the difference between the measured step size of code "i" and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification higher than -1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
ENOB	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$ Where A is the input amplitude and FS is the full scale range of the ADC under test.
GUI	*Graphical User Interface*	
IMD	*Intermodulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
INL	*Integral non-linearity*	The Integral Non Linearity for an output code "i" is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
JITTER	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
LDO	*Low-Drop Out regulator*	
ROHS	Restriction of Hazardous Substances	
SFDR	*Spurious Free Dynamic Range*	Ratio expressed in dB of the RMS signal amplitude, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SINAD	*SIgnal to Noise And Distortion ratio*	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SNR	*Signal to Noise Ratio*	Ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the 25^{th} first harmonics. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
SSO	*Slow Synchronization Output*	See datasheet for details
THD	*Total Harmonic Distortion*	Ratio expressed in dB of the RMS sum up to 25^{th} harmonic components, to the RMS input signal amplitude. It may be reported in dBFS (i.e., related to converter full scale), or in dBc (i.e., related to carrier signal level).
TSYNC	*SYNC duration*	External SYNC pulse width needed for SYNC function.