General Design Checklist for Broadband Data Converters

Introduction

This design checklist is a general checklist covering all aspects of circuit design incorporating e2v's high speed data-converters.

The checklist is meant for use in conjunction with each component's own application note which will describe in further detail the specific requirements for that product.

1. External Components

- Input amplifier (if used) has adequate parameters e.g. bandwidth, SFDR, THD etc.
- Ensure that input amplifier can operate with impedance load of ADC and common mode from ADC (if DC required).
- Check whether split supplies are required to obtain best amplifier performance.
- Ensure that phase margin is maintained for stability.
- Input balun (if used) has adequate bandwidth.
- Check that phase imbalance doesn't impact on performance.
- Check PLL / Clock generator has low enough phase noise.
- Check that amplitude of clock is within required value.
- Check that signal type is correct (sine wave, LVDS, PECL)
- Read Application note '0871B_InputClock_AN'.
- Ensure SPI signals have correct pull-ups.
- Ensure that FPGA inputs can accept data output from ADC (correct logic levels/timing).
- Ensure that FPGA inputs can drive data input of ADC (correct logic levels/timing).
- Check ADC output data clock goes to CLK input of FPGA.
- Ideally synthesise and place and route FPGA before fixing pins to ensure operation at high speed.
- Check power regulators have adequate capacity and have adequate thermal dissipation.
- Check dissipation of ADC and use appropriate heatsink if required.
- Use the thermal diode to monitor the temperature of the converter.

2. Electrical schematic

- Ensure that the input signal dynamic range covers the full range of the converter for optimum signal/noise.
- Ensure appropriate filtering, is performed prior to ADC to ensure optimum performance.
- Check that the recommended analog input and clock input configuration is used (differential? Single-ended?).
- Check the analog input and clock input termination (impedance of termination).
- Check whether AC or DC coupled analog input and clock input is recommended by device?
- Consider use of band-pass filter on clock to reduce phase noise.
- Check that the recommended output data configuration is used (differential? Single-ended?).
- Check the output data termination (impedance of termination).
- Check the reset signal is properly controlled (inactive by default).
- Check the function settings (pull up, down, potentiometer, dynamic control?).
- Check that Test and Scan inputs are correctly terminated.
- Check the bypassing and decoupling of the power supplies (number and value of decoupling capacitance).
- Ensure that supply power on/off sequence is followed (if device requires it).
- Check the unconnected pins.

3. Layout

- See Applications Note: '0983B_HF_Transmission_AN' and '0999B_Board_Layout_AN'.
- Board Placement: Ensure that Analog section of board is separate from digital section.
- Power supplies and ground layers: correct separation of what has to be separated.
- Ensure that Analog supplies of board are separate from Digital supplies.
- Ensure that PCB tracks for the high speed data are the correct impedance.
- Position of the terminations (close to the load if not AC coupled, otherwise close to the driver…).
- Position of the reverse terminations for the analog input (close to the pins).
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- Keep all traces matched to appropriate impedance (50 Ohm for 100Ohm differential inputs).
- Ensure line length matching for signals of the same function, of the same differential pair.
- For differential signals, keep the True and False signal traces close to one another;
- For single-ended signals, make sure that all signals are far enough from their neighbor to avoid crosstalk
- Ensure track propagation times for data signals are equal for all data clocked by same clock.
- To avoid cross talk route potential signals at right angles
- To avoid EMC problems route traces without angles (use arc traces where possible).
- Avoid using vias on signal tracks since they add inductance and capacitance.
- Use larger vias for decoupling capacitors place them touching the capacitor pad.
- Use surface mount low ESR capacitors for decoupling.
- Simulate if possible the digital outputs using Spice or IBIS simulator (Ansoft, Hyperlynx etc.) to check for overshoot/ringing, propagation time.

4. Board Commissioning

- Ensure that ADC control system (SPI) functions correctly.
- View the digital output data and data ready clock using a high speed 'scope; ensure that the set-up and hold times for the receiving device (FPGA etc) are met. Also check that logic levels are correct.
- Use test pattern generators in ADC to ensure correct bit correspondence in FPGA.
- For interlaced systems ensure that correct calibration procedure has been followed, gain, phase, offset.
- Ensure that device synchronisation has been correctly performed, also between changes of mode for some devices.
- Use good quality signal generator. If external clock is used the phase noise should be appropriate for the resolution required. E.g. 10 bit 1GHz BW, phase noise should be of order -160dBc.
- If possible measure clock jitter at ADC input
- For FFT measurements use 8192 samples or greater for optimum spectral resolution.
- If clock and signal are not synchronous, use window function of order 7.