

EV10AQ190x-DK

VITA 57 FMC Quad 10-bit ADC Demo Kit

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Section 1 General Overview

The QUAD 10-bit Demo Kit enables the easy evaluation of the characteristics and performance of QUAD 10-bit ADC EV10AQ190x. The Demo kit is plug_and_play and needs little external equipment.

The Demo kit is delivered with software which allows acquisition of data using the FPGA.

The QUAD 10-bit Demo Kit is compatible with VITA57 FMC (FPGA Mezzanine Card) standard.

For more information please see the VITA site web. <u>http://www.vita.com/fmc.html</u>

The QUAD 10-bit Demo kit is 100% compatible with XILINX VIRTEX 6 evaluation kit ML605.

This board is designed for use as a reference design.

All front end devices are fitted including: DC-DC regulator, ADC driver, clock generator....

Please see Section 3 "Main Functions" .

The FPGA VHDL data acquisition code for the ML605 board is supplied.

Please see Section 5 "FPGA CODE" .

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Its function is as a development system, demonstrating the performance of e2v semiconductors components and not as a final product available on general release.

Since this Development Kit is intended to be used on an industrial workbench and modified by the user to build his prototypes, NO WARRANTY OF ANY KIND can apply.

NO LIABILITY will be accepted by e2v, whatsoever may arise as a result of the use of these boards.

All company and/or product names may be tradenames, trademarks and/or registered trademarks of the respective owner with which they are associated.

1.2 Quad 10-bit ADC The EV10AQ190x-DK Demo Kit is based on e2v EV10AQ190x 1.25 Gsps Quad 10-bit ADC whose block diagram is given on Section 1-1.



Figure 1-1. EV10AQ190x Quad 10-bit ADC Block Diagram

The EV10AQ190x Quad 10-bit ADC integrates four 10-bit ADC cores which can operate independently (four-channel mode) or group by two cores (two-channel mode with the ADCs interleaved two by two) or one-channel mode where all four ADCs are all interleaved.

All four ADCs are clocked from the same external input clock signal and controlled via an SPI bus (Serial Peripheral Interface). An analog multiplexer (cross-point switch) is used to select the analog input depending on the mode the quad ADC is used.

The clock input is common to all four ADCs. This block receives an external 2.5 GHz clock (maximum frequency) and generates the internal sampling clocks for each ADC core depending on the mode used. Please refer to latest version of datasheet EV10AQ190x for more information.

http://www.e2v.com/products-and-services/specialist-semiconductors/broadband-dataconverters/datasheets/

1.3 Demo Kit

Figure 1-2 provides an overview of system architecture.

Figure 1-2. EV10AQ190x-DK Demo Kit System Architecture (when Connected with a VIRTEX6 Evaluation Kit)



The complete system is built with the e2v demo kit and an FPGA development kit. e2v Demo kit contains the following items :

- Quad 10-bit Demo kit with EV10AQ190CTPY ADC
- Cables & Power Supply
 - Universal 12V power Adapter & Cables
 - USB Cables to communicate with a PC (control of ADC settings and settings for data acquisition)
- 4 analog inputs with SMA connectors
- 1 clock input with SMA connector (if external clock input is programming)
- 2 SAMTEC MC-HPC-8.5L connectors HPC (High Pin Count) compatible with VITA57 standard for ADC LVDS digital outputs
- CD ROM with GUI Software
- Note: The ML605 VIRTEX 6 Evaluation kit with XC6VVLX240T-1FFG1156 FPGA is not supplied within the e2v kit and should be purchased separately from Xilinx or its authorised distributors.

General Overview

Figure 1-3. EV10AQ190x-DK Demo Kit Simplified Schematic



Figure 1-4. EV10AQ190x-DK Demo Kit Functional Architecture



Acquisition and formatting of ADC digital output data are done within the FPGA Eval Kit.

Data is then transmitted again to the ADC Demo Kit.

A USB driver on the ADC Demo kit allows for transmission of the data to the computer that performs the display and processing of ADC output data (FFT).

Software and Graphical User Interface are provided with the Demo Kit.

The provided software operates using Labview RunTime (no license required).

Section 2 Quick Start

Operating 1	. Install the Software as described in section 4 Software Tools.
Procedure 2	. Install the FPGA code into ML605 Xilinx evaluation board (see Section 5.3 "FPGA Programming")
3	. Turn OFF the ML605 Xilinx evaluation board.
4	. Fix Heatsink/Fan to the ADC if no external form of ventilation is to be used Section 3.4)
5	. Connect the QUAD 10-bit Demo Kit on ML605 Xilinx evaluation board.
6	. Connect the power supplies of both evaluation boards.
7	. Connect the USB cable.
8	. Turn ON power supplies of QUAD 10-bit Demo Kit.
9	. Turn ON power supplies of ML605 Xilinx evaluation board.
1	0. Launch the EvalkitQuadAdc10Bits.exe software.
1	1. Check if currents are correct (see Section 4.5.5 Power).
1	2. Select the ADC mode of your ADC (4 channels or 2 channels or 1 channel
1	 Turn the mode ADC test ramp active (see chap Section 4.5.2 TEST). This sequence is mandatory to allow the synchronization of 4 channels in FPGA
1	Launch acquisition and check if sample signal is correct.
1	5. Return to normal mode (Turn OFF Test mode).
1	6. Connect a RF generator on Analog input.
1	7. Turn on the RF generator.
1	8. Launch acquisition (see Section 4.5.7 Acquisition).
Troubleshooting	

- Check for the available disk space.
- Check that the USB port is free and properly configured.
 - QUAD 10-bit connected to USB 2 driver



Figure 2-1. USB Port Driver Configuration

Warning: this installation is done for one USB connector only. If USB connector is changed, USB driver need to be re-installed before use.

2.2.2	Start up Procedure	Check that supplies are properly powered on and properly connected.
-------	--------------------	---

- Check if the Xilinx FPGA evaluation board ML605 is properly configured with correct software.
- Check if QUAD 10-bit Demo Kit is properly plugged into FPGA connector.
- Check if USB connector is properly plugged.

2.2.3 Measurement Check if QUAD 10-bit ADC is properly configured in normal mode without standby and test mode.

Note: check if currents are correct (see Section 4.5.5 Power) Note: check if test mode is OFF (see Section 4.5.2 TEST)

- Check if acquisition mode is correctly configured.
- Warning: if no windowing is used or if signal is non coherent, FFT of Figure 6 is obtained



Figure 2-2. FFT without Windowing or with non Coherent Signal

Figure 2-3. FFT with Windowing



Warning: if the Fin frequency has an exact value such as 250 MHz the FTT result is wrong that is why it is recommended to perform measurements with shift of few MHz e.g. 250.2 MHz.





With channel A and channel C (amplifier channels) an RF attenuator should be added on the SMA connecter to have optimum performance. When these channels are not being used the attenuator or 50 Ohm terminator should be kept in place. This will prevent the amplifiers from adding noise into the system.





Check that the junction temperature of QUAD 10-bit ADC is lower than 105°C and that heatsink is properly connected.

Figure 2-6. Junction Temperature Monitoring with GUII



Check if acquisition is synchronous.

The ADC RAMP test procedure will set the ADC to output a ramp on each channel these ramps are synchronous at the output of the ADC after a SYNC process has been completed.

The FPGA RESET done during this procedure will always ensure that the 4 channels are acquired in the FPGA synchronously.

However if the channels are found not to be synchronous as shown in Figure 2-7.

Figure 2-7. Non Synchronous Channels



Return to ADC test mode disable -> Apply and then return into ADC test mode ramp mode -> Apply.

This will re-run the synchronization procedure of the ADC and FPGA..

Note: it is not always necessary to have the ramp patterns aligned to obtain correct data acquisition using the analog inputs.



Figure 2-8. Synchronous Channels

Note: it is not always necessary to have the ramp patterns aligned to obtain correct data acquisition using the analog inputs. Even if the ramp mode is not synchronous, you could return to the normal mode and perform one acquisition. Normally the acquisition of sinus wave in normal mode is correct.

2.3 External The QUAD Equipment ■ RF gener

The QUAD 10-bit Demo Kit needs very little external hardware.

- RF generator for Analog input signal
 - The QUAD 10-bit ADC can convert analog signals up to 2GHz
 - For optimum performance this generator must have a low phase noise
 - Please see Table 2-1 for example of signal generator.
- Cables & Power Supply (provided by e2v)
 - Universal 12V power Adapter & Cables
 - USB Cables to communicate with a PC (control of ADC settings and settings for data acquisition)
- PC with Windows
 - Windows 2000/98/XP and Windows NT and Windows 7 (note 32bit only)
 - Please see chap 4.1 Overview
- FPGA evaluation board compatible with VITA57 FMC standard
 - This Demo Kit board has been specially designed to be plugged with the XILINX VIRTEX 6 evaluation board EK-V6-ML605-G.
 The QUAD 10-bit Demo Kit could be used with other FPGA evaluation boards compatible with VITA57 FMC standard. However, an assessment of available connections should be made to ensure full compatibility.

Option

- RF generator for clock input signal whose frequency is different than 2 GHz
 - The QUAD 10-bit Demo Kit provides clock signal at 2 GHz using its own PLL
 - The QUAD 10-bit Demo Kit could be tested with other clock frequency

Please see Section 6.2 Clock selection

Table 2-1. Example of RF Generator

Signal Generator	SSB Phase Noise @ 1 GHz (20 KHz Offset)
Agilent E4424B 250KHz 2GHz (High spectral purity)	< -134dBc/Hz
Agilent E4426B 250KHz 4GHz (High spectral purity)	< -134dBc/Hz
SMA100A 9 KHz 6GHz (High spectral purity)	< -140dBc/Hz

Quick Start

Section 3 Main Functions

3.1 Analog Input Signal

The user only needs to provide an analog signal at the input.

This signal is digitized by the ADC depending on the chosen operating mode:

- 4 channel mode (1 channel per ADC core)
- 2 channel mode (2 interleaved ADC cores)
- 1 channel mode (4 interleaved ADC cores)

Each channel input is driven in different ways on the board:

- Single to Differential Amplifier from Analog Devices (A channel: ADA4960 D.C. coupled)
- Single to Differential Balun RF transformer (B channel:MACOM ETC1-1-13)
- Single to Differential Amplifier from Analog Devices (C channel: ADA4960- AC coupled)
- Direct input via SMA connector (D channel) (free for customer use)

Main Functions

<image>

3.1.1 Analog Input The Analog input channel A uses a differential amplifier (ADC driver) from Analog Devices ref: ADA4960.



Figure 3-2. Channel A : Schematic

The ADA4960 is used in DC configuration with output common mode driven by ADC QUAD 10-bit. The input is biased at 2.5V since this is a requirement for best performance from the amplifier, this should be taken into account when using this input.

Note: be careful that if a DC voltage is added after the RF generator output that this will not damage the generator.

The ADA4960 is used in AC configuration in channel C.

3.1.2 Analog Input The Analog input channel B uses an RF Transformer from MACOM ref: ETC1-1-13 / MABA-007159





3.1.3 Analog Input Channel C The Analog input channel C uses a differential amplifier (ADC driver) from Analog Devices: ref: ADA4960-1.





The ADA4960-1 is used in AC configuration with output common mode driven by Quad 10-bit ADC.

3.1.4 Analog Input This channel is free for customer use in differential and AC coupling configuration. Channel D





This Channel D could be used in DC configuration. Please see Section 6.1Channel D.

3.2 ADC Clock Input Signal ADC clock input is generated by Clock generated PLL Hititte HMC831 (on-board) at 2.0 GHz. This frequency is fixed.

Figure 3-6. ADC Clock Input : Schematic



Note: By default, the on-board PLL clock is selected but an external clock input (provided by a RF generator) is allowed.

The clock signal is fed to the board via an SMA connector followed by Single to Differential Balun RF transformer (MABA-007159 MACOM).

Note: for operation at different clock frequencies it is probable that the FPGA interface will need to be re-compiled using different timing constraints.

Please see Section 6.2 Clock selection.

3.3 Control of ADC Settings The Graphical User Interface allows for complete monitoring and control of all the settings of EV10AQ190x Quad 10-bit ADC such as channel selection, Gain, Offset, Phase, test mode (with SPI signal). Please see Section 4.5 Operating Modes.

Please refer to datasheet EV10AQ190x for more information.

http://www.e2v.com/products-and-services/specialist-semiconductors/broadband-dataconverters/datasheets/

By default the SPI signal is controlled by FX2 microcontroller but it could be driven by the FPGA. Please refer to Section 6.3 SPI Signal for more information.

3.4 ADC Junction Temperature Monitoring ADC junction temperature can be monitored by a temperature sensor from ON Semiconductors Ref: ADM1032 http://www.onsemi.com/PowerSolutions/product.do?id=ADM1032

Figure 3-7. Temperature Sense: Schematic



ADC junction temperature can be displayed on the PC via the GUI with a resolution of $\pm 2^{\circ}$ C. Please see Section 4.5.5 Power.

In case of excessive junction temperature, the ADC power supply will be turned OFF and a message will notify the user via the GUI.

The Demo Kit provides an external heat sink with internal fan

This heat sink should be fixed to the Quad 10-bit ADC with a thermal conductive foil both side adhesive.

If no other form of ventilation or cooling is to be employed the heatsink ventilator should be fixed to the ADC using the attachment pad provided and the cable should be connected to the connector as shown below.

Note that because of the location of the component underneath the board a heatsink/fan is necessary. Alternatively an airflow across the component can have sufficient cooling effect.

In other applications with the component positioned differently a simple heatsink (4°C/W max) will be sufficient.

Thermal analysis should be performed on any proposed arrangement.





3.5 ADC Current Consumption Monitoring

The ADC currents (I $_{\rm CC},\,I_{\rm CCO}$ and I $_{\rm CCD}$) can be measured by the Demo Kit.

Figure 3-9. ADC Measurement (Partial): Schematic



ADC currents (ICC, ICCO and ICCD) can also be monitored via the GUI. Please see Section 4.5.5 Power.

3.6 ADC SYNC Signal

The QUAD 10-bit ADC requires a SYNC signal when the internal configuration is changed (for example Channel configuration, DMUX configuration, test mode). The QUAD 10-bit Demo Kit performs this SYNC signal automatically when these modes are changed. The SYNC signal is driven by microcontroller FX2 and the D950LV0011 devices transform the single ended signal into an LVDS signal.

Figure 3-10. ADC SYNC Signal



Note: By default, the SYNC signal via FX2 is selected but a SYNC signal via the FPGA is allowed.

Please see Section 6.4 SYNC Signal.

3.7 DC/DC Converter The power supply for the QUAD 10-bit Demo Kit is provided by DC/DC block from Linear Technologies.

■ Vcc (3V3) power supply with micro module LTM8023

http://www.linear.com/pc/productDetail.jsp?navId=H0,C1,C1003,C1424,P39569

■ Vcco and Vccd (1.8V) power supply with micro module LTM8021

http://www.linear.com/pc/productDetail.jsp?navId=H0,C1,C1003,C1042,C1424,P81177

```
Main Functions
```

Figure 3-11. 3V3A Power Supplies



Figure 3-12. 1.8V Power Supplies



The amplifier and PLL power supply uses low noise LDO regulators from Linear Technology.

LT3029EDE

Figure 3-13.



Main Functions

1067BX-BDC-12/11

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EV10AQ190x-DK - User Guide

Section 4 Software Tools

4.1 Overview

The Demo Kit board needs three different kinds of software tools:

FPGA software

The Demo Kit board can be plugged with XILINX VIRTEX 6 evaluation board EK-V6-ML605-G

http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm

e2v provides FPGA program to be used with Quad 10-bit Demo Kit.

User Interface software

The User Interface software is a Visual C++ compiled graphical interface that does not require a licence to run on a Windows NT or Windows 2000/98/XP PC and windows7 (32 bit)

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

Display Software

The User Display software is Labview software that does not require a licence to run on a Windows NT or Windows 2000/98/XP PC and Windows 7 (32bit)

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

Warning: For the software installation, administrative rights are needed.

Warning: If the software is already installed a window appears.

Figure 4-1. Error Message if Labview Software is Already Installed



This applies when a previous version of software is present or a version of the Quad8 bit demo is present. When updating an installation it is recommended to uninstall the existing version (but not DK_DBC_Processing&Display).

If an other demo kit software, e.g. the DK-Quad8, is installed this can be left in place.

Click on OK and continue.

4.2	Configuration	The advised configuration for Windows 2000/98/XP and Windows NT is:	
		"PC with Intel Pentium Microprocessor of over 100 MHz;	
		"Memory of at least 24 Mo.	
		For other versions of Windows OS, use the recommended configuration from Microsoft.	
4.3	User Interface	1. Install the Quad 10-bit Demo Kit application on your computer by launching the	

The screen shown in Figure 4-2 is displayed:

available).



Setup	
	Welcome to the Evalkit Quad Adc 10Bits Setup Wizard This willingtal Evalkit Quad Adc 10Bits version 1.0.3 on your computer. It is recommended that you dose all other applications before continuing. Click Next to continue, or Cancel to exit Satup.
	Next > Cancel

2. Select Destination Directory

Figure 4-3. Quad 10-bit Demo Kit Application "Select Destination Directory"

Setup 🛛
Select Destination Location Where should Evalkit Quad Adc 10Bits be installed?
Setup will install Evalkit Quad Adc 10Bits into the following folder.
To continue, click Next. If you would like to select a different folder, click Browse.
C:\Program Files\E2V\EvalkitQuadAdc10Bits Browse
At least 91.6 MB of free disk space is required.
< Back Next > Cancel

3. Select Components (Start Menu Folder)

Figure 4-4. Quad 10-bit Demo Kit Application "Start Menu Folder"

Setup 🕅
Select Start Menu Folder Where should Setup place the program's shortcuts?
Setup will ore ate the program's shortcuts in the following Start Menu folder.
To continue, click Next, If you would like to select a different folder, click Brawse.
ELWerdint Jusc Acclueits Browse
< Back Next > Cancel

4. Select Components (Additional Tasks)

Figure 4-5. Quad 10-bit Demo Kit Application "Additional Tasks"

Setup 🔀
Select Additional Tasks Which additional tasks should be performed?
Select the additional tasks you would like Setup to perform while installing Evalkit Quad Adc 10Bits, then click Next. Additional icons: ✓ Create a desktop icon
< Back Next > Cancel

5. Select Components (Ready to Install)

Figure 4-6. Quad 10-bit Demo Kit Application "Ready to Install"

Setup 🗙
Ready to Install Setup is now ready to begin installing Evalkit Quad Adc 10Bits on your computer.
Click Install to continue with the installation, or click Back if you want to review or change any settings.
Install dependencies: Microsoft .NET Framework 2.0 SP1 vcredist_x86
Destination location: C:\Program Files\E2V\EvalkitQuadAdc10Bits
Start Menu folder: E2V\EvalkitQuadAdc10Bits
Additional tasks: Additional icons: Create a desktop icon
Back Install Cancel

If you agree with the install configuration, press Install button.

Install

Now a new process of installation started Processing&Display for installing Labview RunTime (no license required.

Please follow instructions.

Warning: don't press finish button on "Completing Setup wizard" window.

The screen shown in Figure 4-7 is displayed:

6. Select Components Processing&Display (installation Wizard)

Figure 4-7. Quad 10-bit Demo Kit Processing&Display "Installation Wizard"

讨 DK_BDC_Processing&Display Setup	
	Welcome to the DK_BDC_Processing <u>D</u> isplay Installation Wizard
	It is strongly recommended that you exit all Windows programs before running this setup program.
	Click Cancel to quit the setup program, then close any programs you have running. Click Next to continue the installation.
	WARNING: This program is protected by copyright law and international treaties.
	Unauthorized reproduction or distribution of this program, or any portion of it, may result in severe civil and criminal penalties, and will be prosecuted to the maximum extent possible under law.
	< Back Next > Cancel

7. Select Components Processing&Display (Destination Folder)

Figure 4-8. Quad 10-bit Demo Kit Processing&Display "Destination Folder"

🖟 DK_BDC_Processing&Display Setup	
Destination Folder Select a folder where the application will be installed.	
The installation wizard will install the files for DK_BDC_ProcessingDisplay in the following folder.	
To install into a different folder, click the Browse button, and select another folder.	
You can choose not to install DK_BDC_ProcessingDisplay by clicking Cancel to exit the installation wizard.	
Destination Folder C:\Program Files\DK_BDC_ProcessingDisplay\ Browse	
< Back Next > Cancel	

8. Select Components Processing&Display (Install the Application)

Figure 4-9. Quad 10-bit Demo Kit Processing&Display "Install the Application"

🔂 DK_BDC_Processing&Display Setup	
Ready to Install the Application Click Next to begin installation.	
Click the Back button to reenter the installation information or click Cancel to exit the wizard.	
< Back Next >	Cancel

The installation of the software is now completed but the Processing&Display software need to be launched. This installation is launched automatically.

9. Select Components Processing&Display (Completing Setup wizard" window)

Figure 4-10. Quad 10-bit Demo Kit Processing&Display "Completing Setup Wizard" Window"

🛃 DK_BDC_Processing&Di	splay Setup 📃 🗖 🔀
	DK_BDC_Processing <u>D</u> isplay has been successfully installed.
	Click the Finish button to exit this installation.
	< Back Finish Cancel

10. Select Quad 10-bit Demo Kit application (Completing Setup wizard" window)

Setup	
	Completing the Evalkit Quad Adc JOBits Setup Wizard Setup has finished installing Evalkit Quad Adc 10Bits on your computer. The application may be launched by selecting the installed icons. Click Finish to exit Setup. ✓ View the README file ✓ Launch Evalkit Quad10Bits
	Finish

Figure 4-11. Quad 10-bit Demo Kit Application "Completing Setup Wizard" Window"

Note about README message.

Please follow instruction before using Quad 10-bit Demo Kit application.

Figure 4-12. README Message

📕 ReadMe.txt - Bloc-notes	
Fichier Edition Format Affichage ?	
Release Note Demokit BDC	~
This document is the release note for the Demokit BDC	
version 1.0.1	
Supported OS: Win2000, Win XP 32, Vista 32, Seven 32	
Known bugs/limitations: - Bad Display in Excel report => Solution : In Control Panel Regional Settings, set the decimal separator to a dot '.'	
	×

For the bugs/limitation for Excel display, please see Section 4.5.10 Regional and Language Options.

4.4USB Driver
InstallationAfter the installation, Quad 10-bit Demo Kit can be powered up and connected to PC
with USB cable.

At the first connection a USB driver installation will be launched.

Warning: if the Demo Kit is connected to another USB connector this installation must be re-started.

The installation is normally fully automatic. If it is not launched automatically, please proceed as described below:

The window shown in Figure 4-13 will be displayed.

Figure 4-13. Install Driver Software

Please choose: Locate and install driver software (recommended)



Figure 4-14. Allow Windows to Search Driver

Please choose: Yes, always search online (recommended)



Figure 4-15. Browse the Driver Software

Please choose: Browse my computer for driver software (advanced)



Figure 4-16. Choose the Folder

Select C:\Program Files\E2V\EvalkitQuadAdc10Bits

C:\Program Files\e2v\EvalkitQuadAc	dc10Bits		Browse	
Include subfolders		(

Figure 4-17. Warning: Installation

Please choose: Install the driver software anyway



A Data transfer has been beginning please wait.
Figure 4-18. END of New Driver Installation

The new driver has been installed



After the installation, the interface can be launched with the following file: C:\Program Files\E2V\EvalkitQuadAdc10Bits\EvalkitQuadAdc10Bits.bat The window shown in Figure 4-19 will be displayed.

Figure 4-19. User Interface Demo Kit

			e2v				
eam	Start	ſ	Stop	7		Snap	
eneral				J			
hannel Select No	ine 🔻		< <hic< td=""><td>le Tab</td><td></td><td></td><td></td></hic<>	le Tab			
Status C	hannel ON / OF hannel Ready /	F 🔴 Busy 🔵	Channel . Channel I	A 🔴 B 🎱	Channel C Channel D	•	
settings Test	Gain / Offse	t / Phase	Input Imped	dance	Clock Po	wer Acqui:	sition
ADC Mode 4-channels 2-channels 	A and C, 2.5	Gsps per char	nel	-Genera -Outp	al Dut Mode Binary	O Gray	
 1-channel Simultaneous 	A, Sampling A	5 Gsps	•			(
				Bandw	ith selection	Nominal	•
Standby		-Synchroni Extra cloo	isation ck.cycles.befo	ore restar	t	Reset	
-	·	0	•			Hardware	Reset
No standby			0		15		

4.5 Operating Modes The Quad 10-bit ADC software included with the Demo Kit provides a Graphical User Interface to configure the ADC.

Push buttons, popup menus and capture windows allows easy:

- 1. Settings;
- 2. Test;
- 3. Gain / Offset / Phase;
- 4. Input Impedance;
- 5. Clock;
- 6. Power;
- 7. Acquisition;

With Setting, Test, Clock and Acquisition windows always click on "APPLY" button to validate any command.

Clicking the "CANCEL" button will restore last settings sent with "APPLY" button.

Figure 4-20. APPLY / CANCEL Buttons

APPLY	CANCEL

With Gain/Offset/Phase and INL windows always click on "Write" then "Send" buttons to validate any command.



Write	
Cancel	
Send	

The Reset button allows re-configuring ADC to the Default Mode.

Figure 4-22. Hardware Reset Button

-Reset	
Hardware Reset	

This user interface could be reduced using "Hide Tab", below.

Figure 4-23. Hide Tab Button

< <hide tab<="" th=""><th></th></hide>	
--	--

		e	2V	
tream	Start	SI	ор	Snap
General Channel Sele	act None	>>5	how Tab	
Status	Channel ON / OFF 🛛 🔴	Channel A 🔵	Channel C 🕥	
	Channel Ready / Busy 🥥	Channel B 🥥	Channel D 🥥	

Figure 4-24. Demo Kit User Interface with Hide Tab Configuration

On the bottom corner the software displays information about software and hardware revision.

- ChipId: revision of Quad 10-bit ADC
- Device: revision of FX2 software
- FPGA: revision of VHDL code

Figure 4-25. Software and Hardware Revision

ChipId:1.1.9 - Device:0.0.7 - FPGA:2.0:2.5 Ghz

4.5.1 Settings

Figure 4-26. User Interface Demo Kit

?				
	e2V			
ream	Stop		Snap	
Seneral Channel Select None 🔻	< <h< td=""><td>lide Tab</td><td></td><td></td></h<>	lide Tab		
Channel ON / OF Channel Ready	=F 🕚 Channe / Busy 🌒 Channe	IA 🔍 Cha IB 🌑 Cha	annel C 🔵 annel D 🥥	
ADC Mode 4-channels 2-channels A and C, 2.5 A, 1-channel A,	Gsps per channel 💌 5 Gsps 💌	General Output Mo	de O (Sray
Simultaneous Sampling		Bandwith sel	ection Nom	iinal 🔻
Standby No standby	Synchronisation Extra clock cycles be	fore restart	- Res	ardware Reset
APP	x]	CANC	:EL]	

In this window, 5 functions are available:

- ADC mode:
- General
- Standby
- Synchronization
- Reset

ADC mode:

4-channels mode = the 4 ADCs work independently at Fclock/2 sampling rate (where Fclock is the external clock signal frequency).

Figure 4-27. ADC Mode: 4-channels Mode

ADC Mode	
4-channels	
O 2-channels	and C, 2.5 Gsps per channel 💌
O 1-channel	A, 5 Gsps 💌
O Simultaneous Sampling	A

2-channels mode = the 4 ADCs are interleaved 2 by 2 (A & B, C & D), the sampling rate is equal to Fclock (where Fclock is the external clock signal frequency), the analog inputs can be applied to A or B and respectively C or D.

Figure 4-28. ADC Mode: 2-channels Mode

ADC Mode	
O 4-channels	
2-channels	A and C, 2.5 Gsps per channel
1-channel	A and C, 2.5 Gsps per channel B and C, 2.5 Gsps per channel A and D, 2.5 Gsps per channel B and D, 2.5 Gsps per channel
 Simultaneous Sampling 	

- I channel mode = the 4 ADCs are all interleaved, the sampling rate is Fclock x 2 (where Fclock is the external clock signal frequency), the analogue input can be applied to either A, B, C or D channel.
- Note: because of limitation of ML605 evaluation board (LVDS max 1GHz in speed grade -1) The capture of Quad 10-bit data is limited to 2 GSps.

Figure 4-29. ADC Mode: 1-channel Mode

ADC Mode	
4-channels	
O 2-channels	id C, 2,5 Gsps per channel 💌
1-channel	A, 5 Gsps 💌
Simultaneous Sampling	A, 5 Gsps B, 5 Gsps C, 5 Gsps D, 5 Gsps

Simultaneous channel mode = the analog input signal of channel A or B or C or D is sent to the 4 ADCs work at the same clock (4 ADC with the same timing) with Fclock/2 sampling rate (where Fclock is the external clock signal frequency).

Figure 4-30. ADC Mode: Simultaneous Sampling

ADC Mode	
O 4-channels	
O 2-channels	d C, 2.5 Gsps per channel 💌
O 1-channel	A, 5 Gsps
Simultaneous Sampling	A 🗸
Standby	B C D

General setting:

Output mode = Gray coding or Binary coding



Bandwidth selection: Nominal give 1.5 GHz bandwidth at -3dB;
 Full gives 3.2GHz bandwidth at -3dB;

Bandwith selection	Nominal
	Nominal
	Full

Standby setting:

- No standby = all channels are active (A: ON, B: ON, C: ON, D: ON);
- Partial standby = either A & B are in standby or C & D are in standby;
- Full standby = all 4 ADCs are in standby.

Figure 4-31. Standby Configuration



Synchronization:

Synchronization: programs the number of clock cycles prior to output clock restart after SYNC reset

Figure 4-32.	Extraclock	Configuration
--------------	------------	---------------

Synchronisation	Synchronisation
Extra clock cycles before restart	Extra clock cycles before restart
0	15
0 15	0 15

Reset:

 Synchronization: programs the number of clock cycles prior to output clock restart after SYNC reset;

Figure 4-33. Hard Reset

ſ	Reset
	Hardware Reset

4.5.2 TEST

In this window, the test mode is available:

A ramp test is generated within each ADC and output

Figure 4-34. Test Ramp Test Mode

Settings	Test	Gain / Offset / Phase	Input Impedance	Clock	Power	Acquisition	
r_Test Mod	e ———						
🔵 Dis	able						
• AD	С	Ramp	🔘 Fla	ashing [Flashing 11	mode 💌	
O FP	GA						

Note: this mode allows synchronizing the 4 channels of ADC with the FPGA RESET.

The synchronizing procedure can be initiated by checking the Disable button and then the Apply button : Then check the ADC and Ramp button and then Apply. Then retrun to normal operation by checking the Disable button and clicking on Apply.

A flashing bit is generated with one bit at 1 within each ADC and output is following with ten bit at 0 (1 FF pattern every ten 00 patterns) or after every 11 or 15 zeros depending on the selection.

Figure 4-35. Flashing Test Mode

Settings Test	Gain / Offset / Phase Ir	nput Impedance Clock	Power Acquisition	
Test Mode]
🔵 Disable				
• ADC	O Ramp	Flashing	Flashing 11 mode Flashing 11 mode	
O FPGA			Flashing 12 mode Flashing 16 mode	

FPGA Test (for testing communication between Demo kit and FPGA) : ramp test

Figure 4-36. FPGA Test Mode

Settings Test	Gain / Offset / Phase Input Impedance Clock Power Acquisition
Test Mode	
🔘 Disable	
O ADC	Ramp Ilashing Flashing Ilashing
• FPGA	

Gain / Offset / Phase

. (
		e2V		
ream	Start	Stop	Snap	
ieneral Thannel Select	None 💌	< <hide tab<="" td=""><td></td><td></td></hide>		
Status	Channel ON / OFF 🛛 🕚 Channel Ready / Busy 🌑	Channel A 🧕 Channel B 🔵	Channel C 🤏 Channel D 🌘	
Settings Te	est Gain / Offset / Phase	Input Impedance	Clock Power	Acquisition
-8,300	-8.3 8.284 Cance	-15,000	-15 14.971	Write Cancel
Internal Gain	-8.3 Send	Internal Ph	ase [-15]	Send
Offset (LSB)	Write			
(-40,000	-40 39.922 Cance	=		
Internal Offs	et -40 Send			

In this window, it is possible to adjust gain, offset and phase of the selected channel via the "channel select" button on the top left of the user interface.

A LED shows if the channel is ON (active - green LED) or OFF (not active - red LED) and if the same channel is ready (ready to receive gain, offset or phase orders - green LED) or busy (not ready to receive new calibration orders - red LED).

Figure 4-38. Channel Selection

Channel Select	None	< <hide tab<="" th=""><th></th></hide>	
Status			
	Channel ON / OFF 🛛 🔴	Channel A 🥥	Channel C 🥥
	Channel Ready / Bucy	Chappel B	Channel D

Once a channel has been selected, gain/offset/phase of this channel can be adjusted:

- you first need to enter the desired value for the gain/offset/phase thanks to the cursor;
- if you need to retrieve the old value of the gain/offset/phase click CANCEL;
- then you should WRITE this value to the internal registers by clicking on the WRITE button,
- if several adjustments are needed (gain AND offset AND phase), then select each value and then click on the respective WRITE buttons;
- once all adjustments are made via the WRITE buttons, orders to the ADC SPI can be sent using the SEND button;
- the calibration is successful if the internal gain/offset/phase boxes display the entered values.

If a new value for the gain/offset/phase has been entered by mistake, it is possible to retrieve the initial value by pushing the CANCEL button.





In the following example, it can be seen that the internal Gain register is set to 0.059 and that the user wants the phase to be set to -15. In the second picture, the WRITE and SEND buttons have been pushed and the internal register shows the new entered value for the phase.

Figure 4-40. Gain Write Send Sequence

Gain (dB) Write	-Gain (dB)
-8.3 8.284 Cancel	-8.300 -8.3 8.294 Cancel
Internal Gain -0.664648 Send	Internal Gain -8.3 Send

4.5.3 Input Impedance

Figure 4-41. User Interface Demo Kit - Input Impedance Settings

ezy Evalkit Quad 10 bits	
File ?	
eev	
C. C	
Stream Start Stop Snap	
General	- i
Channel Select None	
Status	
Channel ON / OFF • Channel A • Channel C •	
Channel Ready / Busy 🔍 Channel B 🔍 Channel D 🔍	
Settings Test Gain / Offset / Phase Input Impedance Clock Power Acquisition	
Input impedance Trimmer	
Write	
60,000	
60 42.31	
Cancel	
	64
ChipId:4.1.8 - Device:1.0.0 - FPGA:0	.64

In this window, it is possible to re-adjust the internal input resistor, which should be matched to 50Ω . The procedure is similar to the previous ones:

- select the channel where you need to adjust the input impedance
- check that the channel is ON and READY (green LEDs)
- enter the resistor value
- push the WRITE button to write these values to the internal registers (you can retrieve the initial value of the impedance by clicking on the CANCEL button)

Figure 4-42. Input Impedance Write Sequence

Input impedance Trimmer	Write	Input impedance Trimmer		Write
60.000 C 60 42.31	Cancel	42.310	60 42	=0 .31 Cancel

This function helps to re-adjust the input impedance in case of a slight mismatch due to temperature variations or process variations.

4.5.4 CLOCK

This sheet allows selection between the Internal PLL or external clock.

Figure 4-43. User Interface Demo Kit - Clock Settings

Eval Kit Quad ADC 10 Bits				
le ?				
	¢	2V		
Stream Start		Stop	Snap	
General				
Channel Select None 💌	•	<hide tab<="" td=""><td></td><td></td></hide>		
Status Channel ON / Channel Read	OFF Channel A y / Busy Channel B	 Channel C Channel D 	•	
Settings Test Gain / Ol	iset / Phase Input Impedar	nce Clock Po	wer Acquisition	
Clock selection				
 Internal clock (PLL) 				
🔲 Pll enable				
PII-				
Output Frequency	2000 MHz	-		
Output Strength	400 mVpp	a		
O External clock				
40 MHz				
	APPLY		CANCEL	
		Chip	Id:4.1.8 - Device:1.0.1 - FPGA:Mis	sing:??? Gh

Note: because of limitation of ML605 evaluation board (LVDS max 1GHz in speed grade -1). The capture of Quad 10-bit data is limited to 2 GSps.

4.5.5 Power

This sheet allows measurement of the Quad 10-bit power consumption and the internal junction temperature.

Figure 4-44. User Inte	erface Demo	Kit - Power
------------------------	-------------	-------------

Y Evalkit Quad	10 bits			
ile ?				
		e2V		
Stream				
Stream	Start	Stop	Snap	
General				
Channel Select	None	< <hide tab<="" td=""><td></td><td></td></hide>		
Status				
	Channel ON / OFF (Channel A 🤍	Channel C 🔍	
	Channel Ready / Busy 🤇	Channel B 🤍	Channel D 🔍	
Settings Te	est 🔰 Gain / Offset / Phase	e Input Impedance	Clock Power	Acquisition
Consumption]	Power	Temp	perature
Vcc 1642.	21 mA			
Vcco 192.5	54 mA	6.11248	Watt 97	∘⊂
Vccd 1.302	49 mA			
			ChipId:4.1.9 - Device	1.0.0 - EDCA:0.44
			Cripid, 1,1,0 - Device	110.0 TT GH.0.0T

4.5.6 Acquisition Control

This sheet controls the acquisition modes of the Quad 10-bit.

Figure 4-45. User Interface Demo Kit - Acquisition Control

^{ezv} Evalkit Quad 10 bits				
File ?				
		e2v		
Stream				
Start		Stop	Snap	
General				
Channel Select None	-	< <hide tab<="" td=""><td></td><td></td></hide>		
Status	-			
Channel	ON/OFF 🟓	Channel A 🙂	Channel C ២	
Channel	Ready / Busy 🕒	Channel B 🔍	Channel D 🤍	
Settings Test Gair	n / Offset / Phase J	input Impedance	Clock Power Acquisit	ion
Resolution in bits 10		Sampling Nbr 40	096	
Sample Format Single10	Coding Binar	y 🔻 Payload	Size in bytes 2048	
Nb Harmonics 10 🜩		FFT unit dB	•	
FFT Window 7 Term B-Ha	rris 🔻	Peak widt	th 11 🚔	
Analog Input Frequency (f	4Hz) 800,000 韋	Bypass Interlacin	g (ADC mode 1 or 2 channels	only)
Datas Saving				
Save to Excel file :				
Sampled signal	FFT Spectrum	🔲 FFT Paramet	ers 📃 INL Coefficients	
Display Graph				
🗙 Sampled signal	🗶 FFT Spectrum	🗙 FFT Parame	ters 🗙 INL Coefficients	
Overrange				
Ch. A	Ch. B	Ch. C	Ch. D	
	APPLY		CANCEL	
		C	nipId:4.1.8 - Device:1.0.0 - FF	GA:0.64

Sampling Nbr:

Number of samples in acquisition

Must be a 2n For FFT N=4X2n (n=number bit of ADC). For INL N=16X2n (n=number bit of ADC) Example for 10-bit ADC FFT must be computed with 4096 points and INL with 16384 points

Nb Harmonics:

Number of Harmonics considered for THD and SNR calculation (Default value is 10 harmonics).

FFT window:

When the analog input signal and the sampling clock are not coherent signals, a FFT windows has to be applied to obtain a correct result.

Analog Input Frequency:

For use when the analog input is not the highest amplitude. Normally the systems takes the highest harmonic as H1.

Bypass Interlacing

This can be used in 1 or 2 channel modes for viewing the non-interlaced data.

Peak width:

When FFT windows is applied the Harmonic signal is composed of several points (Default value is 11).

Figure 4-46. FFT Window Configuration

FFT Window	7 Term B-Harris 💌	Peak width 🚺 🔷
Analog Input	None 7 Term B-Harris	

Data can be saved in Excel file

Figure 4-47. Save Data Configuration

Save to Excel file : Sampled signal FFT Spectrum FFT Parameters INL Coefficients	Datas Saving			
Sampled signal FFT Spectrum FFT Parameters INL Coefficients	Save to Excel file :			
	X Sampled signal	🗶 FFT Spectrum	🗙 FFT Parameters	X INL Coefficients

Select directory

Figure 4-48. Directory Selection

Save to Excel F	ile			? 🔀
Enregistrer dans : Mes documents récents Bureau Mes documents Poste de travail	EvalkitQuadAd	c10Bits	← 🗈 📩 🖬	
Favoris réseau	Nom du fichier :		<u> </u>	Enregistrer
	Туре:	Excel files (*.xls)	•	Annuler

Note: A manual operation is needed to name and save the file.

4.5.7 Acquisition

The stream function can be used to start an acquisition

- Snap: for single acquisition
- Start for continuous acquisition, (stop acquisition with the stop button)

Figure 4-49. User Interface Demo Kit - Stream Function

ile ?		
	ezv	
Stream		
Start	Stop	Snap

When an acquisition is launched several window results appear:

CH_A => ADC channel A

- CH_C => ADC channel C
- CH_D => ADC channel D



Figure 4-50. Sample Signal: Example of Signal in Simultaneous Channel







Figure 4-52. FFT Spectrum Example



FFT	parame	ters					X
	[СН_В]				THD (dBc)	THD (dBFS)	
		Frequency (Mhz)	dB	F.	-51,77	-52,95	
	HO	0,000000	3,09		SINAD (dBc)	SINAD (dBFS)	
	H1	104,980469	-1,18		48,79	49,97	
	H2	209,960937	-56,37		SFDR Freque	ncy (Hz)	
	H3	314,941406	-59,45		209.9609	37M	
	H4	420,043945	-63,45		SEDR (dBc)	SEDR (dBES)	
	H5	474,975586	-73,26				
	H6	370,361328	-85,15		-55,19	-56,37	
	H7	265,014648	-72,53		SNR (dBc)	SNR (dBFS)	
	H8	160,034180	-77,28		51,84	53,02	
	H9	54,931641	-82,98		ENOB	ENOB_FS	
	H10	50,048828	-70,28		7.81	8.01	
	I				SESR (dBc)		
	I		_		-1.18		
	I				FloorNoise(dE	3)	
					-85.93		
	L				,,		
	I						
				7			
	P	·					

Plot selection: one channel or several channels can be plotted for easier reading.





Figure 4-55. Zoom Selection: Several Kinds of Zoom can be chosen



Figure 4-56. Lock Selection



Software Tools





FFT parameters: this channel selection has to be used to see FFT parameters of several channels

Selection 0 => ADC Channel A Selection 1 => ADC Channel B

Selection 2 => ADC Channel C Selection 3 => ADC Channel D

Figure 4-58. FFF Selection

[CH_B]			THD (dBc)	THD (dBFS)	5 ² [CH_C]			THD (dBc)	THD (dBFS)
	Frequency (Mhz)	dB 🥖	-53.19	-55.43		Frequency (Mhz)	dB	-52.11	-56.24
10	0.000000	3.09	SINAD (dBc)	SINAD (dBFS)	HO	0.000000	2.92	SINAD (dBc)	SINAD (dBF
	101.074219	-2.24	48.52	50.76	H1	409.912109	-4.12	46.28	50.41
2	201.904297	-65.97	SEDR Freque	ncv (Hz)	H2	179.931641	-62.53	SFDR Freque	ncy (Hz)
3	302.978516	-57.48	202 0705	16M	H3	229.980469	-64.56	170 0216	41M
1	404.052734	-74.22	502.9765	CEDD (HDEC)	H4	360.107422	-64.06	(dp.)	CEDD /JDEC
5	494.873047	-78.64	SFDR (dBc)	SEDK (GBES)	H5	50.048828	-68.29	SFDR (dBC)	SFUR (dbF:
6	394.042969	-71.20	-55.24	-57.48	H6	459.960937	-74.45	-58.40	-62.53
7	292.968750	-61.85	SNR (dBc)	SNR (dBFS)	H7	130.126953	-71.29	SNR (dBc)	SNR (dBFS)
1	190.917969	-82.77	50.33	52.57	H8	280.029297	-64.92	47.60	51.72
	91.064453	-70.02	ENOB	ENOB FS	H9	310.058594	-72.29	ENOB	ENOB FS
0	10.253906	-81.25	7 77	9 14	H10	100.097656	-76.72	7.40	0.00
1	111.816406	-79.71		0.14	H11	491.943359	-77.08	7.40	0.00
12	211.914062	-83.10	SFSR (dBC)		H12	79.833984	-72.01	SESR (dBc)	
113	312.988281	-80.02	-2.24		H13	330.078125	-76.30	-4.12	
			FloorNoise(dB	3)				FloorNoise(dB)
			-83.32					-82.74	

FFT Processing:

For future calculations, we define:

Sig = Signal power level =
$$\sum_{0}^{N} {}^{\text{""}} \text{spectrum}_{i}^{2}$$

Ho = Power of the continuous component = $\sum_{0}^{\text{setup.PeakWidth}} {}^{\text{spectrum}_{i}^{2}}$
H1 = Power of the fundamental = $\sum_{j}^{N} {}^{\text{spectrum}_{i}^{2}}$
setup.cal..Nbr of Harmonics ""setup.PeakWidth
Hi = Power of the harmonics = $\sum_{\text{Harmonics}}^{N} {}^{\text{spectrum}_{i}^{2}}$

with: setup_PeakWidth = 1 = width of one spur given in number of points; setup_cal_NbrOfHarmonics = 5 or 10 = number of harmonics used for the spectral calculations

PmaxSpur = Power of the highest spur excluding the continuous component and the fundamental

setup.PeakWidth =
$$\sum_{j}$$
 spectrum_i²

$$SFSR_{dBc} = H1_{dB}$$
Average Noise_{rms} = $\sqrt{\frac{Sig - H0 - H1}{N_{sig} - N_{H0} - N_{H1}}}$ N = number of points

$$THD_{dBc} = 10 \log \frac{H1i}{H1}$$

$$SNR_{dBc} = 10 \log \frac{H1}{Sig - H0 - H1 - H1i}$$

$$SFDR_{dBc} = 20 \log \frac{Harmonic_{rms}}{fundamental_{rms}}$$

$$SINAD_{dBc} = 10 \log \frac{Sig - H0 - Average Noise^{2}rms}{Sig - H0 - H1}$$

$$ENOB = \frac{SINAD_{dB} - 10 \log 1.5}{6.02}$$

$$THD_{dBFS} = THD_{dBc} + SFSR_{dBc}$$

$$SNR_{dBFS} = SNR_{dBc} - SFSR_{dBc}$$

$$SFDR_{dBFS} = SFDR_{dBc} + SFSR_{dBc}$$

$$SINAD_{dBFS} = -10 \log(10^{(-SNR_{dBFS}/10)} + 10^{(THD_{dBFS}/10)})$$

$$\text{ENOB}_{\text{dBFS}} = \frac{\text{SINAD}_{\text{dBFS}} - 10 \log 1.5}{6.02}$$

The parameters with the _FS prefix correspond to the same parameter but in dBFS (from full scale).

4.5.8 Demo Kit It is possible to save the context of the Demo Kit (saving of all settings and configuration File configuration).

This context can be saved for later use, so that saved settings can be reloaded. File DK BDC QUAD10bit Conf.ctx





Warning: for each channel A B C D don't forget to push the SEND button to perform this setting on each sheet (Setting, Gain/Offset/Phase, INL...).

4.5.9 Data Save File

- It is also possible to save the data of your acquisition (saving of all data samples and FFT result). This data is stored into an Excel file with different sheet:
 - Sample signal: Data of Quad 10-bit ADC with channel A B C D in this order in columns
 - INL curve of channel A B C D in this order in columns
 - FTT parameters (SFDR, THD, SNR, SINAD, EBOB) of each Channel A B C D in line
- Harmonic level of each channel A B C D in columns
- FFT Module and FFT frequency of each Channel A B C D in columns

File: DK BDC QUAD10bit DATA.xls

Figure 4-60. Example of Excel File

Column A: corresponds to channel A Column B: corresponds to channel B Column C: corresponds to channel C Column D: corresponds to channel D

■ Bichier Edition Affichage Insertion Format, Qutils Données Feighte 2	Microsoft Excel - DK BDC Qua	d 10bit DATA.xls						
D prime prim prim prim<	Fichier Edition Affichage Insertio	on Forma <u>t O</u> utils <u>D</u> onn	ées Fe <u>n</u> être <u>?</u>				_	. 8 ×
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A B C D E F G H I J K L 1 0076 505 520 -	A1 🗾 = 0							
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Warning: before using, your PC needs to be configured. The decimal separator must be a dot "." instead of comma "," like in French.

Use a control Regional Setting to check if decimal separator is configured with a dot ".".

4.5.10 Regional and Language Options

Use a control Regional Setting to check if decimal separator is configured with a dot ".".

Figure 4-61. Regional and Language Options

📌 Regional an	d Language Options			
Formats Location Keyboards and Languages Administrative To change the way your computer displays numbers, currencies, dates, and time, select an entry from the format list. Item (Computer displays numbers)				
Current form	nat:			
French (Fran	nce) 🔹			
Examples of	how data is displayed using this format:			
Number:	123 456 789,00			
Currency:	123 456 789,00 €			
Time:	15:08:25			
Short date:	06/08/2010			
Long date:	vendredi 6 août 2010			
	C <u>u</u> stomize this format			
For addition	al formats, keyboards, and tools, go to the Microsoft website.			
	OK Cancel Apply			

Selection: Customize this format.

Figure 4-62. Customize Regional Option

Sheet Numbers

The decimal separator must be configured with a dot "."

Numbers Cu	irrency Time Date	/
Example		/
Positive:	123 456 789,00	Negative: -123 456 789,00
Decim	al symbols	
<u>N</u> o. of	digits after decimal:	2
D <u>i</u> git g	rouping symbol:	•
Digit g	rouping:	123 456 789 💌
N <u>e</u> gat	ive sign symbol:	- •
Nega <u>t</u>	ive number format:	-1,1 🔹
Dis <u>p</u> la	y leading zeros:	0,7 🔹
<u>L</u> ist se	parator:	; •
<u>M</u> easu	rement system:	Metric 🔹
<u>S</u> tanda	ard digits:	0123456789 👻
<u>U</u> se na	tive digits:	Never 👻
Click Reset	to restore the system defa	ult settings for <u>R</u> eset

Software Tools

1067BX-BDC-12/11

e2v semiconductors SAS 2011

Section 5 FPGA CODE

The FPGA code has been designed to be used with ML605 Xilinx Virtex 6 evaluation board.



Figure 5-1. ML605 Xilinx® VIRTEX® 6 Evaluation Board

Warning: Please configure your ML605 evaluation board with correct Switch configuration.

5.1	Software Configuration	XILINX configuration: VIRTEX-6 FPGA ML605 Evaluation Kit Xilinx ISE Design Suite version 12 or upper with IMPACT software
5.2	FPGA Binary File	A binary file is provided with the Demo Kit
		CDROM\FPGA Bin10_demo_v1.1.bit
		 Configuration PLL at 2 GHz with data rate into FPGA at 1Gbps
		Note: because of limitation of ML605 evaluation board (LVDS max 1Gb/s in speed grade -1)
		The capture of Quad 10-bit data in requires Fclock lower than 2 GHz.
		Two Binaries are provided for iMPACT software
		CDROM\FPGA Bin\prog_q10.ipf (configuration of iMPACT)
		CDROM\FPGA Bin\prog_DKQ10_V1.1.mcs (PROM file)

5.3 FPGA Programming

Connect the USB Mini cable on USB JTAG connector J22 Change the Configuration Mode Switch and System ACE Address

Figure 5-2. Configuration Mode Switch of ML 605 Board



Launch the iMPACT of ISE suite and load the CDROM\FPGA bin\bin\prog_q10.ipf

Figure 5-3. Loading of DKQUAD10bit.ipf file

Image: Second secon
MPACT Processes ↔ □ ♂ ×
MPACT Flows ↔ □ Ø × Boundary Scan SlaveSerial Direct SPI TDI SystemACE Exxes Create PROM File (PROM File Formatter) xccace xccace xcEvkx240t bypass qualit_demoV1.1.bit MPACT Processes ↔ □ Ø × Available Operations are: ♥ Program wrify
Boundary Scan SlaveSerial SloveSerial SystemACE Create PROM File (PROM File Formatter) MPACT Processes ↔ □ 중 × Available Operations are: Yourfy
MPACT Processes ↔ □ ♂ × Available Operations are:
Available Operations are: Program Wrify
Erzse Blank Check Readback Get Device Checksum Read Device Status
W PROM File Formatter: BPLFlash Single FPGA W Boundary Scan
Warnings + C & S
A WARMANU: INFAULTS23 - Can not find Cable, check Cable Setup :
Configuration Platform Cable USB 6 MHz usb-hs

Note: ensure that program into PROM is correctly programmed.

Don't forget to program the CDROM\FPGA Bin\progQ10_V1.1.mcs file into PROM.

 Device 1 (ACECF xccace) Device 2 (FPGA xc6vlx240t) Device 2 (Attached FLASH, XCF12 	Property Name	Value	
Device 2 (Attached FLASH, XCF12	1 Unit for an	Value	
	veriry		
	General CPLD And PROM Properties		
	Erase Before Programming		
	FPGA Device Specific Programming Proper	ties	
	Assert Cable INIT during programming		
	After programming Flash	automatically load FPGA with Flash co	

Figure 5-4. Programming the File PROM\DKQUAD10bit.mcs



🐉 ISE iMPACT - [Boundary Scan]		
🛞 Eile Edit View Operations Output De	ebug <u>W</u> indow <u>H</u> elp	_ 8 ×
- 🗋 🖻 🗟 🕺 🛅 🗙 🖽 🕸 🗱 🖬	# # @ Ē □ ♪ N?	
MPACT Flows ↔ □ & ×	Right click device to select operations	
Boundary Scan SlaveSerial SlaveSerial SystemACE Create PROM File (PROM File Formatter)	TDI Emar xccace xc6vb.240t bypass gaad1_deme_V1.1.bit	
Available Operations are: Program Verfy Erase Blank Check Readback Get Device Checksum Read Device Status	Program Succeeded	
	PROM File Formatter: BPI Flash Single FPGA 🛛 Boundary Scan	
Warnings		+□♂×
<u>f WARNING</u> :iMPACT:923 - Can not :	find cable, check cable setup !	~
1		×
Console Errors Warnings	Configuration Platform Ca	ble USB 6 MHz usb-hs

5.4 VHDL CODE A documentation of VHDL architecture is provided with the Demo Kit. See CDROM\Documentation\FPGA Code\ DK_QUAD10_bits_FPGA_Design_Document_v1.pdf

Figure 5-6. VHDL Top level simplified block diagram



Section 6

Demo kit Hardware Configuration

The Demo Kit could be hardware configured by changing manually some capacitor or resistance.

This chapter describes all user settable hardware configurations.

6.1 Channel D The Channel D could be used in DC configuration mode by replacing C126 and C127 by a 0Ω resistor.





6.2 Clock Selection The ADC clock is generated by a PLL, but an external clock can be used (for frequency different than PLL). The selection between the two clocks is done manually with a resistor.

Remove R15 and R37 resistors and solder R36 and R50 with a 0Ω .

Note: The VHDL code supplied permits operation at 2 GHz. A re-compilation with different timing constraints will be required for other frequencies.





Figure 6-3. Implantation of R15, R37, R36 and R50 Resistors



6.3 SPI Signal The SPI signal is controlled by the FX2 microcontroller, but it could also be controlled by FPGA.

The selection between the two clocks is done manually with a resistor.

Note: e2v doesn't provide the SPI controller FPGA code.

Remove R93, R95, R97, R99 and R101 resistors and solder R94, R96, R98, R100 and R102 with a $0\Omega.$

Figure 6-4. SPI Schematic



Figure 6-5. Implantation of R93, R94, R95, R96, R97, R98, R99, R100, R101 and R102 resistors



6.4 SYNC Signal

The SYNC signal is controlled by the FX2 microcontroller, but it could also be controlled by the FPGA.

The selection between the two clocks is done manually with a resistor. Note: e2v doesn't provide the SYNC signal FPGA code.

Remove R105 resistor and solder R106 with a 0Ω .

Figure 6-6. SYNC Schematic



Figure 6-7. Implantation of R105 and R106 Resistors


Section 7 Layout Information



Figure 7-1. Top Side Layer 1

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EVAL-KIT QUAD ADC 10bit LAYER 1 COMPONENT SIDE





EVAL-KIT QUAD ADC 10bit LAYER 12 SOLDER SIDE Layout Information

Section 8 Mechanical Dimensions

The Demo Kit board with Quad 10-bit ADC dimension is 139 mm \times 76.5 mm \times 8 mm. It is compatible with VITA57 FMC standard.

Figure 8-1. Mechanical Dimensions



Mechanical Dimensions

Section 9

Ordering Information

Table 9-1.Ordering Information

Part Number	Temperature	Comments
EV10AQ190TPY-DK	Ambient	ROHS compliant

9-1

Ordering Information

1067BX-BDC-12/11

e2v

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