Application Note

Application Note on Offset, Gain, Phase Calibration Sequence ADC Quad 10-bit 1.25G

1. Introduction

This application note gives you some details on parameter setting sequence to interlace the four ADCs. In fact, optimum performances are obtained when calibration is done correctly. For this, all the ADCs must have the same characteristics; the same offset, the same gain and the same phase.

This application note gives you the calibration process.

2. Offset Gain Phase Adjustment

In order to calibrate the ADC three adjustment features are available.

The Offset, Gain Phase of each ADC are controlled through the Digital Interface (SPI)

The digital interface is a standard SPI (1.8V CMOS) with:

Four **DACs for the gain controls** are addressed thru the SPI:

Four **DACs for the offset controls** are addressed thru the SPI:

- Offset DACs act close to the cross point switch;
- Gain DACs act on the biasing of the reference ladders of each ADC core.

These DACs have a resolution of 10-bit and will allow the control via the SPI of the offset and gain

- Gain adjustment on 1024 steps, ± 10% range; (1 step ~ 0.02% adjust)
- Offset adjustment on 1024 steps, ±40 LSBrange (1 step ~ 0.08LSB offset adjust).

Four **DACs for fine phase control** are addressed through the SPI, they have an 10-bit resolution

- Phase adjustment on 1024 steps, ±15 ps (1 step ~ 29fs adjust)

The e2v evaluation board contains Graphical User Interface (GUI), which allows device adjustment through the SPI interface. The SPI adjustments are accessed using the internal register within the Offset Gain Phase sheet of GUI.

We can observe the influence of each parameter (Offset, Gain and Phase) on the FFT spectrum.

3. Offset Calibration

This calibration is based on the middle code. In fact, if there is no signal on analogue input, the signal will be on the code ($2^n/2$)-1 (where n is the resolution of the ADC).

- Connect the clock input but disconnect the analogue input (disconnect the analogue input or switch off the generator or choose an entrance channel (Ain, Bin, Cin or Din) which is not used)
- acquire the samples
- make an average of the samples
- adjust the mean value of the four ADCs on the middle code

For example, the offset of the red channel must be increased and the offset of the blue channel decreased.

Figure 3-1.

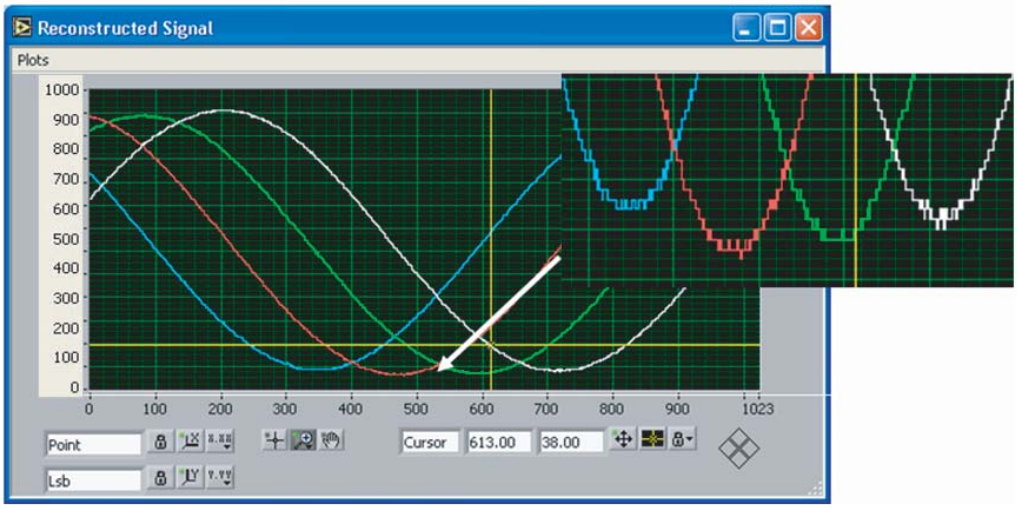
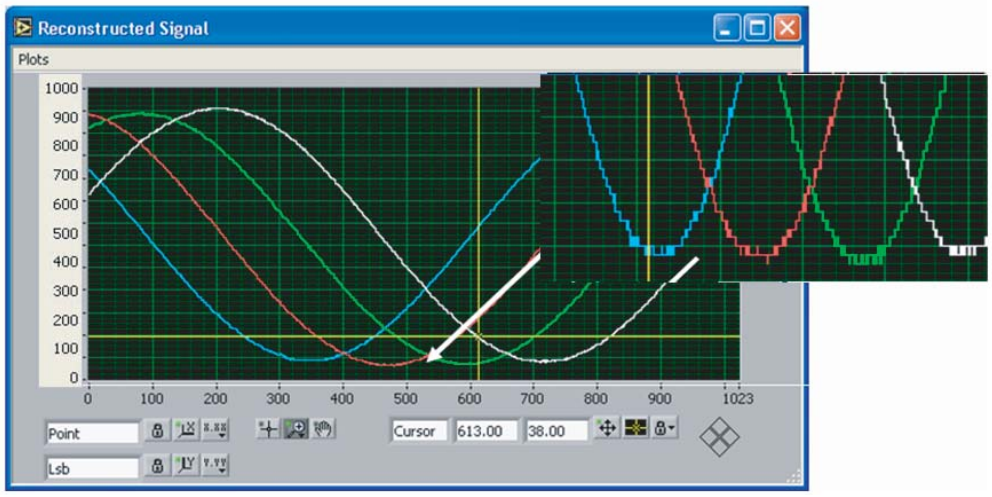


Figure 3-2.



Another way to preform this increase is to input a sine wave and export the sampled data to Excel where the averaging can be done.

4. Gain Calibration

For this calibration, reconnect the signal on analogue input. The gain calibration is based on the level of the SFSR. So some FFT are required.

The alignment is done compared with one channel chosen at the beginning.

- Connect the analogue and clock inputs
- Acquire the samples
- Make an FFT
- Adjust the SFSR of the four ADCs on the SFSR of the channel chosen

Here, for example, the gain of the green and blue channel must be increased and the red channel reduced.

Figure 4-1.

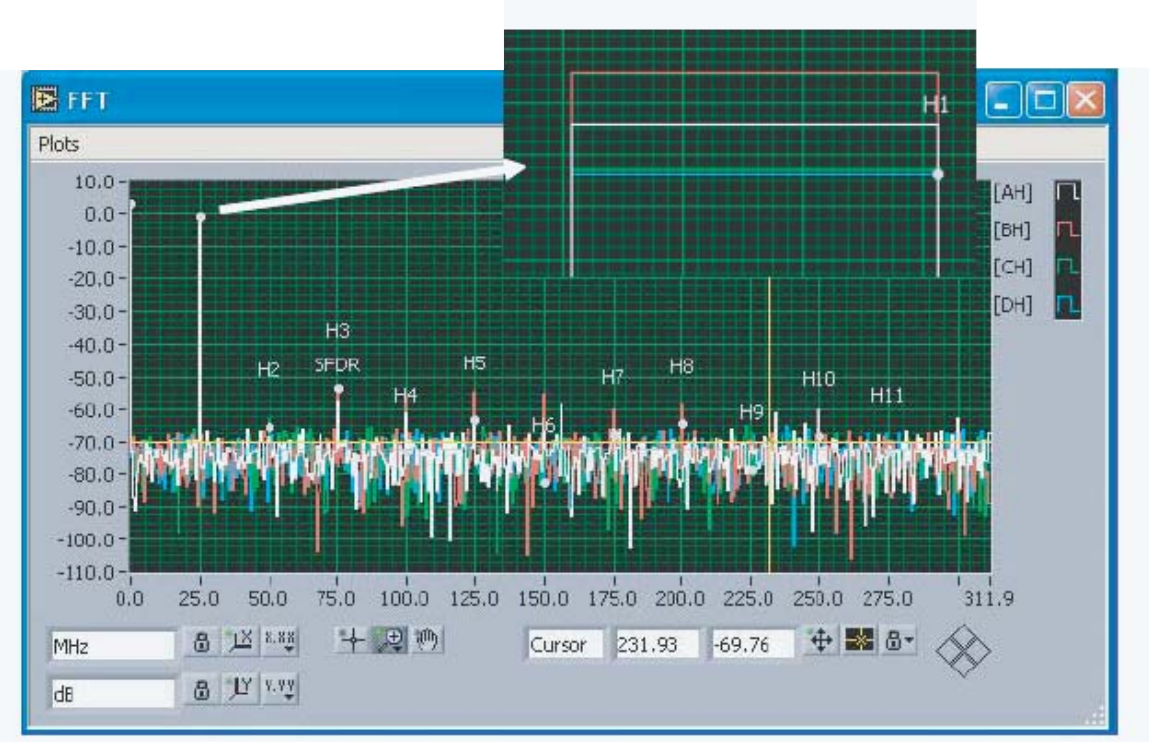
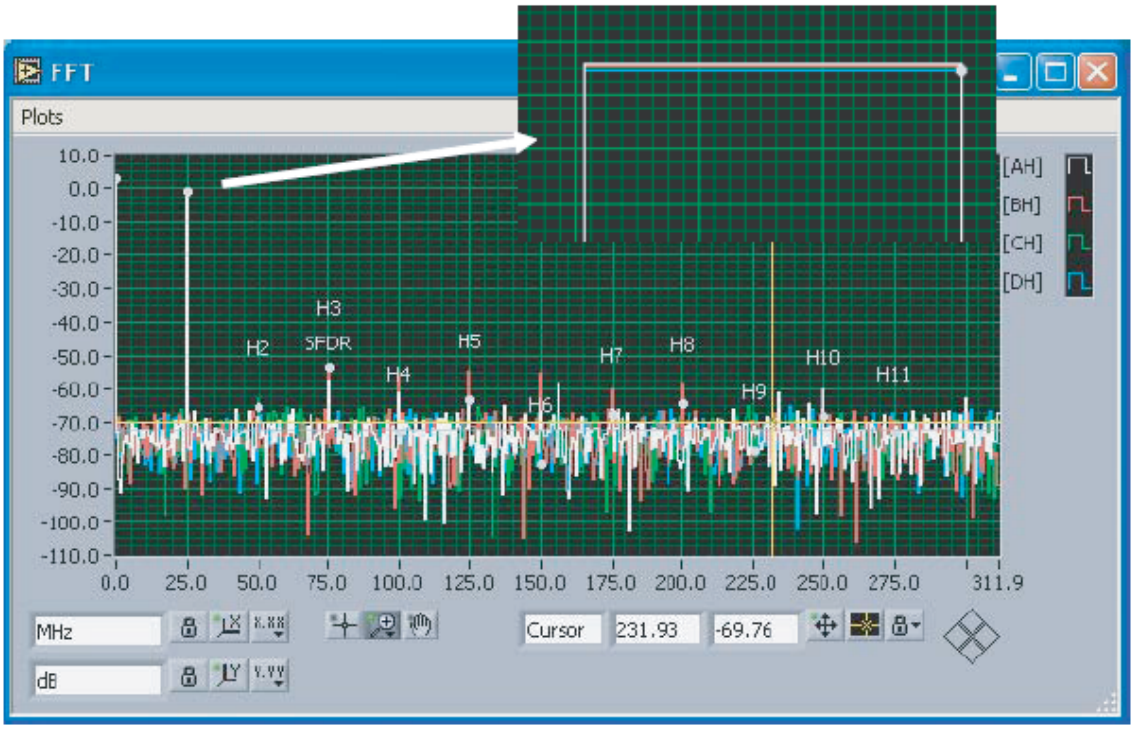


Figure 4-2.



When the result is acceptable, you can go to the last calibration.

5. Phase Calibration

There are a number of different method of calibrating the phase of an EV10AQ190A.

1. Using the component in 1 channel mode and arranging the clock to sample the input at the same point.
2. Using 4 channel mode and simultaneous sampling.
3. Using an iterative search.

5.1 Using 1 Channel Mode

The method illustrated below uses the GUI provided with the Evaluation board EV10AQ190A-EB and not the system delivered with the Demo board, EV10AQ190A-DK.

We used the fact that Fin = 2 × Fc but without coherency. This means that there is not an integer number cycles within a given sample window however the clock and signal were locked.

The alignment is done compared with one channel chosen at the beginning.

We used the fact that Fin = 2 × Fc to calibrate the phase because, in this case, all the reconstructed signals are in line. Each clock will make a sample at the same time on the sine curve. So it is easier to calibrate the phase. In the case when Fin = Fc for example, each clock will make two samples on the sine curve, consequently it is impossible to calibrate the four ADCs.

For example, you make the calibration with Fin=1GHz and Fc=500Msps. But, in order to have a competitive calibration, it is better to make your calibration at the clock frequency where you want to use the converter afterwards.

- Connect the analogue and clock inputs
- Disconnect filters
- acquire the samples
- make an average of the samples

adjust the mean value of the four ADCs on the value of the channel chosen

Figure 5-1.

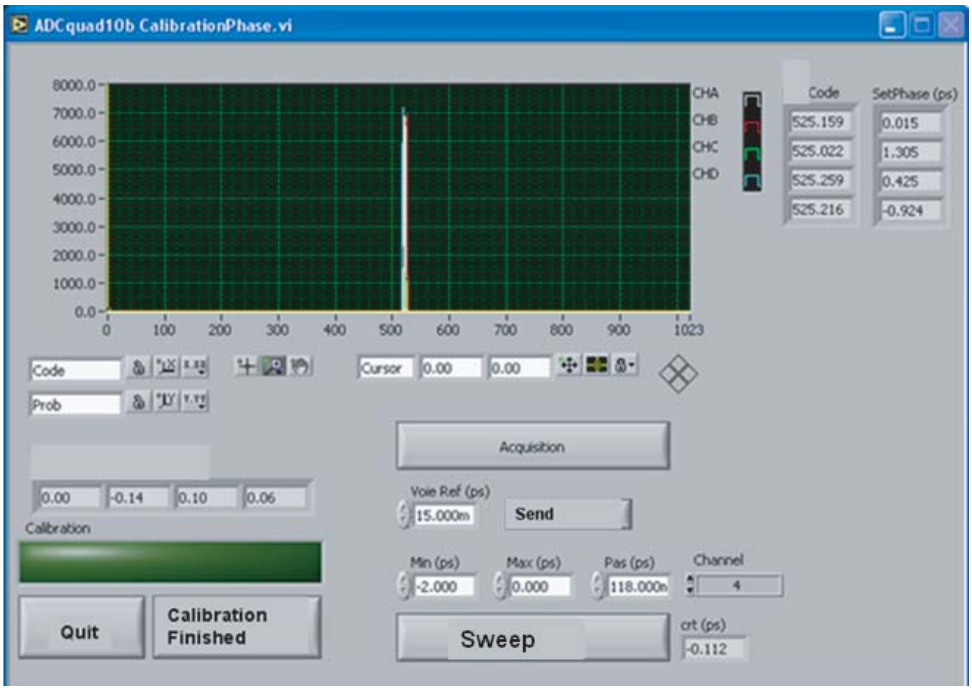
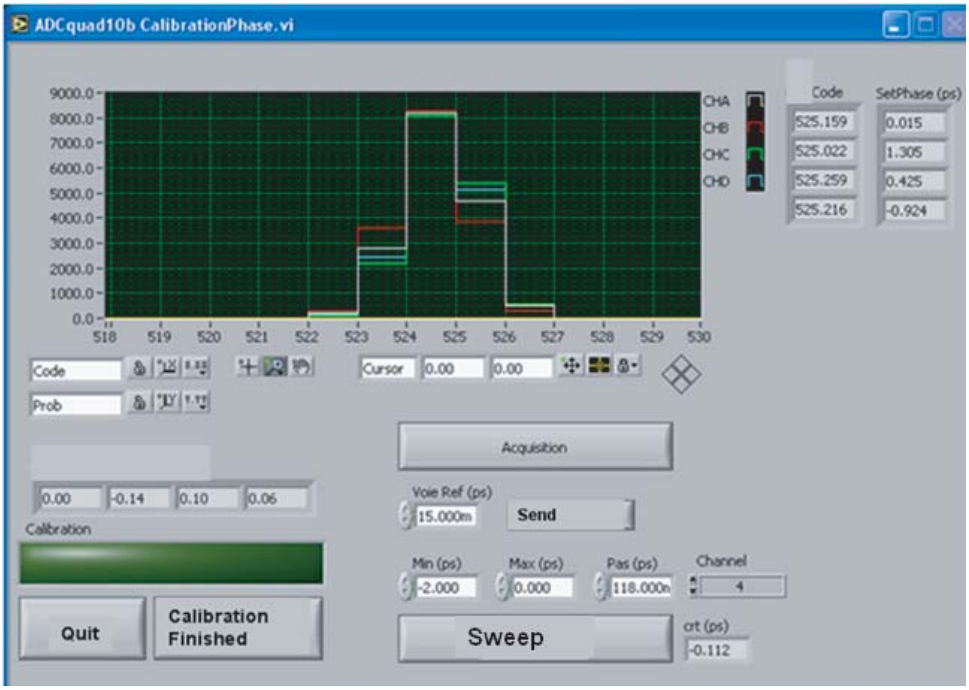


Figure 5-2.



When the result is acceptable, you can interleave all the ADCs.

5.2 Using the Simultaneous Sampling Mode.

In this mode a signal is input onto one input channel and using the simultaneous sampling mode this is propagated to all ADC cores. The principle in this case is that each channel samples the signal at the same point in time and any differences in aperture delay are detected and calibrated.

The input signal frequency should be locked to the clock frequency and be at Fclk/2. There should be an adjustable delay between the two signals so that the sample point is taken at the point of largest slew.

When using the demo kit, it is not possible to obtain a histogram output as in the case of the evaluation board. The data should be output to Excel and then manipulated using a macro.

Once a histogram is obtained, the sample point of each core can be adjusted to minimize the phase difference.

5.3 Using an Iterative Search

In this case the component is placed in 1 channel mode with the gain and offset already calibrated.

The phase of one channel is fixed and each other channel is varied in turn until the interleaving spurs are reduced to a minimum, a software routine can be written to improve search timescales. The input frequency should be close to the highest frequency expected by the application.

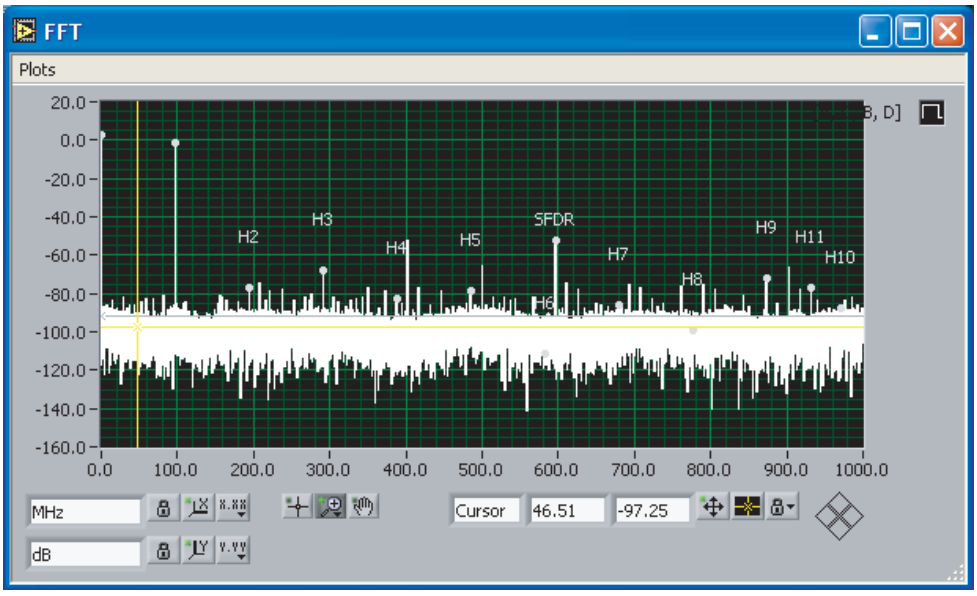
In some cases where the convergence is difficult to obtain – the initial fixed channel should be adjusted.

5.4 Effect of Phase Calibration

This phase calibration has a significant impact on the SFDR, which is given by an interleaving spur, not a harmonic.

Before the phase calibration:

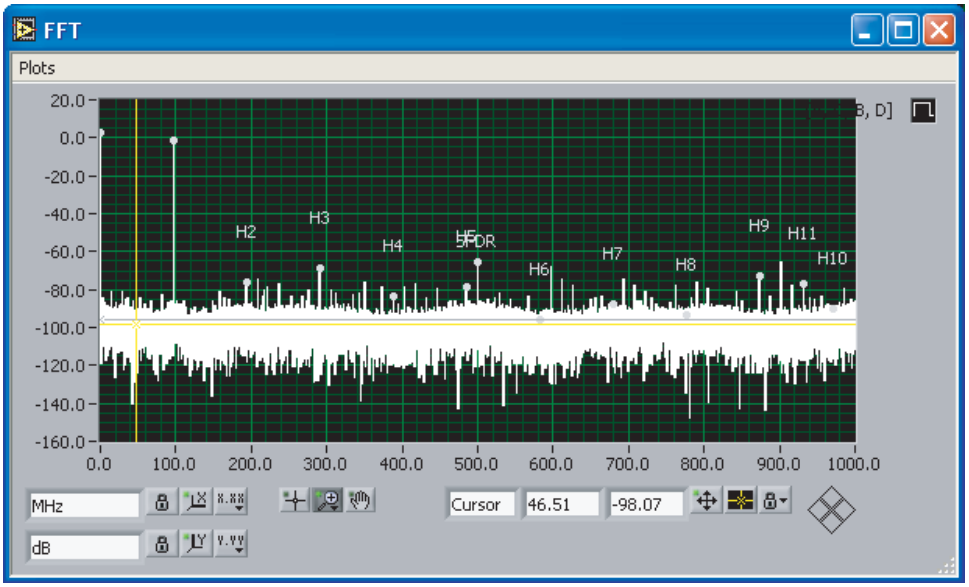
Figure 5-3.



SFDR = –50 dB

After the phase calibration:

Figure 5-4.



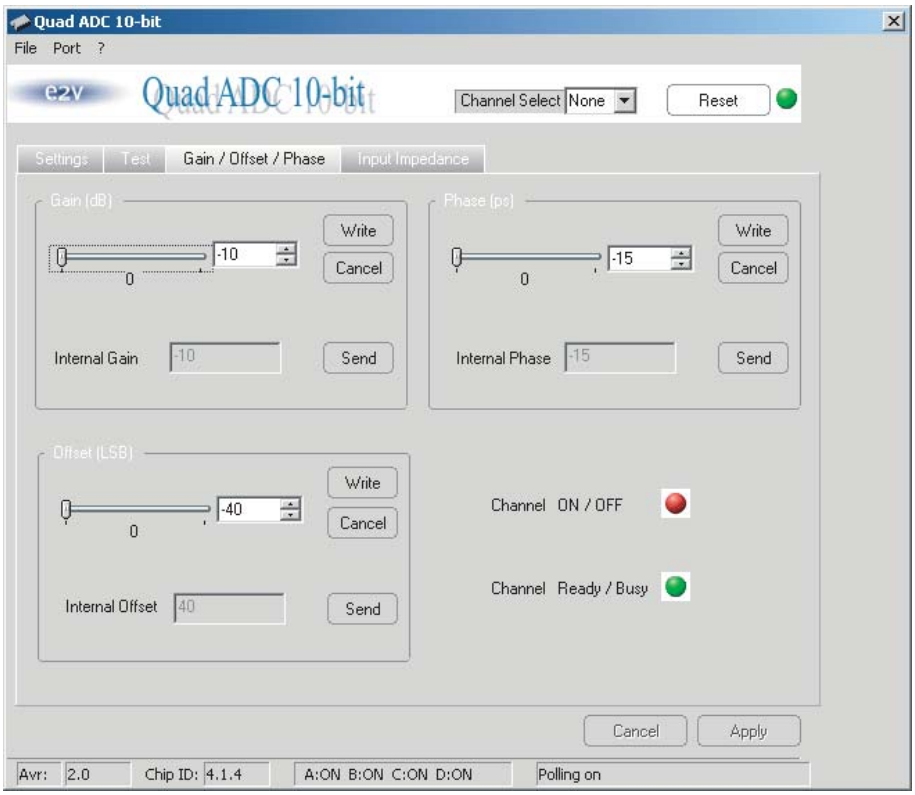
SFDR = –65 dB

The calibration phase must be done correctly.

Gain/Offset/Phase

This is a reminder on how to calibrate Gain/Offset/Phase with the GUI:

Figure 5-5.



In this window, you can adjust the gain, offset and phase of the channel selected via the "channel select" button on the top right of the user interface.

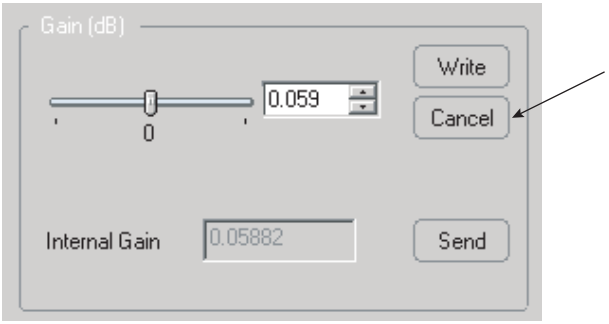
A LED shows if the channel is ON (active – green LED) or OFF (not active – red LED) and if the same channel is ready (ready to receive gain, offset or phase orders – green LED) or busy (not ready to receive new calibration orders – red LED).

Once a channel has been selected, you can adjust the gain/offset/phase of this channel:

- you first need to enter the desired value for the gain/offset/phase thanks to the cursor;
- if you need to retrieve the old value of the gain/offset/phase click CANCEL;
- then you should WRITE this value to the internal registers by clicking on the WRITE button,
- if several adjustments are needed (gain AND offset AND phase), then select each value and then click on the respective WRITE buttons;
- once all adjustments are made via the WRITE buttons, then you can SEND the orders to the ADC SPI via the SEND button;
- the calibration is successful if the internal gain/offset/phase boxes display the entered values.

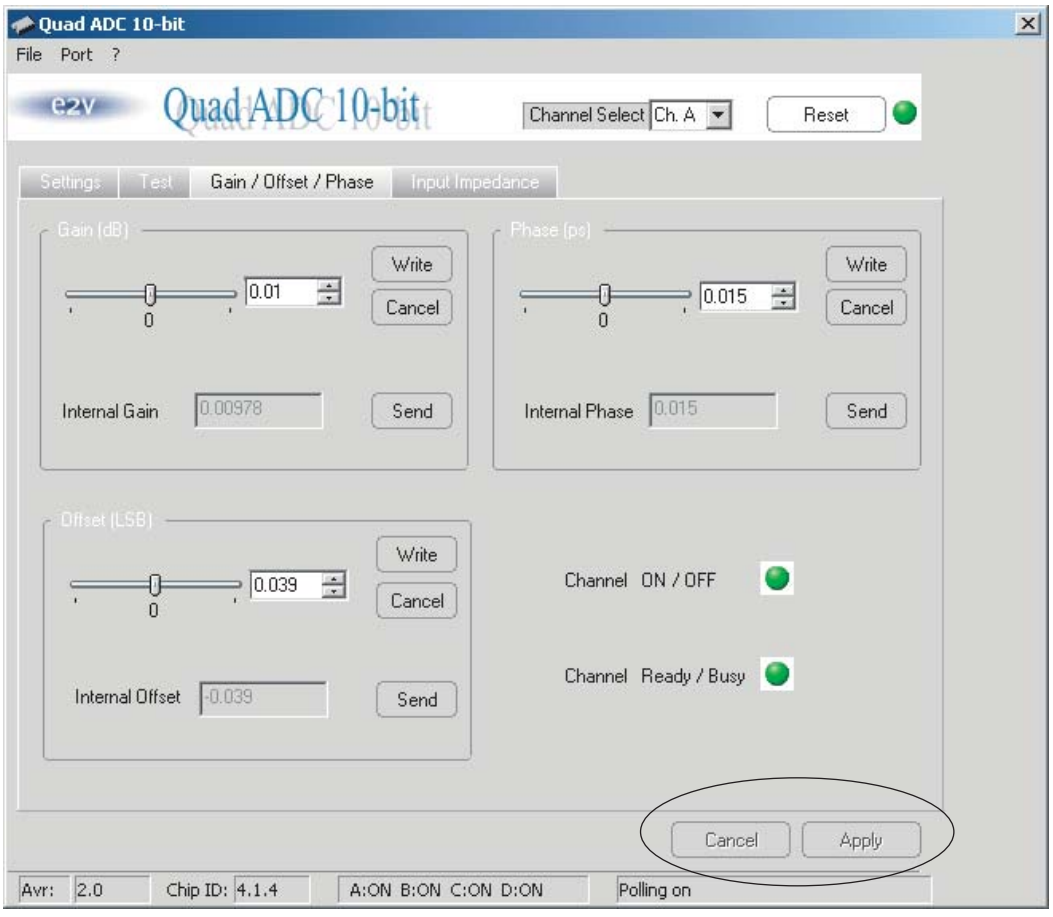
If a new value for the gain/offset/phase has been entered by mistake, it is possible to retrieve the initial value by pushing the CANCEL button.

Figure 5-6.



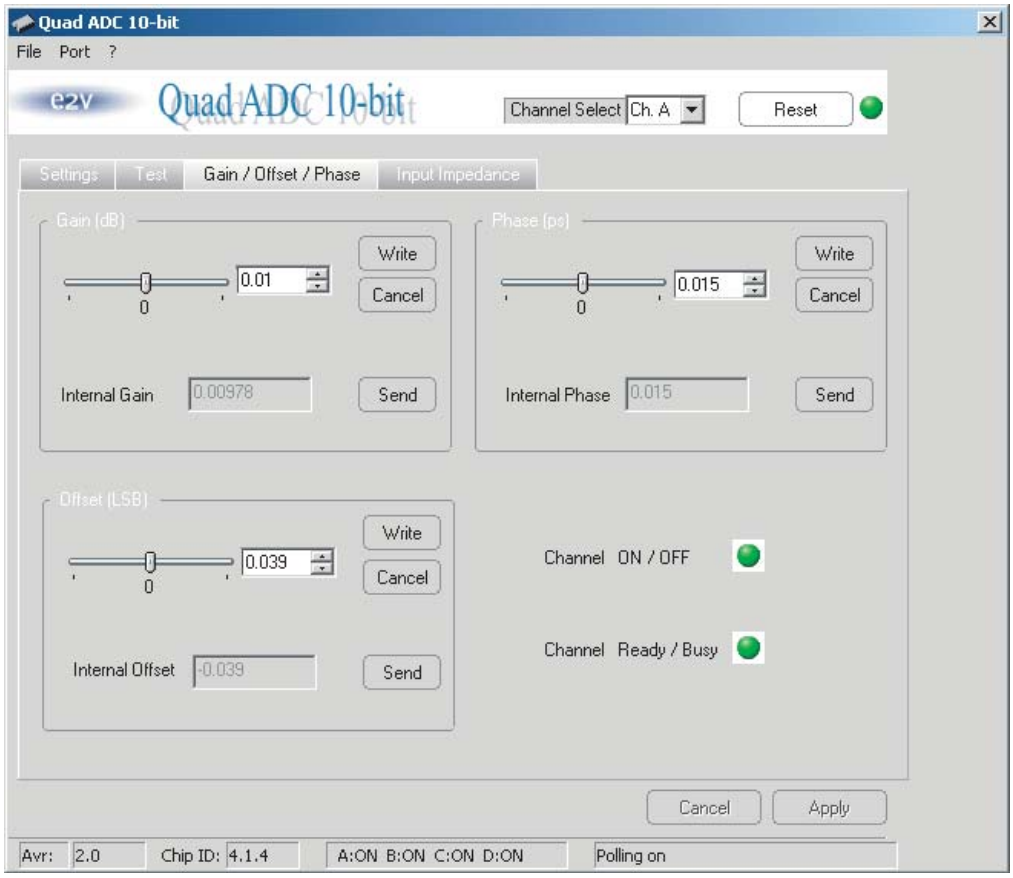
The general APPLY and CANCEL buttons are not active in this window (as soon as the SEND button is applied, the gain/offset/phase adjustments are made active).

Figure 5-7.



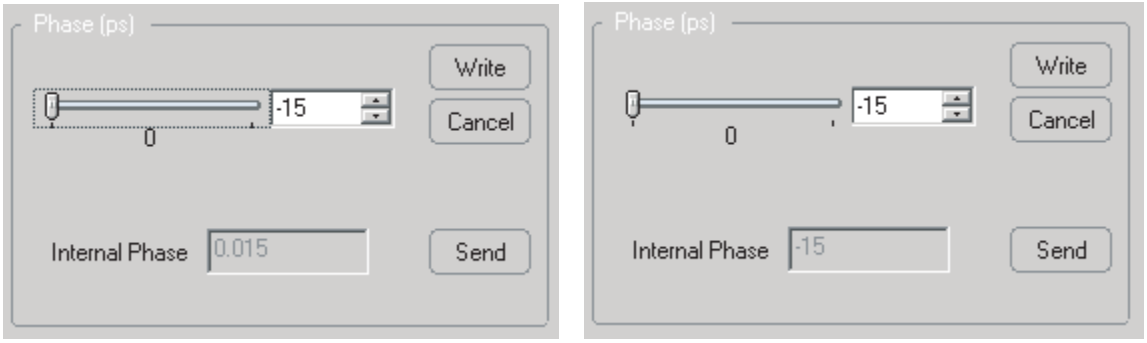
In the following example, channel A is selected. Values for the gain, the offset and the phase have been entered via the WRITE and then the SEND buttons, which explains why the Internal values are equal to the internal setting values.

Figure 5-8.



In the following example, you can see that the internal phase register is set to 0.015 and that the user wants the phase to be set to –15 ps. In the second picture, the WRITE and SEND buttons have been pushed and the internal register shows the new entered value for the phase.

Figure 5-9.



The iterative technique for calibrating the phase was described previously. Based on a reference phase for one channel the phase of the adjacent channels is adjusted so that the interleaving spurs decrease.

This is repeated over all channels until the interleaving spurs (at Fclk /4 in 1 channel mode for softset variations and at Nyquist – Input frequency for gain and phase variations) are reduced to their minimum level.

Once the calibration is done, you can save it to re-use it later.

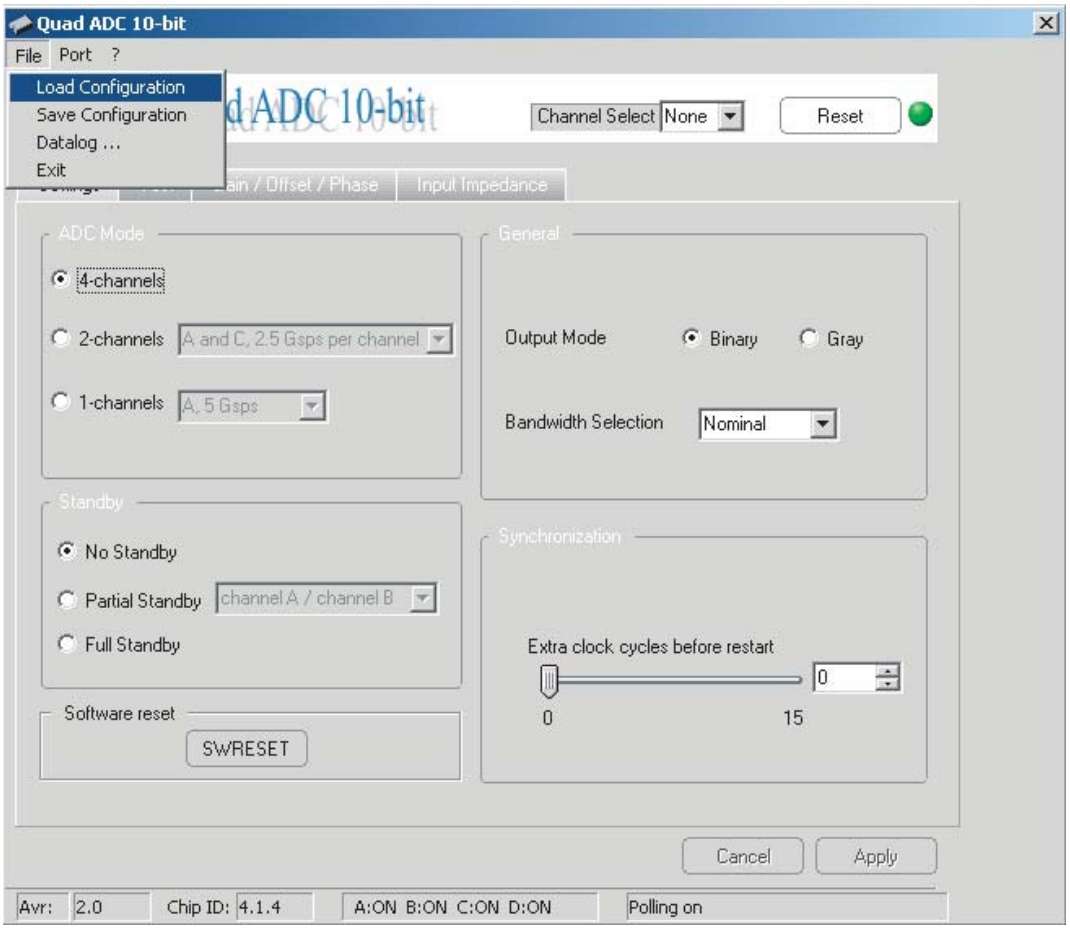
Load and Save configuration

The "File" menu shows possibility to load or save a configuration of the EV10AQ190 or to create a data-log file.

It is possible to save the configuration of EV10AQ190 into a .txt file:

Select the "File" menu and click to "Save Configuration".

Figure 5-10.



Temperature stability

It is better if the calibration is performed at the junction temperature which the part will used. In this case, tests have shown that the calibration values remain valid, for the four cores in a single component, if the temperature varies by ±20°C

6. Conclusion

There are some important points to respect:

- The calibration must be in this order: Offset, Gain, Phase
- Offset calibration: disconnect the analogue input
- Phase calibration: make your calibration at the clock frequency where you want to use the converter afterwards.

If these previous points are respected, the calibration will be very good. So, the interlace will be possible and you will gain on performances, namely on the SFDR.

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