AT84AS001-EB Evaluation Board

User Guide

e2v

Table of Contents

e2v

Section 1
Introduction

1.1 Scope

The AT84AS001 Evaluation Board (EB) is designed to facilitate the evaluation and characterization of the AT84AS001 12-bit 500 Msps ADC in AC coupled mode.

The AT84AS001 Evaluation Board (EB) includes:

- The 12-bit 500 Msps ADC Evaluation Board including AT84AS001 ADC and Atmel AVR ATMEGA128 soldered
- A cable for connection to the RS-232 port
- Software tools necessary to use the 3-wire serial digital interface

The user guide uses the AT84AS001 Evaluation Kit as an evaluation and demonstration platform and provides guidelines for its proper use.

1.2 Description

The AT84AS001-EB is very straightforward as it implements AT84AS001 12-bit 500 Msps ADC device, Atmel ATMEGA128 AVR, SMA connectors for the sampling clock, analog inputs and reset inputs accesses and 2.54 mm pitch connectors compatible with high-speed acquisition system probes.

Thanks to its user-friendly interface, the AT84AS001-EB kit enables to test all the functions of the AT84AS001 12-bit 500 Msps ADC using the 3-wire serial interface connected to a PC.

- Gain and offset control
- Standby mode

To achieve optimal performance, the AT84AS001-EB Evaluation board was designed in a six metal-layer board using FR4 HTG epoxy dielectric material (200 µm, ISOLA IS410 featuring a resin content of 45%). The board implements the following devices:

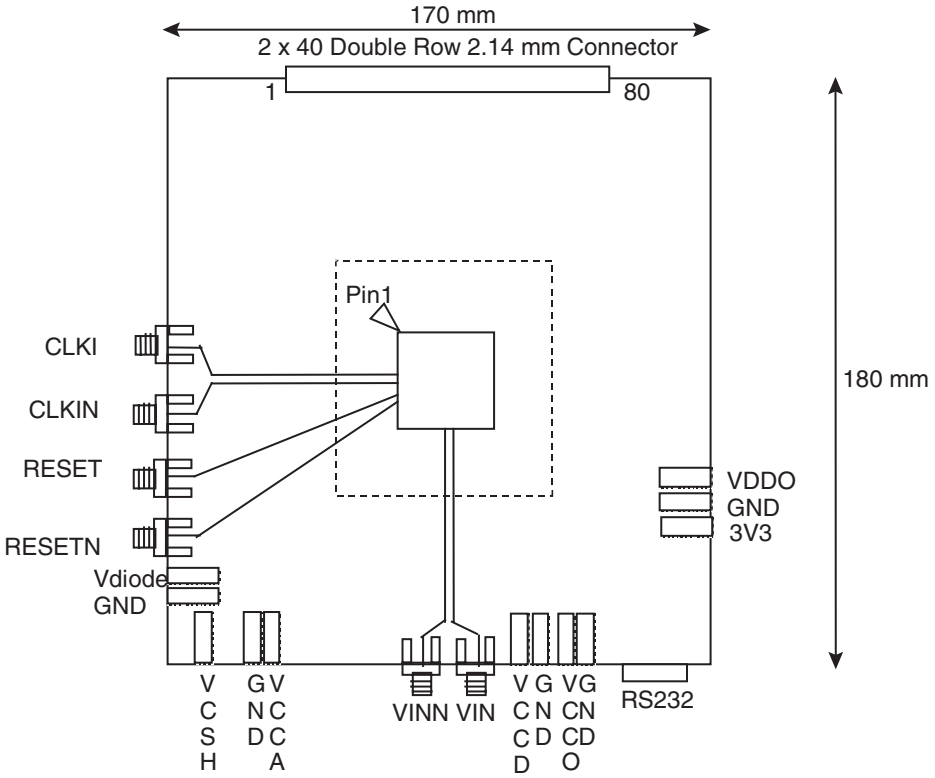
- The 12-bit 500 Msps ADC Evaluation Board with the AT84AS001 ADC soldered
- SMA connectors for CLK, CLKN, VIN, VINN, RESET and RESETN signals
- 2.54 mm pitch connectors for the digital outputs, compatible with high-speed acquisition system probes
- Banana jacks for the power supply accesses and the die junction temperature monitoring functions (2 mm)

- One green LED used to check when the 3-wire serial interface is active
- One switch to select the 3-wire serial interface
- An RS-232 connector for PC interface

The board dimensions are 170 mm × 180 mm.

The board comes fully assembled and tested, with the AT84AS001 installed.

Figure 1-1. AT84AS001 Evaluation Board Simplified Schematic



As shown in Figure 1-1, different power supplies are required:

- V_{CCA} = 5V analog positive power supply
- V_{CCD} = 3.3V analog positive power supply
- V_{CCO} = 2.5V digital output
- V_{DDO} = 2.5V ADC 3-wire serial interface power supply
- 3.3V digital interface primary power supply for the microcontroller

e2v

Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full-speed operation of the AT84AS001 12-bit 500 Msps ADC, a multilayer board structure was retained for the evaluation board. Six copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in FR4 HTG epoxy dielectric material (ISOLA IS410).

The following table gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 mm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces
FR4 HTG / dielectric layer	Layer thickness = 200 mm
Layer 2 Copper layer	Copper thickness = 18 µm Upper ground plane = reference plane
FR4 HTG / dielectric layer	Layer thickness = 349 µm
Layer 3 Copper layer	Copper thickness = 18 µm Power planes = V_{CCA} and V_{CCD} and 3V3
FR4 HTG / dielectric layer	Layer thickness = 349 µm
Layer 4 Copper layer	Copper thickness = 18 µm Power planes = V_{DDO}, V_{CCO}
FR4 HTG / dielectric layer	Layer thickness = 349 µm
Layer 5 Copper layer	Copper thickness = 18 µm Power planes = reference plane (identical to Layer 3)
FR4 HTG / dielectric layer	Layer thickness = 200 µm
Layer 6 Copper layer	Copper thickness = 40 µm (with NiAu finish) DC signals traces

Note: The board is 1.6 mm thick.

The clock, analog input, reset, digital data output signals and ADC functions occupy the top metal layer. The ground planes occupy layers 2 and 5. Layers 3 and 4 are dedicated to the power supplies.

2.2 Analog Inputs/Clock Input

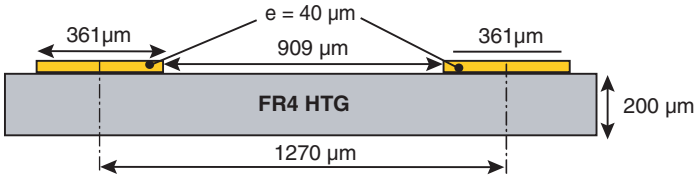
The differential clock and analog inputs are provided by SMA connectors (reference: VITELEC 142-0701-8511).

Both pairs are AC coupled using 10 nF capacitors.

Special care was taken for the routing of the analog and clock input signals for optimum performance in the high-frequency domain:

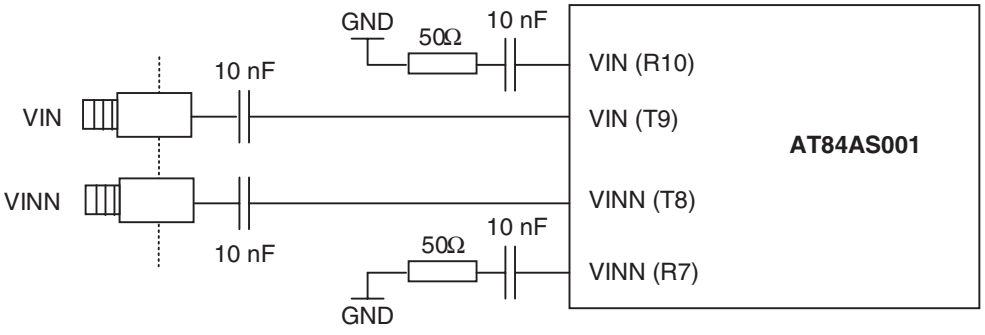
- 50Ω lines matched to ± 0.1 mm (in length) between VIN and VINN or CLKI and CLKIN
- 1.27 mm pitch between the differential traces
- 361 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the VIN and VINN or CLKI and CLKIN ball footprints

Figure 2-1. Board Layout for the Differential Analog and Clock Inputs



Note: The analog inputs are reverse terminated with 10 nF in series with 50Ω to ground very close to the device (same line length used for both reverse termination).

Figure 2-2. Differential Analog Inputs Implementation

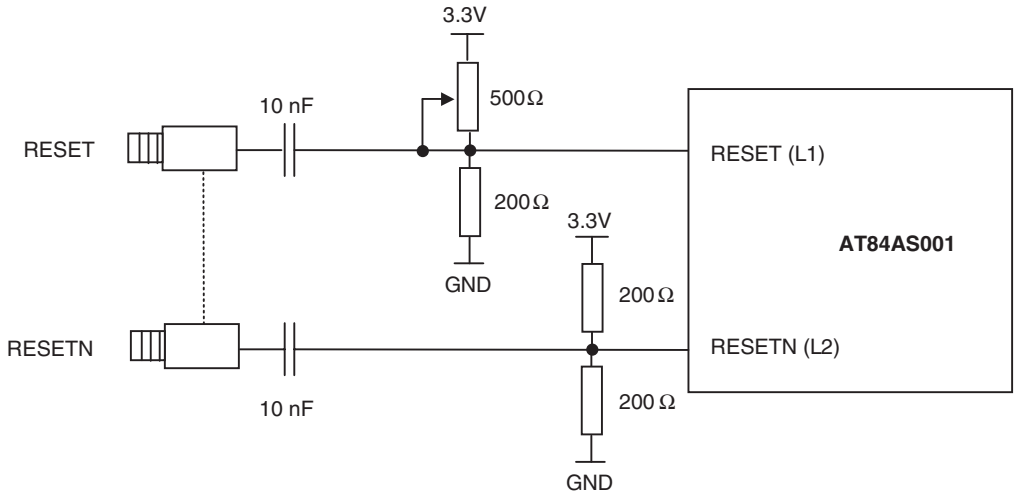


2.3 Reset Input

The differential reset inputs are provided by SMA connectors (reference: VITELEC 142-0701-8511).

The signals are AC coupled using 10 nF capacitors and pulled up and down via 200Ω resistors. A variable resistor of 500Ω is implemented on RESET: by adjusting this resistor value one can activate and deactivate easily the reset signal.

Figure 2-3. Reset Inputs Implementation



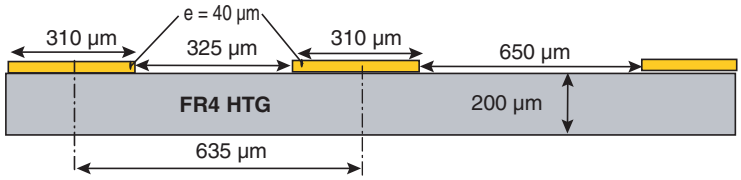
Note: The reset is active low.

2.4 Digital Output

The digital output lines were designed with the following recommendations:

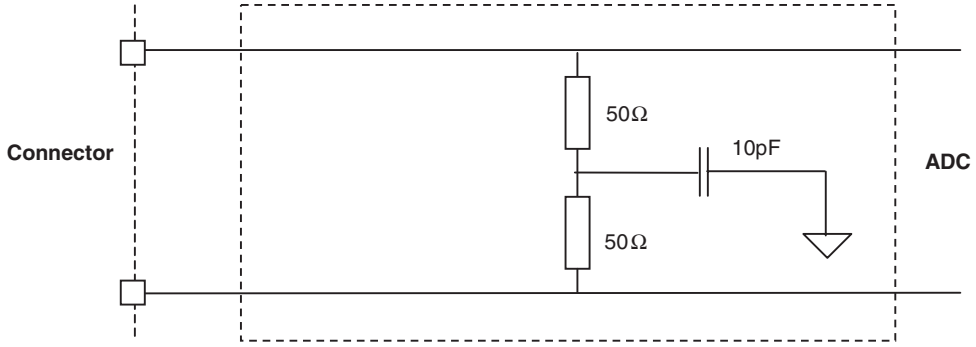
- 50Ω lines matched to ±0.1 mm (in length) between signal of the same differential pair:
- 80 mm max line length
- ±1 mm line length difference between signals of two differential pairs
- 635 µm pitch between the differential traces
- 650 µm between two differential pairs
- 310 µm line width
- 40 µm thickness

Figure 2-4. Board Layout for the Differential Digital Outputs



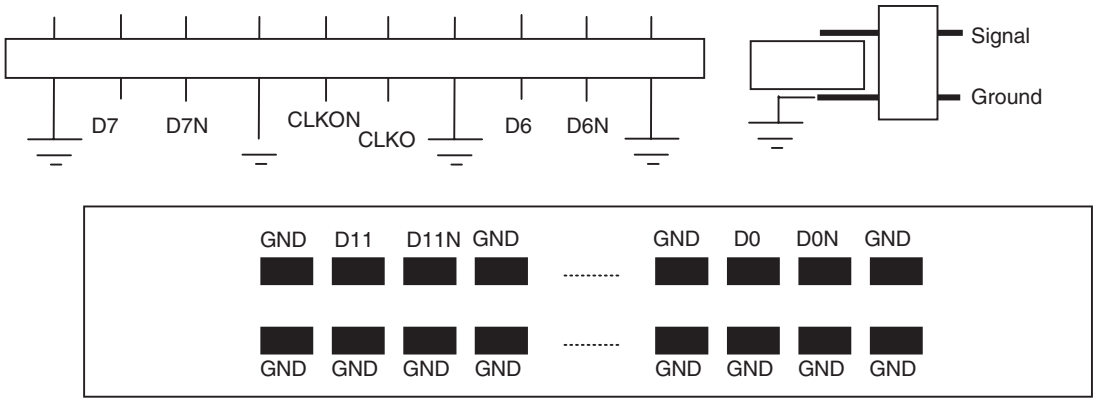
Note: The digital outputs are compatible with LVDS standard. They are on-board 100Ω differentially terminated as described in Figure 2-5.

Figure 2-5. Differential Digital Outputs Implementation



Double row 2.54 mm pitch connectors are used for the digital output data. The upper row is connected to the signal while the lower row is connected to ground, as illustrated in Figure 2-6.

Figure 2-6. Differential Digital Outputs 2.54 mm Pitch Connector



Note: The order of the output clock is different from the one of the data as illustrated in Figure 2-6.

2.5 Power Supplies

Layers 3 and 4 are dedicated to power supply planes (V_{CCA}, V_{CCD}, V_{CCO}, V_{DDO} and 3.3V). The supply traces are low impedance and are surrounded by two ground planes (layers 2 and 5).

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

Each power supply is decoupled as close as possible to the AT84AS001 device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

e2v

Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the AT84AS001 12-bit 500 Msps ADC.

The analog input signal and the sampling clock signal should be accessed in a differential fashion. Band pass filters should also be used to optimize the performance of the ADC both on the analog input and on the clock.

It is necessary to use a very low jitter source for the clock signal (recommended maximum jitter = 50 ps pk-pk)

Note: The analog input is AC coupled on the board.

3.2 Operating Procedure

1. Install the serial interface software as described in section 4 *Software Tools*.
2. Connect the power supplies and ground accesses through the dedicated banana jacks. V_{CCA} = 5V, V_{CCD} = 3.3V, V_{CCO} = 2.5V, 3.3V and V_{DDO} = 2.5V.
3. Connect the clock input signals. Use a very low-phase noise high frequency generator as well as a band pass filter to optimize the clock performance. The clock input level is typically 3 dBm and should not exceed 10 dBm (into 50Ω). The clock frequency can range from 1 MHz up to 500 MHz.
4. Connect the analog input signal (The board has been designed to allow only AC coupled analog inputs). Use a low-phase noise high frequency generator. The analog input full scale is 1.1V peak-to-peak around VCSH (Input common mode = 0.42 × V_{CCA}). It is recommended to use the ADC with an input signal of –1 dBFS max (to avoid saturation of the ADC).
   The analog input frequency can range from DC up to 250 MHz with less than 0.5 dB attenuation.
5. Connect the high speed acquisition system probes to the output connectors. The digital data are differentially terminated on-board (100Ω) however, they can be probed either in differential or in single-ended mode.
6. Connect the PC's RS-232 connector to the Evaluation Board's serial interface.
7. Check that the 3-wire serial interface mode is off (green LED off).
8. Switch on the ADC power supplies (recommended power up sequence: simultaneous or in the following order: V_{CCA} = 5V, V_{CCD} = 3.3V, V_{CCO} = 2.5V, 3.3V and V_{DDO} = 2.5V).
9. Turn on the RF clock generator.
10. Turn on the RF signal generator.

11. Perform a reset (RESET potentiometer) on the device.
12. Turn on the switch to activate the 3-wire serial interface (green LED on). The reset of the ADC is controlled via this potentiometer which, can be tuned to 3.3V (reset active) up to 0V (reset inactive)

The AT84AS001-EB evaluation board is now ready for operation.

3.3 Electrical Characteristics

For more information, please refer to the device datasheet (reference 5412).

Table 3-1. Recommended Conditions Of Use

Parameter	Symbol	Comments	Recommended	Unit
Analog supply voltage	V_{CCA}		5	V
Digital supply voltage	V_{CCD}		3.3	V
Output supply voltage	V_{CCO}		2.5 (see note)	V
Differential analog input voltage (Full scale)	V_{IN} -V_{INN}		1.1	Vpp
Differential clock input level with 200 fs rms jitter	Vclkn		3	dBm
Maximum operating junction temperature	T_J		110	°C

Note: V_{CCO} can be set either to 2.5V or to 3.3V but we recommend to set it to 2.5V in order to minimize the power dissipation.

Typical conditions:

- V_{CCA} = 5V; V_{CCD} = 3.3V; V_{CCO} = 2.5V
- V_{IN} - V_{INN} = 1.1 Vpp full-scale differential input; Digital outputs LVDS (100Ω)
- T_{amb} (typical) = 25°C unless otherwise specified

Table 3-2. Electrical Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Resolution				12		Bit
Power Requirements						
Power supply voltage Analog Digital Output and 3-wire serial interface		V_{CCA} V_{CCD} V_{CCO}	4.75 3.15 2.2	5 3.3 2.5	5.25 3.45 3.45	V
Power supply current Analog Digital Output and 3-wire serial interface		I_{CCA} I_{CCD} I_{CCO}		340 150 79		mA
Power supply current (full standby mode) Analog Digital Output and 3-wire serial interface		I_{CCA} I_{CCD} I_{CCO}		26 15 25		mA
Power dissipation Full power Standby		P_D		2.4 242		W mW
Analog Input						
Full-scale input voltage range (differential mode only)		V_{IN} V_{INN}	–275 –275		275 275	mV
Input common mode		V_{CSH}		2.1		V
Analog input power capacitance (die)		C_{IN}			2	pF
Input resistance		R_{IN}		2000		Ω
Clock Input						
Logic compatibility			PECL/ECL/LVDS (providing AC coupling)			
Clock Input power level (50Ω single-ended or 100Ω differential)		P_{CLK}	–4		10	dBm
Clock Input common mode voltage				$2 \times V_{CCD}/3$		V
Clock Input swing (differential mode on each clock input)		V_{CLK}, V_{CLKN}		±320		mV
Clock input swing (single-ended mode with C_{LKN} 50Ω to GND)		V_{CLK} , V_{CLKN}		±450		mV
Clock input capacitance		C_{CLK}			2	pF
Clock input resistance Differential		R_{CLK}		100		Ω
Digital Inputs (Serial Interface)						
Maximum clock frequency (sclk)			50			MHz

Table 3-2. Electrical Characteristics (Continued)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit
Logic compatibility				CMOS (V_{CCO} = 2.5V)		
Control input voltages						
Logic low		V_{IL}	–0.3	0	0.3	V
Logic high		V_{IH}	V_{CCO} – 0.3	2.5	V_{CCO} +0.3	
Digital Outputs and CLKO						
Logic compatibility				LVDS		
Output levels (LVDS)						
Logic low		V_{OL}	0.925	1.1		V
Logic high		V_{OH}		1.4	1.475	V
Swing		$V_{OH} – V_{OL}$	250	300	400	mV
Common mode		V_{OCM}		1.2		V
Output impedance (LVDS)		R_O	30	50	70	Ω
Change in Vod between 0 and 1 (LVDS)					25	mA
Change in Vos between 0 and 1 (LVDS)					25	mA
Output current (shorted output) (LVDS)					12	mA
Output current (grounded output) (LVDS)					30	mA
Output level drift with temperature (LVDS)				1.4		mV/°C
Reset Input						
Logic compatibility for RESET input				PECL/LVDS		
2.5V PECL differential logical level						
Logic *0* voltage		V_{IL}	0.5	0.68	1	V
Logic *1* voltage		V_{IH}	1.3	1.48	1.9	V
Swing (peak-to-peak)		$\|V_{IL} – V_{IH}\|$		0.8		V
3.3V PECL differential logical level						
Logic *0* voltage		V_{IL}	1.3	1.48	1.9	V
Logic *1* voltage		V_{IH}	2	2.28	2.6	V
Swing (peak-to-peak)		$\|V_{IL} – V_{IH}\|$		0.8		V
LVDS differential logical level						
Logic *0* voltage		V_{IL}	0.925	1.1	1.2	V
Logic *1* voltage		V_{IH}	1.3	1.4	1.475	V
Swing (peak-to-peak)		$\|V_{IL} – V_{IH}\|$		0.3		V
Differential logical levels compatibility						
Logic *0* voltage		V_{IL}	0		V_{CCD} –0.1	V
Logic *1* voltage		V_{IH}	1.3		V_{CCD} +0.1	V
Swing (peak-to-peak)		$\|V_{IL} – V_{IH}\|$	0.2		V_{CCD} +0.1	V

Section 4

Software Tools

4.1 Overview

The 12-bit 500 Msps ADC Evaluation user interface software is a Visual C++® compiled graphical interface that does not require a licence to run on a Windows® NT® and Windows® 2000/98/XP® PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Configuration

The advised configuration for Windows® 98 is:

- PC with Intel® Pentium® Microprocessor of over 100 MHz
- Memory of at least 24 Mo
- For other versions of Windows® OS, use the recommended configuration from Microsoft

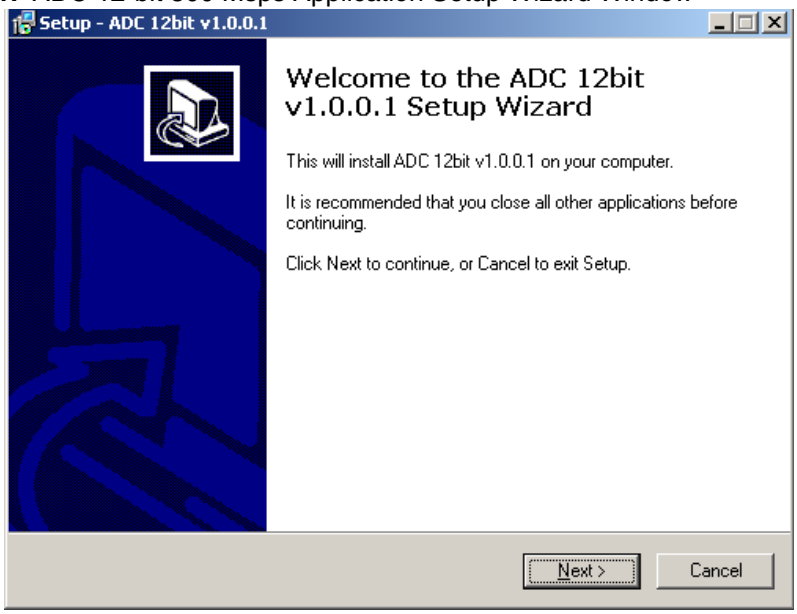
Note: Two COM ports are necessary to use two boards simultaneously.

4.3 Getting Started

1. Install the ADC 12-bit application on your computer by launching the ADC_12bit_1.0.x.x.exe installer (please refer to the latest version available).

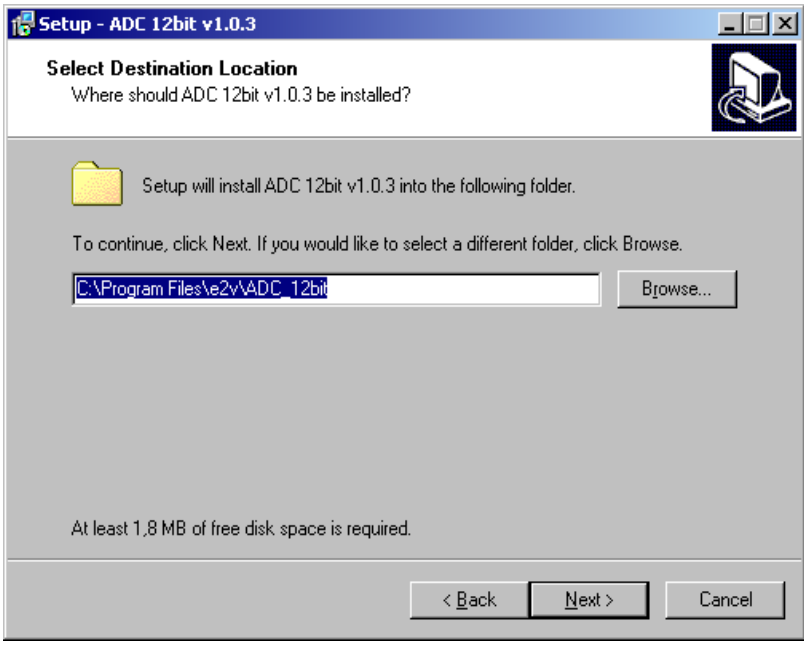
The screen shown in Figure 4-1 is displayed:

Figure 4-1. ADC 12-bit 500 Msps Application Setup Wizard Window



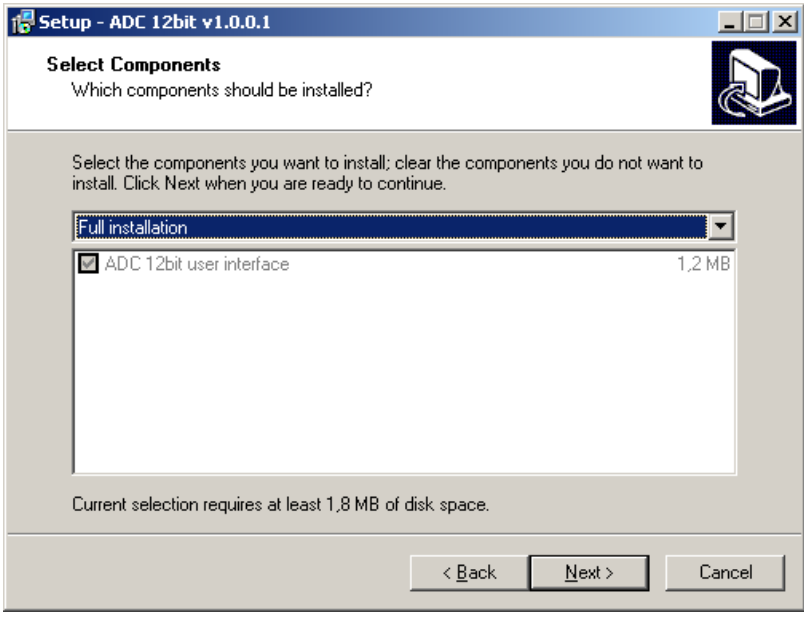
2. Select Destination Directory

Figure 4-2. ADC 12-bit 500 Msps Select Destination Directory



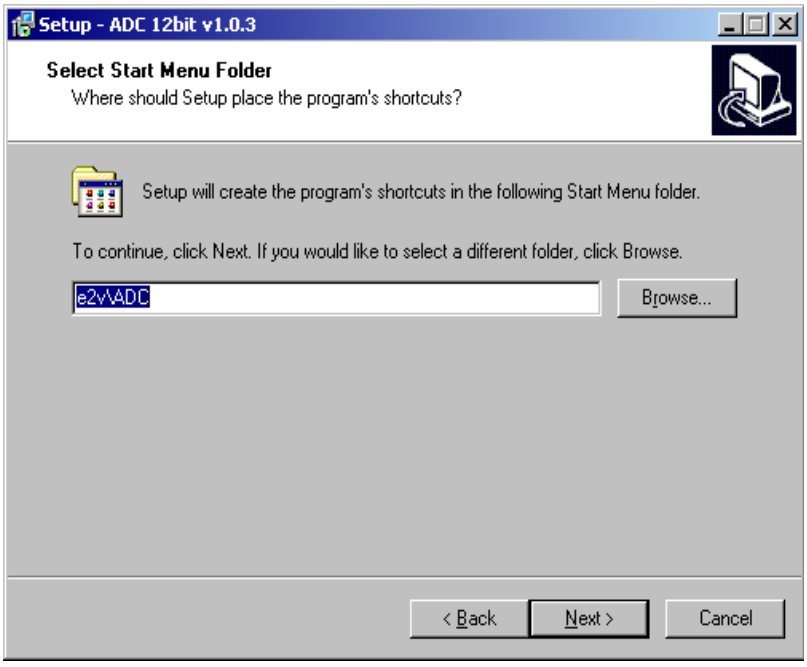
3. Select Components (choose full installation)

Figure 4-3. ADC 12-bit 500 Msps Select Component Window



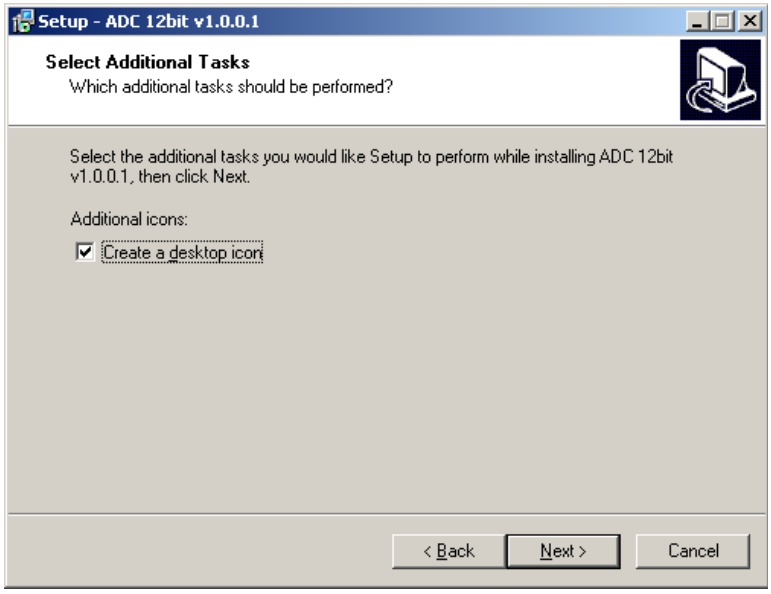
4. Select Start Menu Folder

Figure 4-4. ADC 12-bit 500 Msps Select Start Menu Window



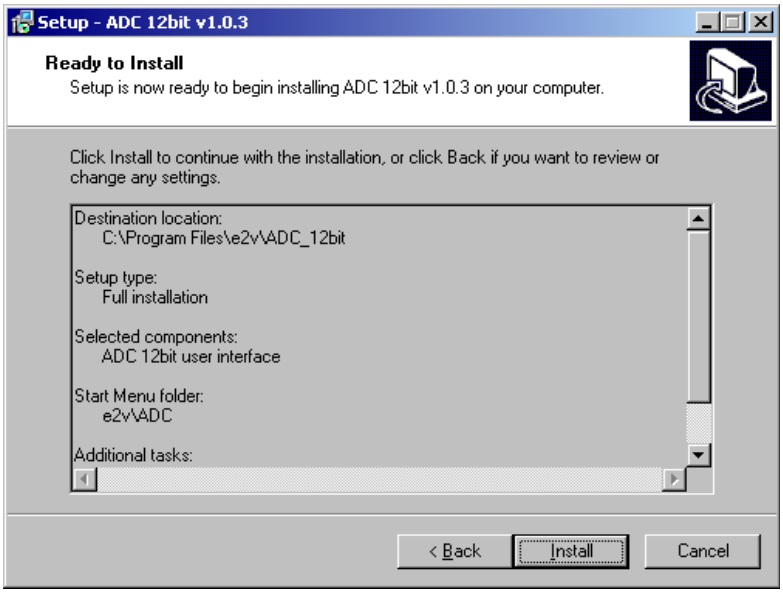
5. Select Additional Tasks

Figure 4-5. ADC 12-bit 500 Msps Select Additional Task Window



6. Ready to install

Figure 4-6. ADC 12-bit 500 Msps Ready to Install Window

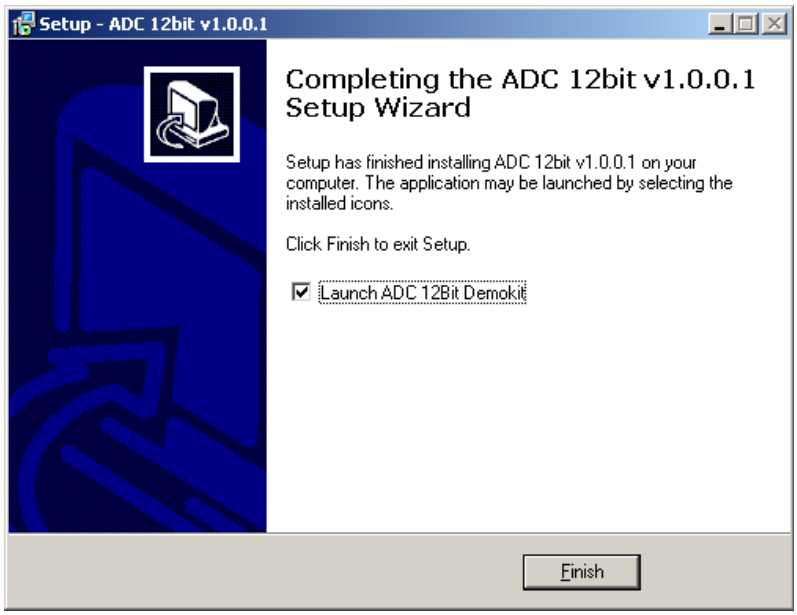


If you agree with the install configuration press *Install* button.

Figure 4-7. ADC 12 bit 500 Msps application Setup Install Push Button

The installation of the software is now complete.

Figure 4-8. ADC 12 bit 500 Msps Completing Setup Wizard Window

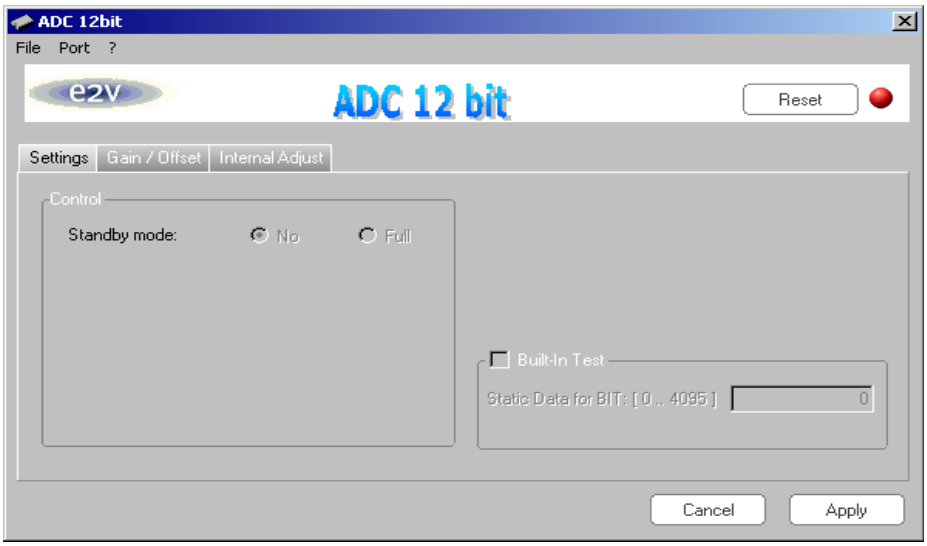


After the installation, you can launch the interface with the following file:

C:\Program Files\e2v\ADC_12bit\ADC12Bit.exe

The window shown in Figure 4-9 will be displayed.

Figure 4-9. ADC 12-bit 500 Msps User Interface Window



Note:
1. If the ADC 12 bit 500 Msps application board is not connected or not powered, a red LED appears on the right of the reset button and the application is grayed out.
2. Check your connection and restart the application.
3. If the serial interface is not active the LED appears in orange and the application is grayed out too.

Figure 4-10. ADC 12-bit 500 Msps User Interface Window

Turn **ON** the switch on the demo board, the application should become available and the LED turns to green.

Figure 4-11. ADC 12-bit 500 Msps User Interface Window

4.4 Troubleshooting

1. check that you own rights to write in the directory.
2. check for the available disk space.
3. check that at least one RS-232 serial port is free and properly configured.
4. check that the serial port and DB9 connector are properly connected.
5. check that all supplies are properly powered on.
6. check that the serial mode is active (green LED ON).

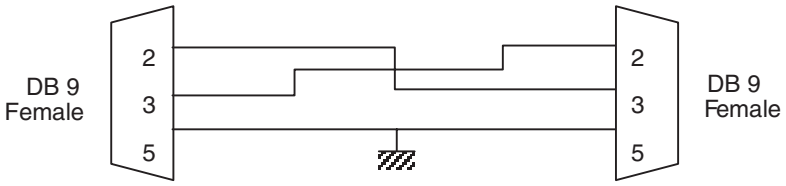
The serial port configuration should be as fallows:

- Bit rate: 19200
- Data coding: 8 bits
- 1 start bit, 1 stop bit
- No parity check

Figure 4-12. 12 bit ADC User Interface Hardware Implementation

1. Use an RS-232 port to send data to the ADC.
2. Connect the crossed DB 9 (F/F) cable between your PC and your evaluation board as illustrated in Figure 4.13 on page 4-7.

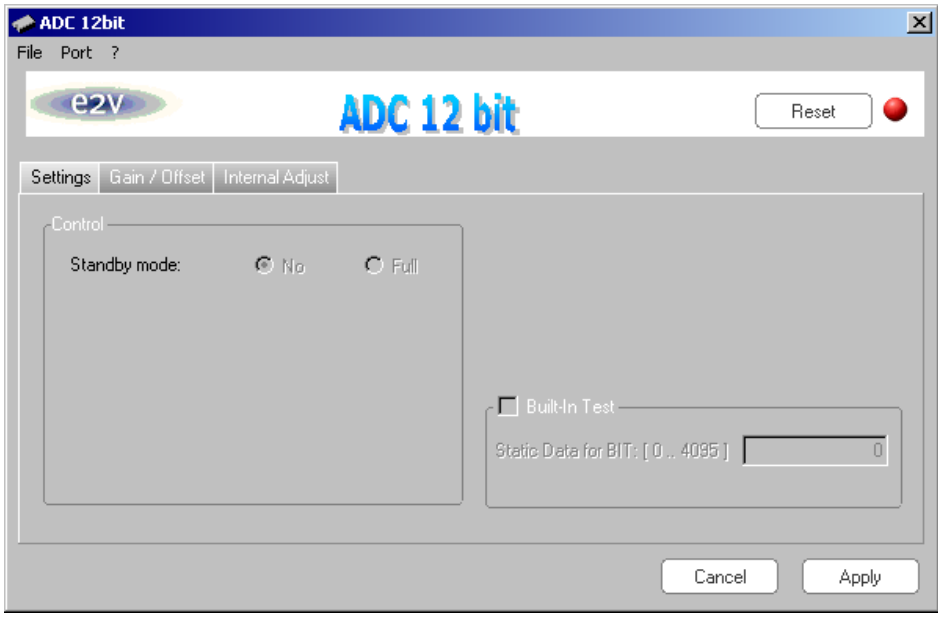
Figure 4-13. Crossed Cable



4.5 Installation Software

At startup, the application automatically checks all RS232 ports available on the computer and tries to find the evaluation board connected to the RS232 port.

Figure 4-14. 12-bit ADC User Interface Port Menu



The *Port* menu shows all available ports on your computer. The port currently used has a check mark on its left. By clicking another port item the application will try to connect to an evaluation board via the selected port. If a board is successfully detected on the new port, the LED is green and the new port gets the check mark. If the application is not able to find a board on this port, an error message is displayed.

4.6 Operating Modes

The software provides a graphical user interface to configure the ADC.

Push buttons, popup menus and capture windows allow easy:

1. Setting.
2. Gain/offset.
3. Internal adjustment.

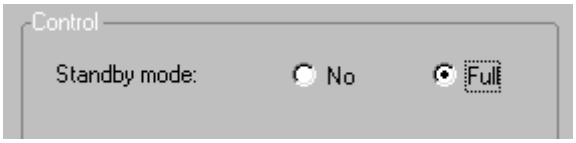
Always click on *Apply* button to validate any command.

Clicking the *Cancel* button will restore last settings sent with *Apply* button.

Reset button allows to configure ADC (Default Mode).

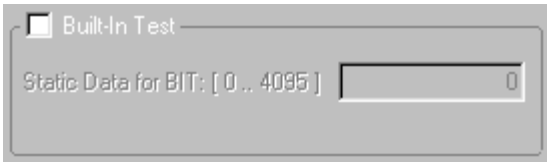
4.7 Settings

4.7.1 Standby Mode Configurable No or Full

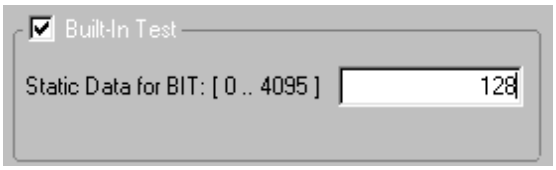


4.7.2 BIST Mode

ADC Built-in Test Inactive



ADC Built-in Test Active: Static Data 0 to 4095

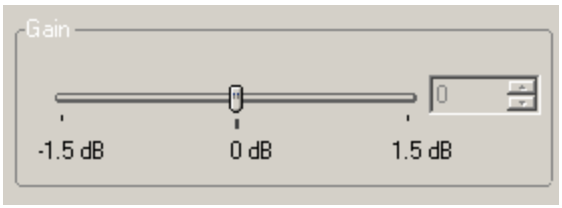


The Built-in Test allows to fix a constant output word. The data value can be fixed between 0 and 4095.

4.8 Gain/Offset

4.8.1 Gain

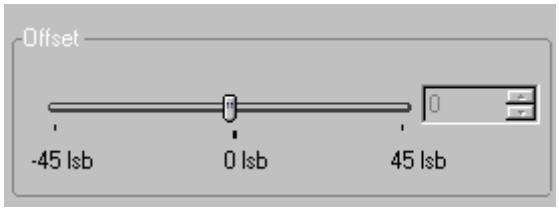
The *Gain* can be adjusted (–1.5 to 1.5 dB).



The gain mode allows to adjust the ADC full scale in function of the analog input level used.

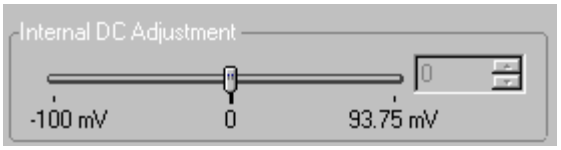
4.8.2 Offset

The *Offset* can be adjusted (–45 to 45 LSB).



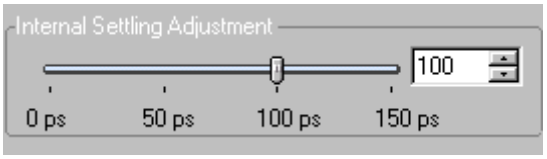
4.9 Internal Adjustment

4.9.1 Internal DC of ADC Adjustment < –100 to 93.74 mV



The internal DC voltage allows to adjust the internal common mode offset. The best configuration suggested is between -50 mV to 0 mV..

4.9.2 Internal Settling of ADC Adjustment 0 to 150 ps)



The *internal setting adjustment* allows to change the sampling time. The default value (0 ps) is suggested the best adjustment.

4.9.3 ADC Duty Cycle (Track-Hold) 40% to 60% or 50% to 50%

The internal duty cycle of the Track-Hold can be adjusted. We recommend to use 40%-60% for high analog input frequencies. (that is > 150 MHz).

Section 5

Application Information

5.1 Analog Input

The analog input (VIN, VINN) is entered in differential AC coupled mode as described in Figure 5-1.

Pins R10 and R7 are used for the reverse 50Ω termination and are also AC coupled via 10 nF capacitors.

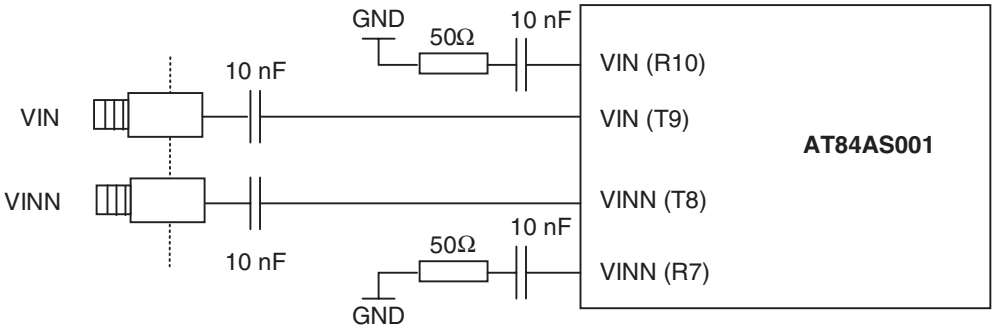
The single-ended operation for the analog input is not allowed as it would degrade the ADC performance significantly. It is thus recommended to use a differential source (DC to 500 MHz maximum) to drive the analog input of this ADC (external balun or differential amplifier).

References of differential amplifiers and external baluns:

- M/A-COM H9 balun
- M/A-COM TP101 1:1 transformer

In order to optimize the performance of the ADC, it is also recommended to use a band pass filter on the analog input path.

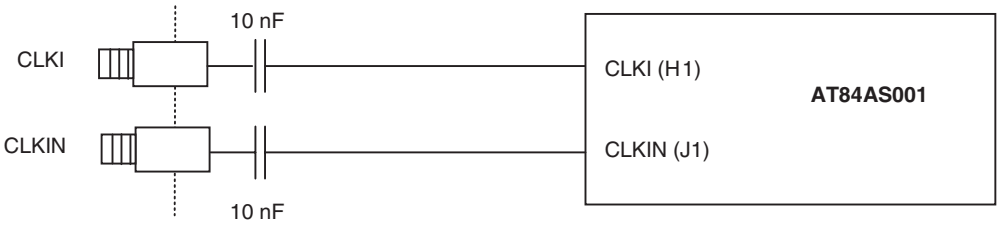
Figure 5-1. Analog Input Implementation



5.2 Clock Input

The clock input can be entered indifferently in single-ended or differential mode with no performance degradation. The clock is AC coupled via 10 nF capacitors as described in Figure 5-2.

Figure 5-2. Clock Input Implementation



If used in single-ended mode, CLKIN should be terminated to ground via a 50Ω resistor. This is physically done by shorting the SMA on CLKIN with a 50Ω resistor.

The jitter performance on the clock is crucial to obtain optimum performance from the ADC. We thus recommend to use a very low phase noise clock and to filter the clock signal if a fixed frequency is used.

For a clock at 500 MHz, we use in our test bench:

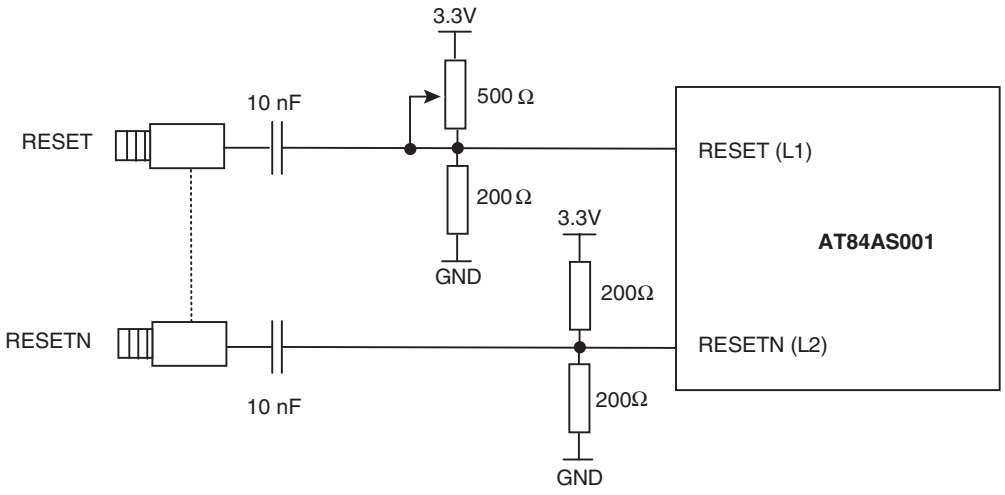
- Pass band filter from LORCH MICROWAVE 9BP8-500/30-S (up to 8 dB attenuation, 70 dB rejection up to 5000 MHz)
- 500-14512 500 MHz-SC Sprinter Crystal Oscillator from WENZEL Associates

5.3 Reset input

The Reset is not necessary to start the ADC but it is recommended to apply a reset after power up.

The reset signal is implemented as illustrated in Figure 5-3.

Figure 5-3. Reset Inputs Implementation

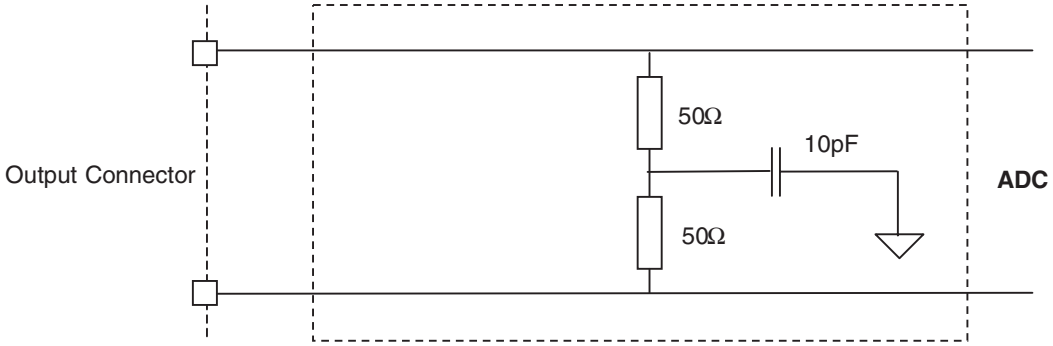


By turning the potentiometer on the RESET signal to the 3.3V, you activate the reset and deactivate it by turning the potentiometer back to its initial position (near ground). Reset is active low

5.4 Output Data

The output data are LVDS and are 2 × 50Ω terminated to ground via a 10 pF capacitor as shown in Figure 5-4.

Figure 5-4. Output Data On-board Implementation



Note: The data are output in binary format and in double data rate (the output clock frequency is half the data rate and thus half the input clock frequency).

5.5 VCSH Output Signal

A 2 mm banana jack is provided for the VCSH signal which provides the analog input common mode voltage (= 0.42 V_{CCA}).

As the analog input is entered in AC coupled mode, this VCSH does not need to be used but is output on a banana jack for debug.

5.6 Diode for Junction Temperature Monitoring

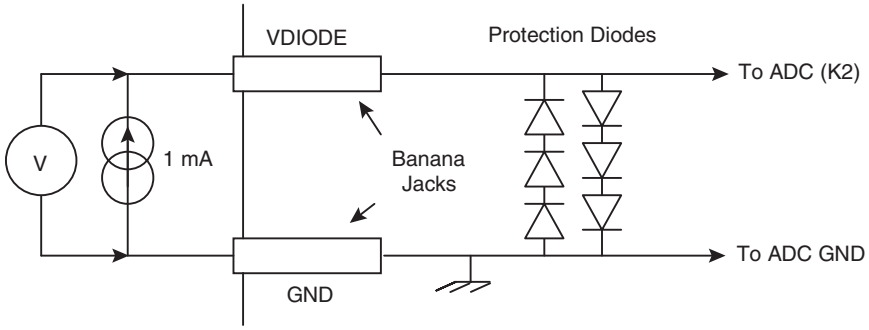
Two 2 mm banana jacks are provided for the die junction temperature monitoring of the ADC.

One banana jack is labeled VDIODE and should be applied a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to ground.

The ADC diode is protected via 2 × 3 head-to-tail diodes.

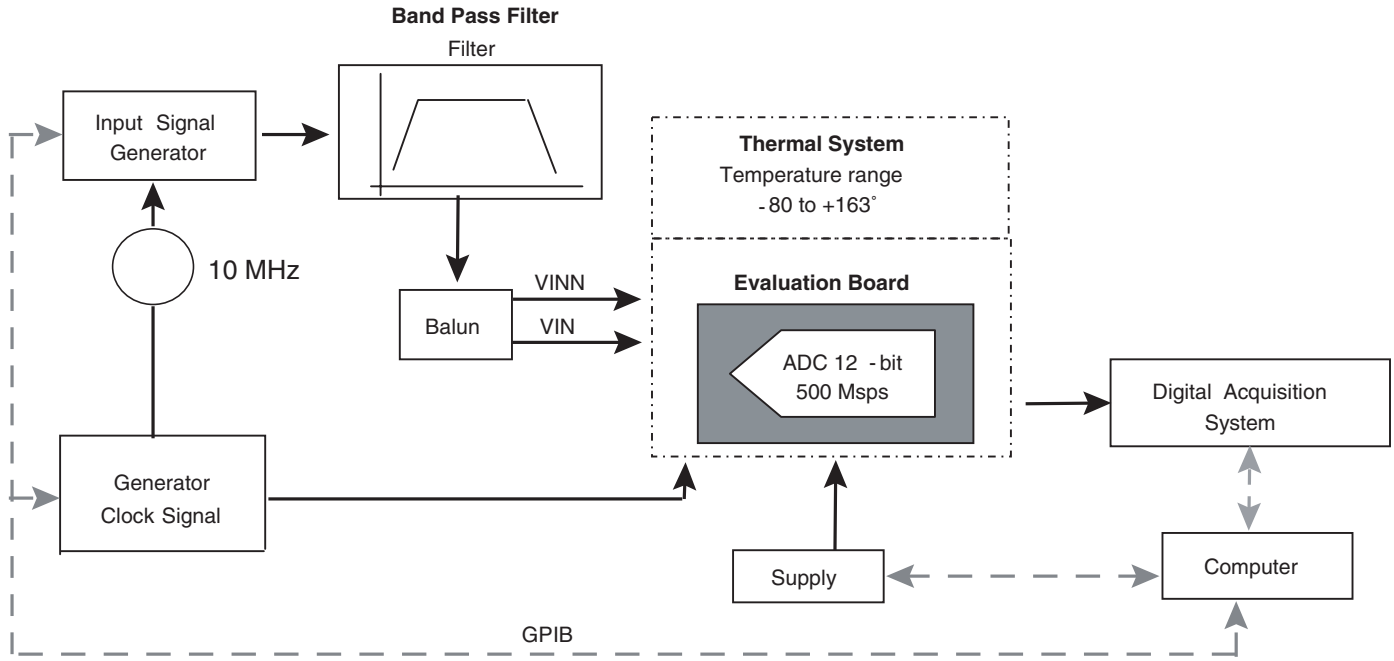
Figure 5-5 describes the setup for the die junction temperature monitoring using a multimeter.

Figure 5-5. Die Temperature Monitoring Test Setup



5.7 Test Bench Description

Figure 5-6. Test Bench Description



Section 6

Ordering Information

6.1 Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
AT84XAS001TP	TBGA 192	Ambient	Prototype	
AT84AS001CTPY	EBGA 192 RoHS	Commercial *C* grade $0°C < T_{amb} < 70°C$	Standard	For availability please contact your local sales office
AT84AS001VTPY	EBGA 192 RoHS	Industrial *V* grade $–40°C < T_{amb} < 85°C$	Standard	For availability please contact your local sales office
AT84AS001TP-EB	TBGA 192, or EBGA 192 RoHS	Ambient	Prototype	Evaluation board

Section 7

Appendices

7.1 AT84AS001-EB Electrical Schematics

Figure 7-1. Power Supplies Bypassing

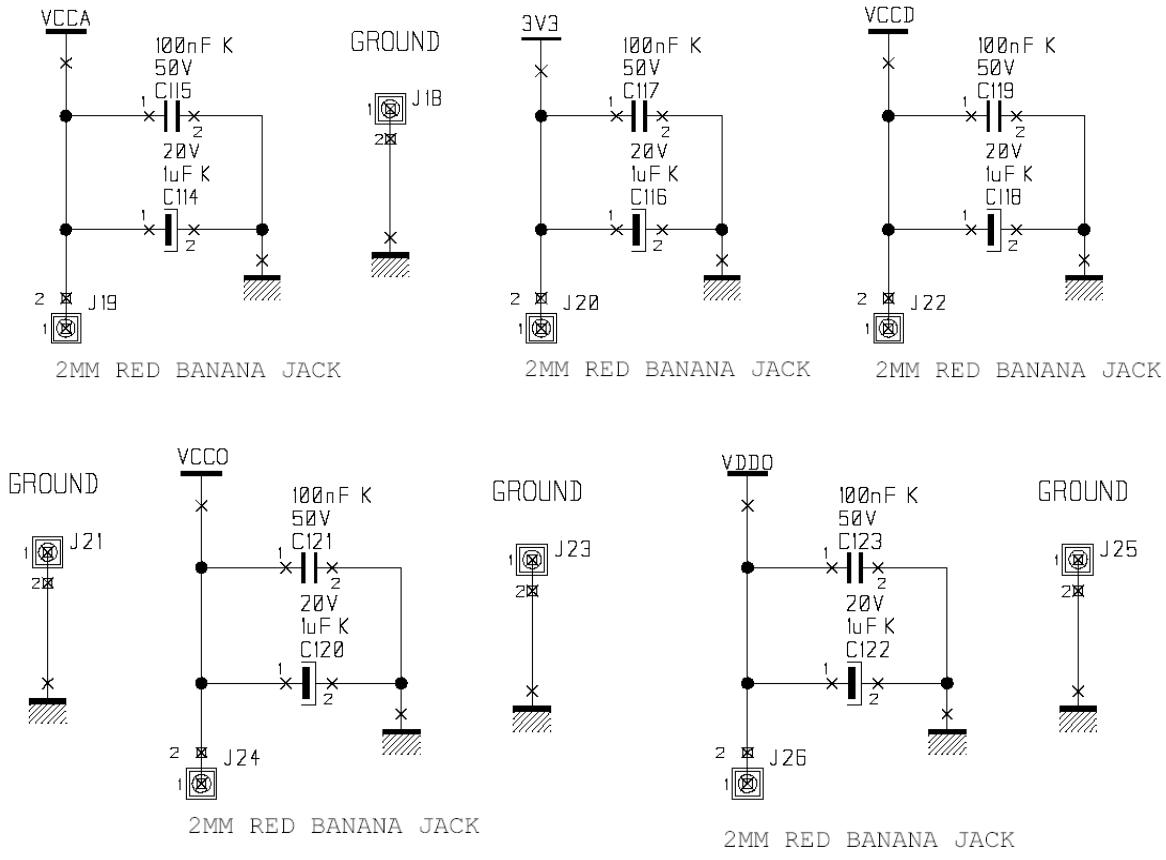


Figure 7-2. Power Supplies Decoupling (J = ±5% Tolerance)

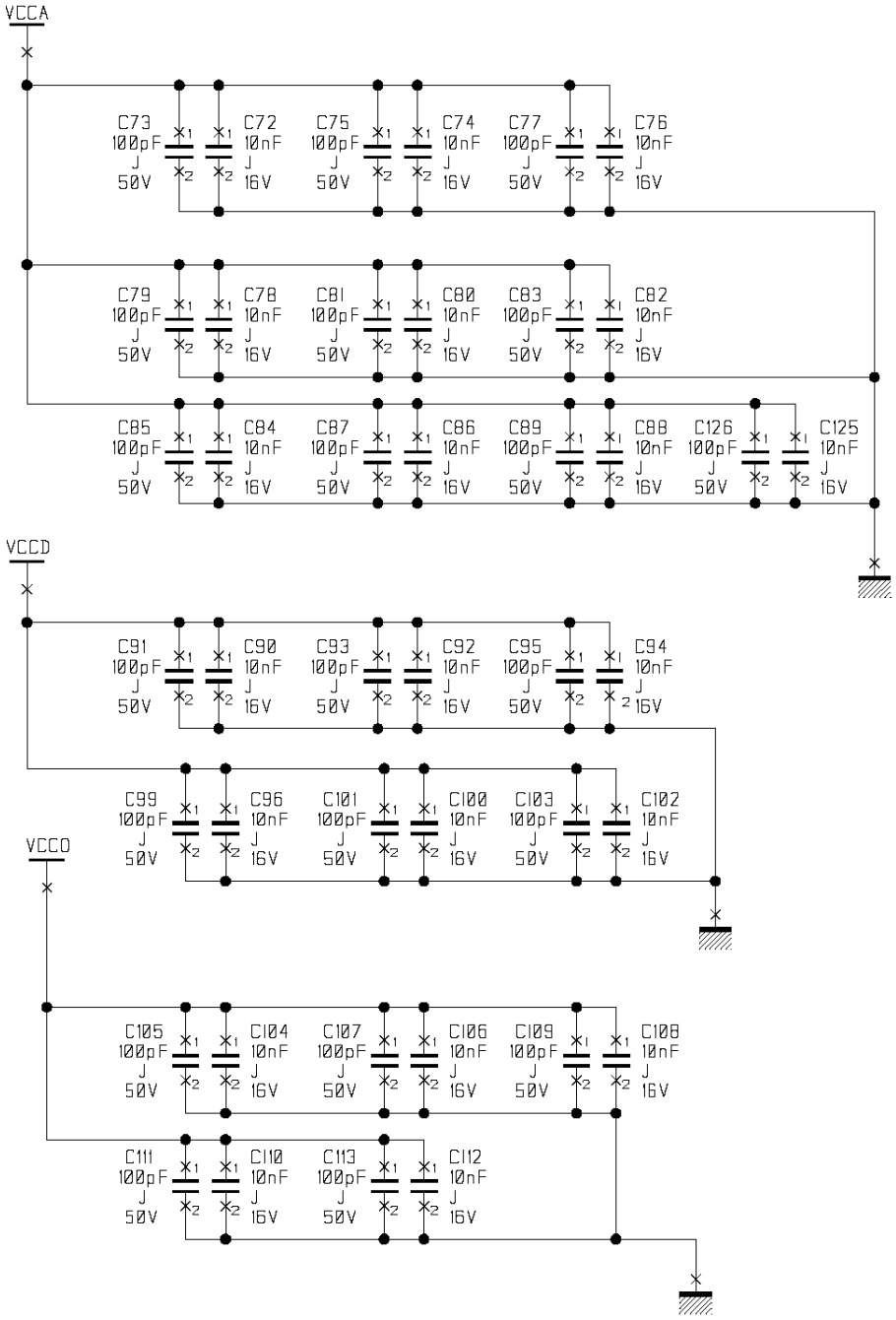


Figure 7-3. Electrical Schematics (ADC)

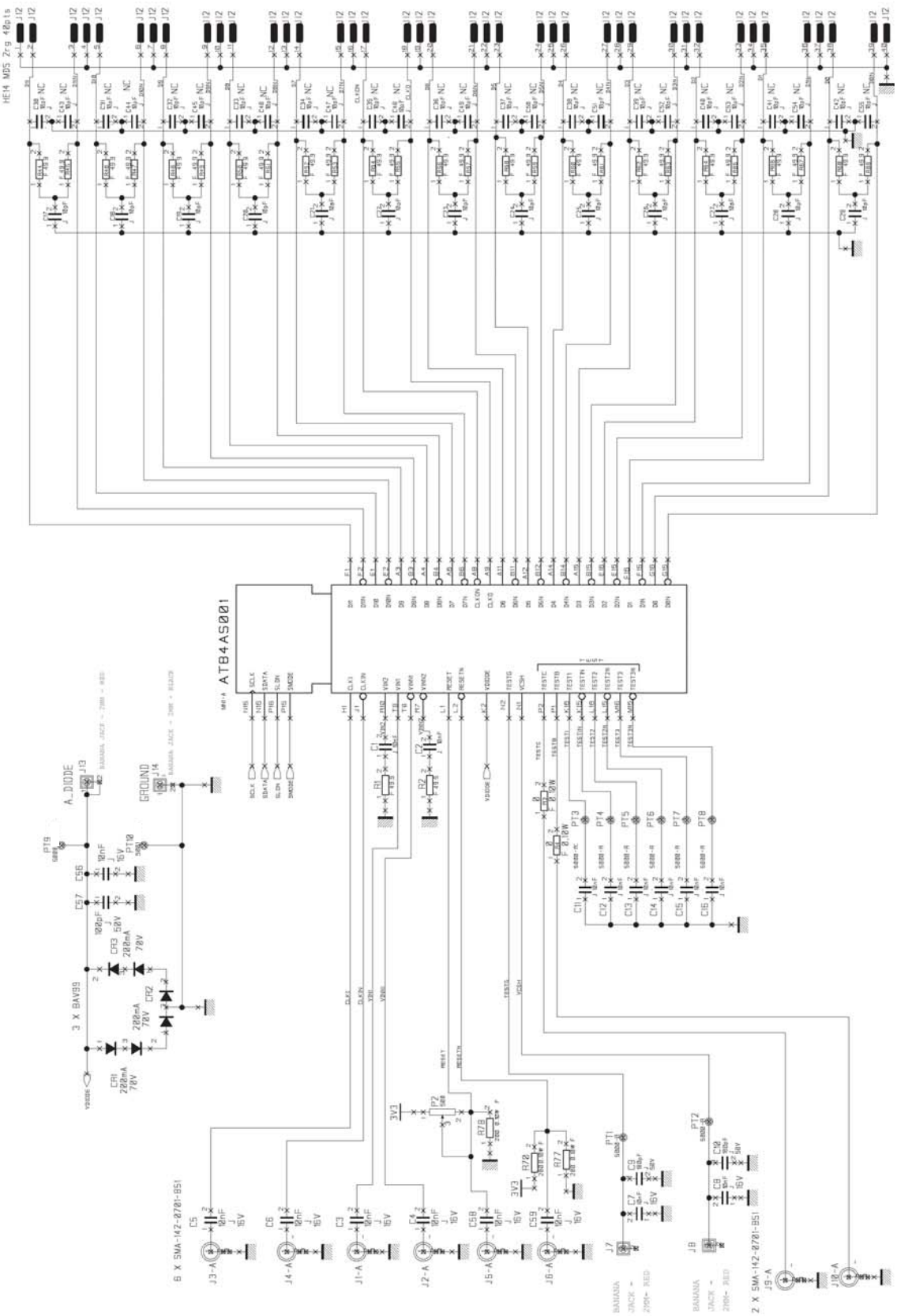
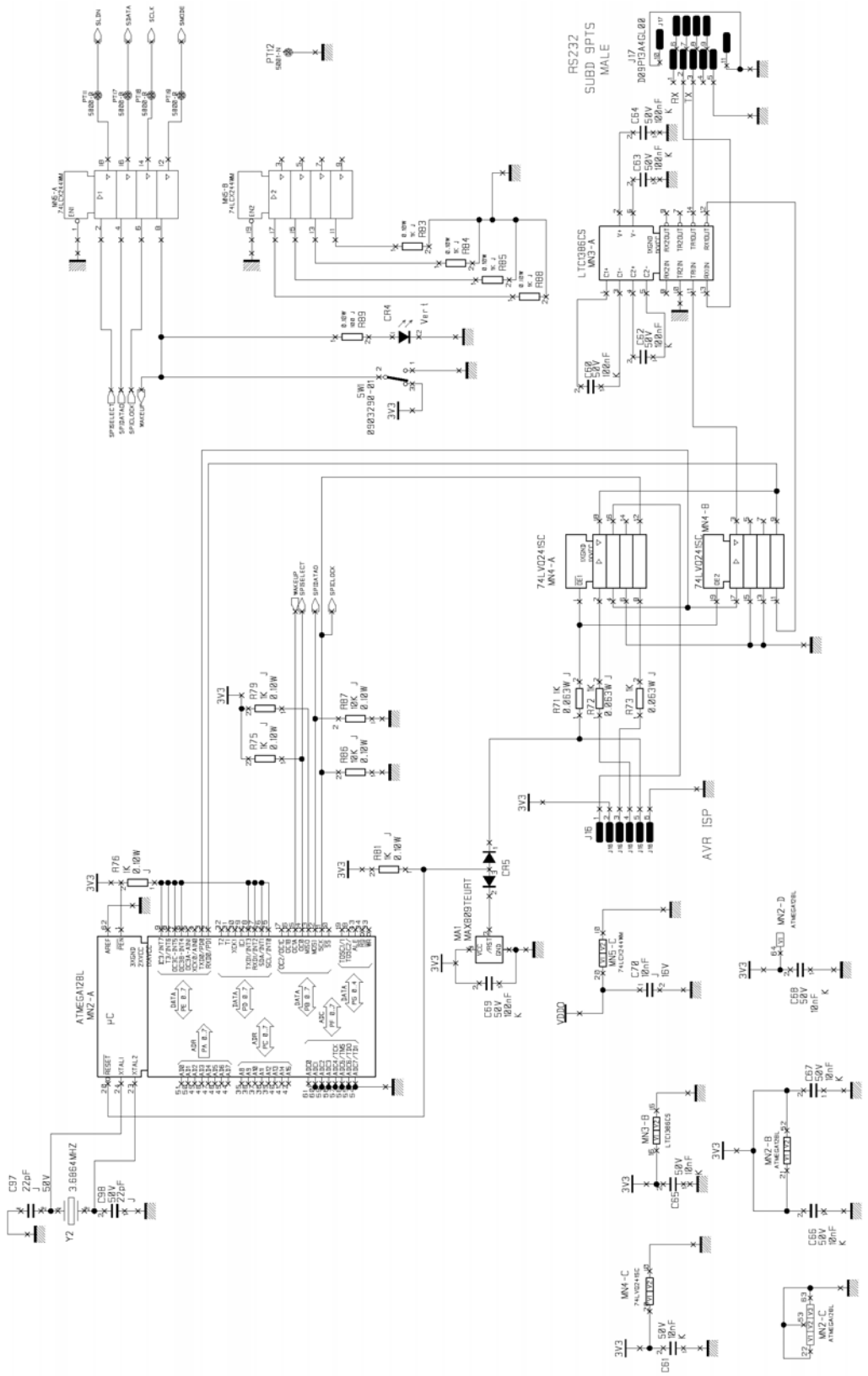


Figure 7-4. Electrical Schematics (AVR)



7.2 AT84AS001-EB Board Layers

Figure 7-5. Top Layer

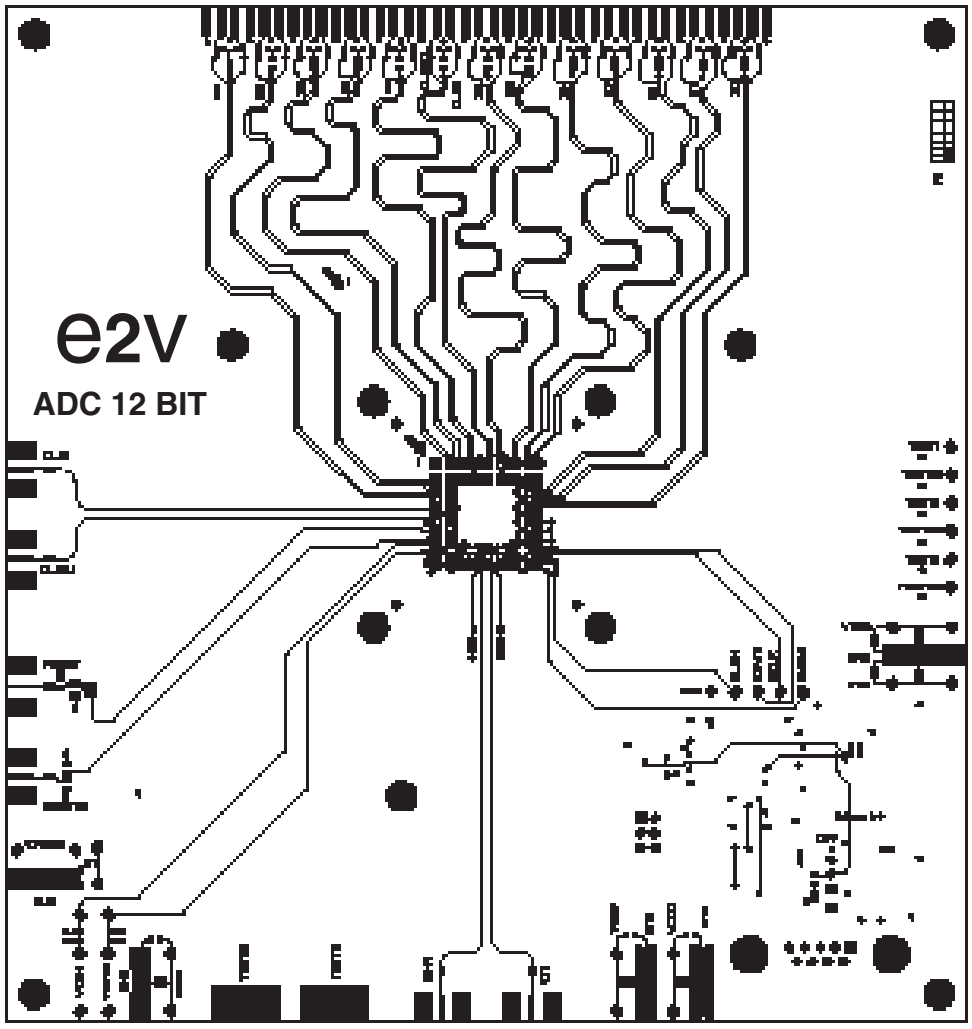


Figure 7-6. Bottom Layer

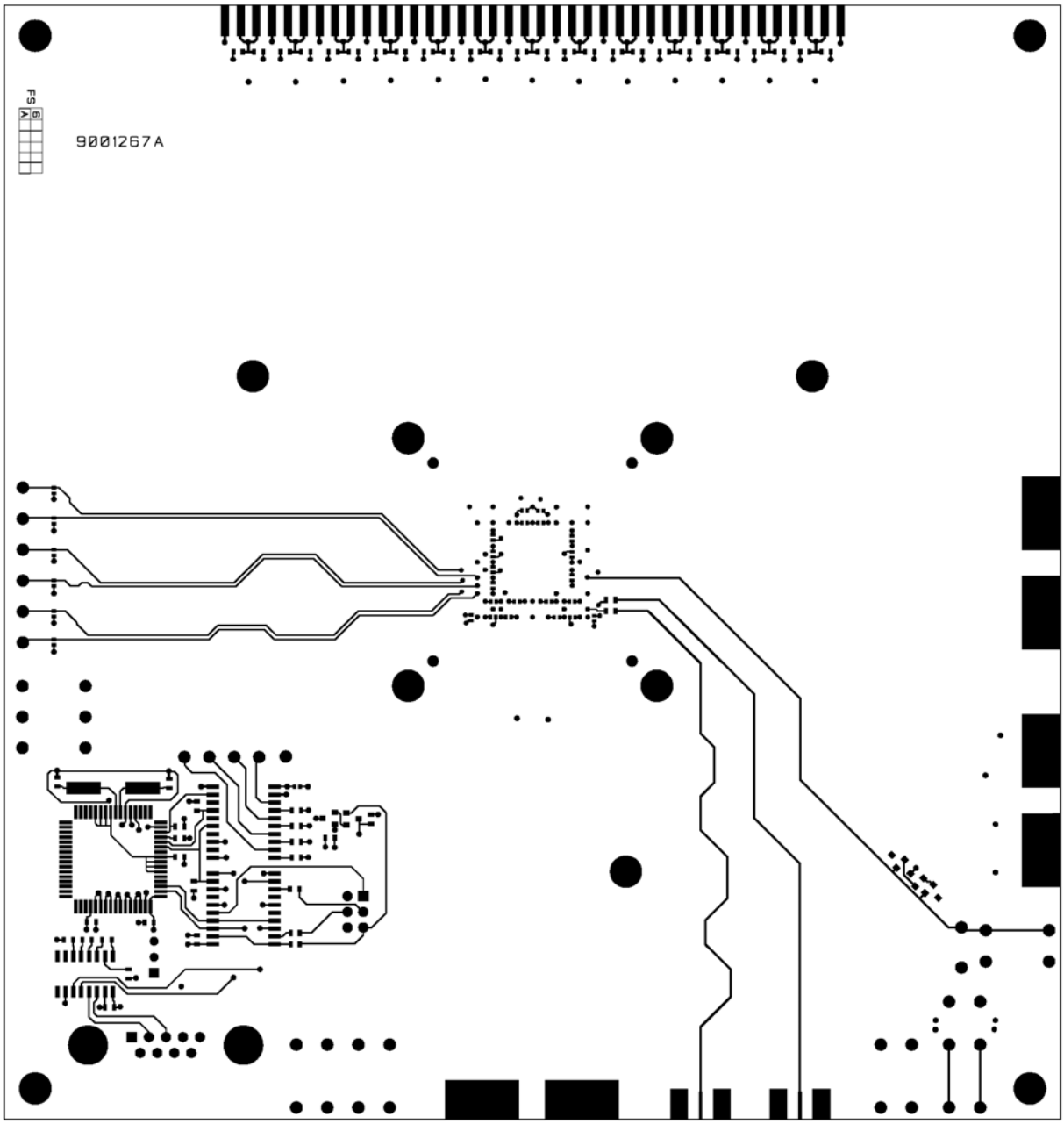


Figure 7-7. Equipped Board (Top)

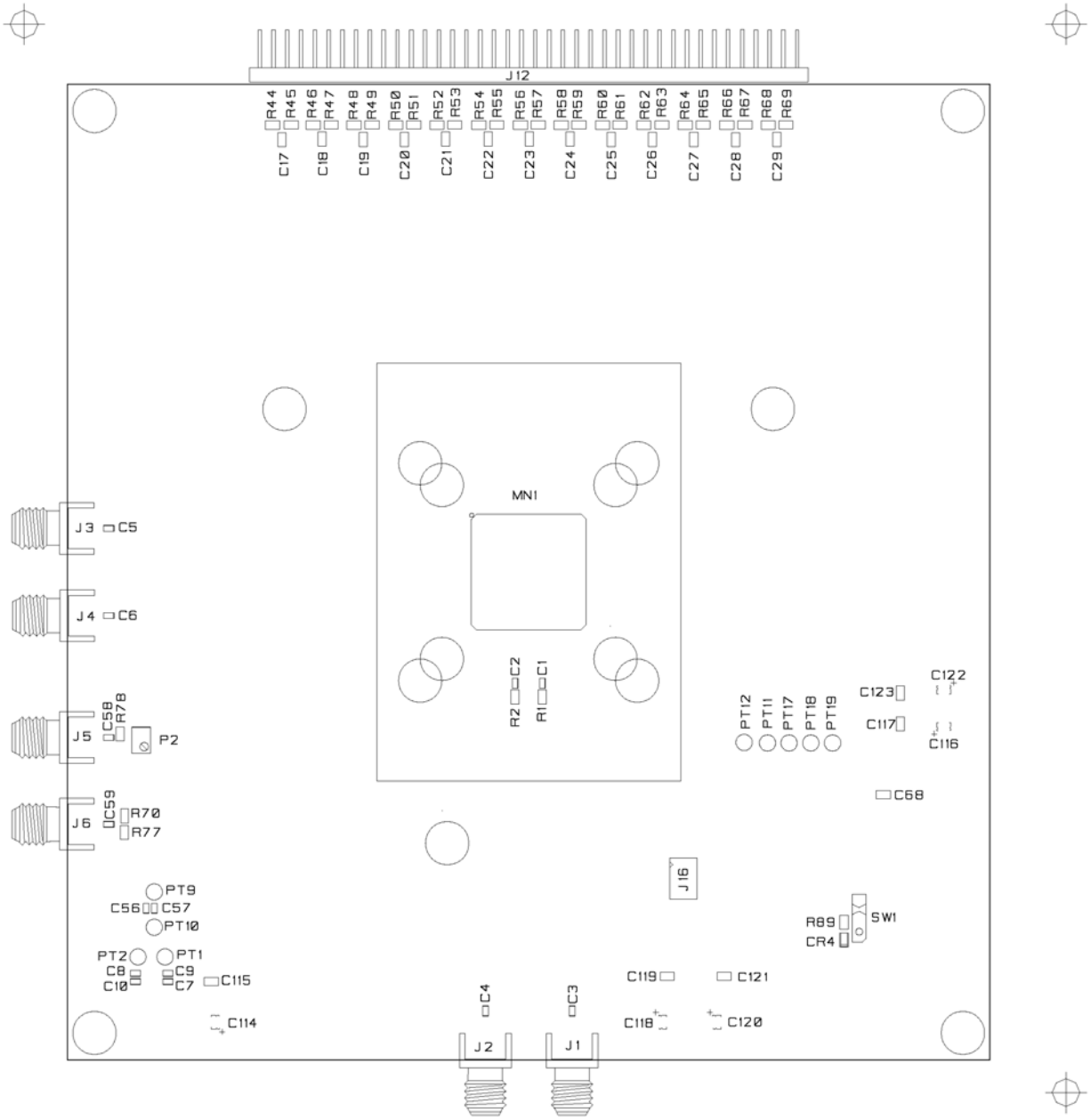
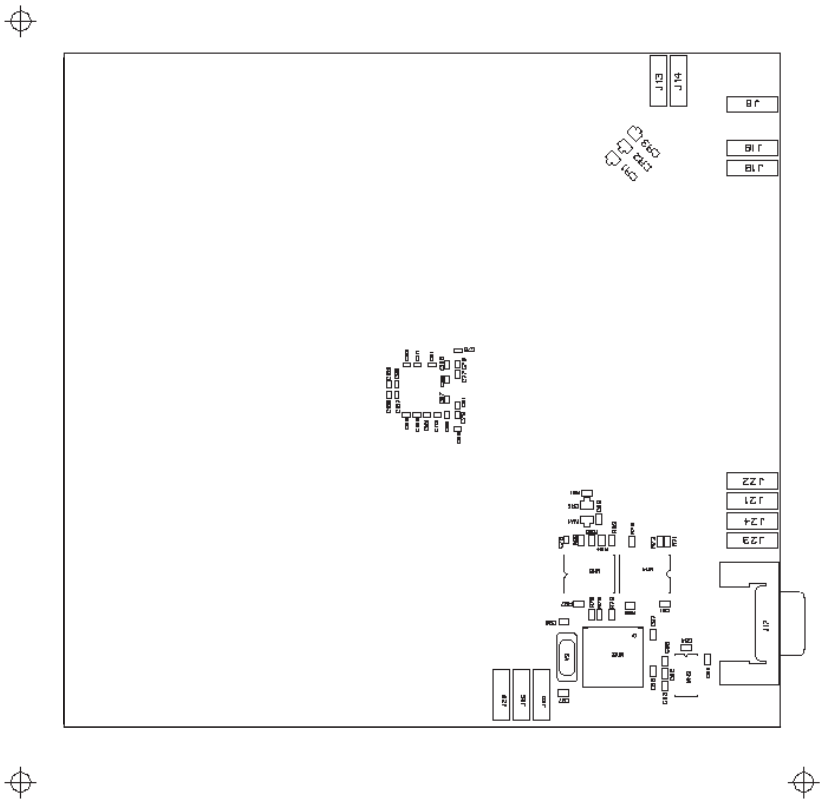


Figure 7-8. Equipped Board (Bottom)



e2v

5467B–BDC–12/06